High-Range Switched-Capacitor Tracking Filter

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Abstract—A high-range switched-capacitor (SC) filter capable of tracking sinusoidal signals without the need of a reference is presented. The filter tracks sinusoids by adapting the sampling clock of the switched-capacitors. An important feature of this filter is its ability to track sinusoidal signals in cases where the frequency of the signal and the center frequency of the filter are off by several octaves. This is particularly useful in applications where the range of frequencies of the signal is very wide.

I. INTRODUCTION

Tracking sinusoid signals in noise is a common procedure in communications, radar, and spectral analysis applications. Traditional techniques to track sinusoids include methods such as FIR filters combined with LMS algorithm (least mean square) [1], phase-locked loops (PLL), and adaptive constrained IIR structures [2]. Adaptive FIR filters can, under the right conditions, achieve close to optimum solution but have the disadvantage of being computationally intensive and are slow to converge. Conventional PLL-based tracking filters are faster and easier to implement but they require a reference whose center frequency is relatively close to the input signal, this severely limits their range of operation. Finally, constrained IIR structures have the characteristic of adjusting only the center-frequency dependent coefficients of the filter in order to track the signal. Because only the center-frequency parameters are adjusted, constrained IIR structures are more stable, and are more computationally efficient than adaptive FIR filters, although their response is not as fast as PLL structures.

Our switched-capacitor implementation, like all other switched-capacitor implementations of tracking filters mentioned in literature ([3], [4], [5]), takes advantage of the property that the frequency response of switched-capacitor filters can be scaled along the frequency axis by varying the frequency of the sampling clock of the switched-capacitors [6]. However, one of the disadvantages of the implementation mentioned in [3], which is a PLL structure, is that the filter requires a reference signal to bring the PLL to lock range. Furthermore, this implementation is unsuitable for applications in which the phase difference between the input signal and the PLL is off by more than 90°. The implementations mentioned in [4] and [5] are based on constrained IIR structure but have the disadvantage of being slower than PLL structures.

In this paper, we propose a tracking filter implementation that provides a compromise between PLL's and constrained IIR structures. Our implementation is a structure that is based on a hybrid implementation of these two approaches and consists of a constrained IIR structure that uses a phase tracking mechanism. The system is capable of tracking sinusoidal signals without the need of a reference to bring the circuit to locking range.

The resulting implementation is a filter that shares some of the best qualities of constrained IIR and PLL structures such as high computational efficiency, high stability, fast response, and a high-range of operation.

II. SYSTEM DESCRIPTION

The system diagram of the SC tracking filter is shown in Fig. 1. The system is composed of a second order SC bandpass filter with center frequency \( f_0 = f_{clk}/100 \), where \( f_{clk} \) represents the sampling clock of the switched-capacitors. Because SC filters have pole frequencies that are directly proportional to the sampling rate of the clock, the frequency response of the SC bandpass can be adapted by simply varying the frequency of the sampling clock of the switched-capacitors [6].

![Fig. 1. Block diagram of switched-capacitor tracking filter.](image-url)
III. ADAPTATION MECHANISM

The objective function for the adaptation mechanism is the square value of the output of the notch $e^2(t)$. The goal is to minimize $e^2(t)$ by controlling the center frequency parameter of the filter. When this output is minimized, the tracking filter is locked onto the input signal.

The proposed algorithm minimizes $e^2(t)$ by finding the optimum value of the center-frequency dependent parameter $f_{\text{clk}}(t)$ and it is described by the following equation.

$$f_{\text{clk}}(t) = f_{\text{clkt}}(t - \Delta t) - \mu e^2(t) \text{sgn}(\phi(t)) \tag{1}$$

The parameter $\text{sgn}(\phi)$ represents the sign of the phase comparator output, and $\mu$ is a constant of proportionality selected to guarantee stability in the process. Equation (1) shows how the clock rate $f_{\text{clkt}}(t)$ is dependent of its past rate value $f_{\text{clkt}}(t-\Delta t)$ and by an adaptation step whose direction and magnitude are determined by the sign of the phase difference $\text{sgn}(\phi)$ and by the magnitude of the square of the output of the notch $e^2(t)$.

IV. CIRCUIT IMPLEMENTATION

The SC tracking filter was implemented using discrete components. The bandpass was built with a MF10 universal monolithic switched-capacitor filter from National Semiconductors. It was designed to have a center frequency $f_o$ of 5KHz for a $f_{\text{clk}}/f_o$ ratio of 100. The quality factor was designed for $Q=10$. The notch filter was formed by using an analog adder that subtracted the output of the bandpass from its input. The response of the notch filter is shown in Fig. 3.

![Response of SC-Notch when the input is swept from 2KHz to 8KHz and $f_{\text{clk}}(t)$ is constant at 500KHz.](image-url)
The multiplier was implemented with an AD633 analog multiplier from Analog Devices. The adder and integrator were built using standard 741 operational amplifiers. The clock was generated with a LM566C Voltage Controlled Oscillator and it was configured to operate on a range from 200kHz to 800kHz. This range was adequate to track sinusoid signals between 2KHz and 8KHz.

The phase comparator, shown in figure 4, was built with standard 74LS74 D-Flip Flops and a 74LS00 nand gate. The phase comparator is based on a sequential phase-frequency detector (S-PFD) used in phase lock synthesizers. The input signal and the output of the SC bandpass filter are converted to square waves and compared by the S-PFD. The duty cycles of the pulses available at the S-PFD outputs are proportional to the phase difference. These pulses are then filtered through a lowpass filter and then compared to generate a constant signal which is positive if the output of the bandpass leads the input or negative otherwise. Fig 5 shows the outputs of the S-PFD before they are filtered.

The outputs sgn(\(\phi\)) (top) and \(\mu e^2(t)sgn(\phi)\) (bottom) when the input signal is swept from 2KHz to 8KHz while \(f_{clk}(t)\) is kept constant at 500KHz.

V. EXPERIMENTAL RESULTS

As described in the previous section, a full prototype was built to verify the circuit operation. Figure 6 shows the feedback signal coming out of the multiplier that controls the VCO by adjusting the voltage level of the integrator. The sign of the phase comparator, sgn(\(\phi\)), is shown at the top of the figure and \(\mu e^2(t)sgn(\phi)\) at the bottom. The input is swept from 2KHz to 8KHz while \(f_{clk}(t)\) is maintained at 500KHz.

The transient response of the tracking filter is illustrated in Fig. 7. The signal on the top controls the VCO frequency. It takes about 15ms for the filter to track the signal when it steps from 8KHz down to 2KHz. The time for adaptation depends on how far apart the center frequency of the signal is with respect to the current \(f_0\) of the filter, but it also depends on the RC constant of the integrator.

Fig. 4. Schematic of sequential phase-frequency detector, S-PFD.

Fig. 5. Output of S-PFD showing the duty cycle changes as the signal leads (left) or lags (right) the reference. The bottom part shows the same output in more detail.

Fig. 6. The outputs sgn(\(\phi\)) (top) and \(\mu e^2(t)sgn(\phi)\) (bottom) when the input signal is swept from 2KHz to 8KHz while \(f_{clk}(t)\) is kept constant at 500KHz.

Fig. 7. Transient response of tracking filter showing the notch output while input signal is stepped from 8KHz to 2KHz.
Fig. 8. Output of the bandpass filter (bottom) when a 5KHz sine wave input is corrupted by noise.

The tracking filter was also tested when the input signal was corrupted by noise as shown in Fig. 8. Experimental testing showed that the filter was capable of tracking a sine wave as long as the noise did not exceed 50% of the amplitude of the input.

CONCLUSIONS

A version of a SC tracking filter capable of tracking sinusoid signals was implemented using discrete components but it can also be implemented in a single CMOS IC. The circuit was tested and demonstrated its ability to efficiently track sine signals without the need of a reference. The system was also capable of tracking sinusoid signals in the presence of noise.

REFERENCES