A CMOS Readout Circuit for LTPS-TFT Capacitive Fingerprint Sensor

Yu-Sheng Tiao, Meng-Lieh Sheu, Shi-Min Wu, Hong-Ming Yang

Abstract — In this paper, a CMOS readout circuit for capacitive fingerprint sensor fabricated by using low temperature polycrystalline silicon thin-film transistor (LTPS-TFT) process is presented. Based on capacitive fingerprint sensing, the readout circuit grabs the induced capacitance by the finger directly touched on the sensor chip. An experimental readout chip is designed for sensor array size of 30 x 30, and implemented by using a standard CMOS process. A prototype PCB is used to integrate the readout chip and sensor chip to achieve a fingerprint acquisition system.

I. FINGERPRINT SENSOR INTRODUCTION

Nowadays, the mobile appliances like PDAs, notebook computers and cellular phones bring us convenient yet inimical threat of privacy. The more convenient these mobile appliances are, the more significant the issue on personal security is. The demand of user authentication is becoming more and more important to protect against illegal access of personal mobile appliances. Conventional protection schemes such as personal identification number (PIN) or password may be replaced by biometrics technologies. A lot of biometrics technologies have been developed for user authentication. For example, face, fingerprint, hand geometry, keystroke dynamics, hand vein, iris, retinal pattern, signature, voice print, facial thermogram, odor, DNA, gait, and ear recognition are different biometrics technologies that are either widely used or under investigation. Many researchers make efforts on fingerprint authentication because of the property of low-cost solutions, reliability and technical soundness.

Up to the present, optical scan is the most common sensing type for fingerprint image acquisition. However, optical scan needs lens, light source, and some mechanical facility, which may provide the outstanding precision but hard to be embedded in a mobile appliances. In recent years, direct-touched fingerprint sensing, especially the capacitive fingerprint sensors, becomes more attractive due to the progress of semiconductor manufacturing process. The capacitive fingerprint sensors have the two main forms which are fabricated by CMOS and LTPS [1-4] processes. For the CMOS process, capacitive fingerprint sensor and readout circuit can be integrated effectively in a single chip. Nevertheless, the cost of capacitive fingerprint sensor will be very high due to its large sensing area. On the other hand, the cost of LTPS capacitive fingerprint sensor can be much lower than CMOS one. Yet, it usually needs an additional readout circuit to accomplish an integrated system. In this paper, a CMOS readout circuit for capacitive fingerprint sensor fabricated by using LTPS-TFT process is presented. Based on capacitive fingerprint sensing, the readout circuit grabs the induced capacitance by the finger directly touched on the sensor plate. A test readout chip is designed for 30 x 30 array size and implemented by using a standard CMOS process. A prototype PCB is used to integrate the readout chip and sensor chip to form a fingerprint acquisition system.

The paper is organized as follows. The introduction of fingerprint sensor is in section 1. In section 2, the operation of LTPS capacitive fingerprint sensor is introduced. The architecture and design of readout circuit are described in section 3. Then, in section 4, the implementation of CMOS readout circuit and integration with LTPS sensor array are demonstrated. Finally, the conclusion is made in section 5.

II. FINGERPRINT ACQUISITION BY LTPS CAPACITIVE SENSOR

Fig 1 shows the basic sensing operation of a capacitive fingerprint sensor. The sensor is fabricated by using the top metal layer of semiconductor process as the bottom plate of sensing capacitor. The isolation glass is used as a dielectric layer. The finger surface would be the top plate of sensing capacitor. In microscopic scale, the surface of the fingerprint may have deep part like a valley or elevated part like a ridge. As the surface of the fingerprint contacts the sensor array, a capacitance value of a few to some tenths of fF would be induced according to the distance between the surface and the top metal plate. Intuitively, so called ridge part will produce a larger capacitance, $C_{rr}$ ($C_{rr} = C_1 = \frac{\varepsilon_1 A}{d_1}$); while the valley part is responsible of a smaller capacitance, $C_{rv}$ ($C_{rv} = C_1' - C_2' = d_1^{-1} d_2^{-1} \varepsilon_2 A \varepsilon_2 A$). By recognizing these variations on capacitance value, the valley and ridge of fingerprint pattern can be constructed.

![Fig 1. Capacitive Fingerprint Sensing](image-url)
Generally, the fingerprint pattern has line width and space in the range of 200µm to 400µm. To achieve a reasonable resolution for acquired fingerprint image, the size of unit sensor cell is designed to be 50µm × 50µm which results a 500 dpi resolution. In such small area of unit sensor cell, the induced capacitance is very little (about 10fF~300fF) for LTPS process. However, LTPS is not suitable for readout circuit. The readout circuit still needs to be implemented by CMOS process, and integrates with the sensor by packaging technology. Therefore, there exists a large parasitic capacitance (maybe as large as some pF) between the sensor and readout circuit. It becomes hard to sense the small capacitance on the unit sensor cell from the large parasitic capacitance.

In this paper, an experimental LTPS-TFT capacitive sensor array, whose unit sensor cell is shown in fig 2, of size of 30 x 30, provided by [5] is shown in fig 3. In order to obtain a larger capacitance, one TFT switch is used for controlling the sensing operation of the unit cell. The unit cell would sense a capacitance value about 320fF when a grounded finger surface covers the whole area of the unit sensor plate.

III. THE ARCHITECTURE AND IMPLEMENTATION OF READOUT CIRCUIT

A capacitive fingerprint sensor system typically comprises a capacitive sensor array and its readout circuit as shown in fig 4. In this work, the capacitive sensor array is built of LTPS-TFT process as described in previous section. To effectively read out the sensed capacitance of small values, a readout circuit for LTPS-TFT capacitive fingerprint sensor array is proposed as shown in fig 5. The readout circuit is designed and implemented by using a standard 0.35µm 5V CMOS process. A prototype PCB is then used to integrate the sensor array and readout circuit chips by wire bonding. Also, to drive the TFT, discrete components with 12V power supply are placed on the PCB.

A. Readout Circuit Design

A column-wise readout scheme is applied in the proposed readout chip. Each column has its own readout circuit. The unit pixels in the same column share a readout circuit as shown in fig 6. The readout circuit consists of three switches and followed by an amplifier stage. The transistors of Charge and Reset are responsible for pre-charging the sensor capacitor and clearing the unwanted charge in column line, respectively. The control timing is shown in fig 7. During pre-charging, the TFTs in selected row are turn on by a ROW_x signal. The induced capacitance ($C_{LTPS}$) by fingerprint as well as the parasitic capacitance ($C_P$) of the pixels in the selected row will both be charge to $V_{DD}$. Then the TFTs are turn off and a reset operation is performed to clear the charge stored in parasitic capacitance. After finishing pre-charge and column-reset, the ROW_x signal will enable again to perform charge sharing, a sensing voltage $V_X = (C_{LTPS} \times V_{DD})/(C_{LTPS} + C_P)$ is derived. The column switch passes $V_X$ into the following amplifier stage for signal amplification. The amplifier stage comprises $Gm$ amplifier, current integrator and correlated double sampling (CDS) sub-circuits. After the amplification, the amplified signals are selected column by column by a multiplexer to an analog to digital converter to obtain digital output.

![Fig 4. Capacitive Fingerprint Sensor System](image)

![Fig 5. Architecture of Readout Circuit for LTPS Capacitive Fingerprint Sensor Array](image)
The capacitive sensor and the readout circuit are connected by wire bonding, so a large parasitic capacitance exists in the column line. The sensed voltage is just some mV to hundreds of mV. A Gm amplifier is used to transform the sensed voltage into current as shown in fig 8, where Md9 transistor is an enable switch. fig 9 shows a current amplifier to perform current integration. The integrated voltage is stored in a 2pF capacitor. Then a correlated double sampling (CDS) stage, as shown in fig 10, works as an output stage to mitigate possible fixed pattern noise of sensor array [6].

B. Digital Control Circuit

Figure 11 shows the readout control circuit architecture. An external 2MHz clock, which is designated for sensing 10 frames per second in a 300 x 300 array, is used to generate all timing control signals. The readout operation is column-wise. Each time a single row is enabled to sense the induced capacitance. All the pixels in the selected row are processed simultaneously by column-wise readout circuits, and the sensed and amplified voltages are hold in every columns. Multiplexing signals are used to selected the hold voltages column by column to an ADC for digital output.

IV. SIMULATION AND EXPERIMENT RESULTS

To readout the experimental LTPS-TFT capacitive sensor array described in section 2, a test readout chip is designed and implemented by using a standard 0.35μm 2P4M CMOS process. The simulation results are shown in fig 13 and fig 14. The simulation of readout control timing is shown in fig 13. The simulation of sensed signal and 4-bit digital outputs are shown in fig 14. The chip layout and photo are shown in fig 15. The chip specifications are listed in table 1.

The layout of prototype print circuit board is shown in fig 17. The PCB is under manufactured. Wire bonding will be used to connect the capacitive sensor chip and the readout chip on PCB to accomplish an experimental
fingerprint acquisition system. The measurement results will be reported in the conference.

V. CONCLUSION

In this paper, a CMOS readout circuit chip is designed and implemented for an experimental LTPS-TFT capacitive fingerprint sensor array chip. A prototype PCB is also designed for integrating both the CMOS readout chip and LTPS-TFT sensor chip to achieve a prototype fingerprint acquisition system. Although the experimental chip has an array size of 30 x 30, the timing control is designated according to grab 10 frames per second in an array size of 300 x 300. The simulation results shows that the readout chip can sense induced capacitance ranged from 0fF to 600fF, and convert to output voltage ranged from 3.93V to 1.7V, respectively.

The paper, there are some improvements made on Gm Amplifier in the future. First, the array is too big, so the stability analysis of Amplifier gain should be executed. Furthermore, Vx voltage is little, so offset Voltage cancel circuit is increased. Therefore, they will avoid the mistake of Gm Amplifier circuit operation.

ACKNOWLEDGMENT

The authors would like to give their thanks for the help from Chip Implementation Center on the chip implementation. The work is supported by Himax Technology, Inc.

REFERENCES