Modeling of a CMOS Active Pixel Image Sensor: Towards Sensor Integration with Microfluidic Devices

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***Abstract*—Recently, microfluidic devices have received considerable attention because of the many potential applications in medicine and environmental monitoring. In such systems, cells and particles suspended in fluids can be manipulated for analysis. Microfluidic systems are projected to develop more complex functions as they integrate electronic/optoelectronic sensors that could monitor the activity within microchannels. This paper presents research work on modeling and simulation of a CMOS Active Pixel Sensor providing some basis for the future integration with microfluidic devices. Computer simulations are carried out demonstrating the functionality of each stage of the sensor and a small pixel array is modeled and simulated incorporating the addressing and reset signals. Results illustrate how the performance of the CMOS active pixel sensor can be adjusted to meet the specifications for scientific applications.**

***Keywords*-CMOS; image sensor; pixel array; active pixel; APS; microfluidics; lab-on-a-chip.**

I. Introduction

In recent years, microtechnology and biomedical research have enabled the development of smaller, bio-compatible and more complex devices designed for a wide range of medical applications. The micro-fabrication processes allow the implementation of not only electronic circuits, but also mechanical and optoelectronical systems on the same silicon die. This capability widely extends the design possibilities when thinking about new devices that help people to diagnose illnesses, develop new drugs and novel biosensors.

Of particular interest is the development of new microdevices that have the capability of performing clinic analysis using very small volumes of corporal fluids or tissues, and even analysis of individual cells [1]. These devices, so-called Laboratory-on-a-Chip (LoC), are promising instruments because of its high throughput and its potential of performing analysis in a wide variety of biological studies, such as DNA extraction, cellular separation and characterization, virus, bacteria and cancer cells detection and testing of new drugs, without relying on significant laboratory infrastructure.

The CMOS technology, which can be used to fabricate LoC accessories, suggest the possibility of implementing a full image-sensing system where not only the image capture is possible but also the chip timing, control and image processing circuitry onto the same silicon die. This brings the possibility of customizing a micro-camera for a particular application such as LoC monitoring [2]. These micro-devices are called Camera-on-a-Chip and are possible thanks to a relatively new image sensor technology called Active Pixel Sensor (APS) that takes advantage of the existing CMOS manufacturing facilities. This possibility of fabrication brings several advantages over the other main imaging technology, the Charge-Coupled Device (CCD), like lower foundry cost, lower power consumption, lower power supply voltages, higher speed and smartness by incorporating on-chip signal processing [3], [4], [5].

Moreover, it has been demonstrated the integration of micro-opto-electronic devices with LoCs, where the optical components are placed directly over the LoCs, so they replace the task done by a microscope in the actual laboratory analysis [1]. These advantages makes the Camera-on-a-Chip the perfect complement for the LoCs to accomplish the objective of fast and low-cost clinical analysis.

In the following sections, the APS architecture is defined and the functionality of its stages are modeled, focusing on the design of each of its elements and taking as the essential criteria, the specifications for microfluidic devices reported in literature [1], [6], [7], [8], such as the pixels fill factor, dynamic range and low-noise performance.

II. Active Pixel Sensor modeling

Figure 1 shows the circuit model of a single active pixel sensor. This model comprises the reset ($\mathrm{M_{RST}}$) and readout circuitry ($\mathrm{M_{SF}}$, $\mathrm{M_{SEL}}$ and $\mathrm{M_{COL}}$). All devices are in-pixel except $\mathrm{M_{COL}}$ which is placed at the bottom of the pixel (or column of pixels). In addition to this, a capacitive load $\mathrm{C_{COL}} = 10\ \mathrm{pF}$ has been included for simulation purposes.

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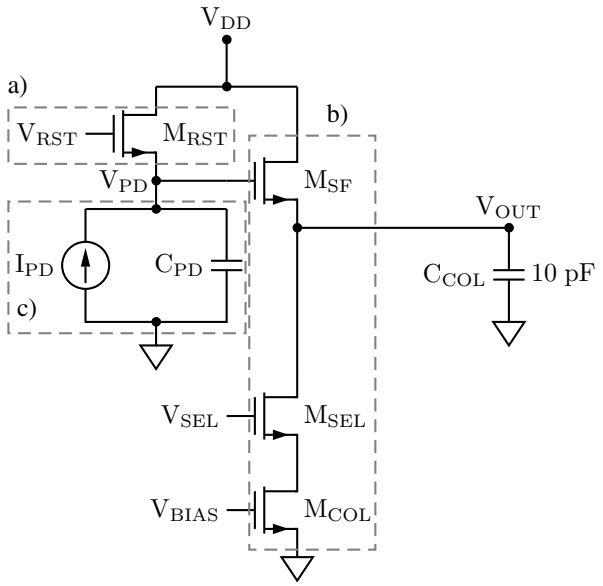

Figure 1. 3T pixel configuration: a) Reset transistor, b) Read-out circuit and c) Photodiode.

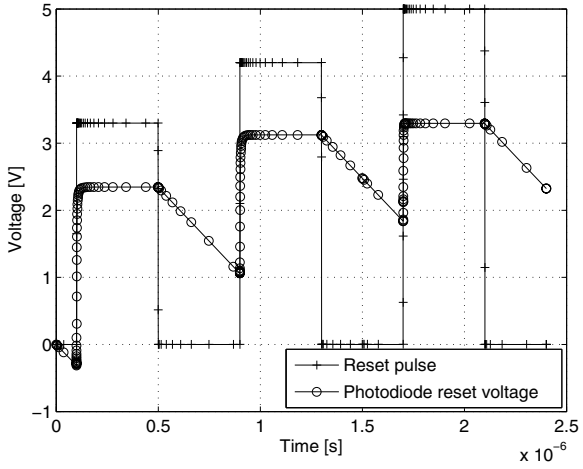

Figure 2. Reset pulse V_{RST} using 3.3 V, 4.2 V and 5 V pulses, and the resulting reset voltage V_{PD_RST}.

A. Reset device

The transistor M_{RST} is used to set the photodiode to a known voltage value through signal V_{RST}. This device was sized to the minimum feature size in order to maximize the pixel's fill factor and to reduce the charge injection to the photosensitive area after reset [3].

Using a reset pulse of $V_{RST} = 3.3$ V on the gate of M_{RST}, the photodiode reset voltage was found to be $V_{PD_RST} = 2.43$V, which means that more than the 26% of the signal range is lost because of the increased threshold voltage of M_{RST}. The threshold voltage of M_{RST} is then $V_{TH\_RST} = V_{RST} - V_{PD\_RST} = 3.3 - 2.43 = 0.87$ V.

Furthermore, through simulation, the threshold voltage of the reset transistor was found to be $V_{TH\_RST} = 0.931$ V under the same conditions; this gives an error of 6.5% for the threshold voltage and an error of 3.7% for the reset voltage of the photodiode which has a value of $V_{PD\_RST} = 2.34$ V on simulation.

One way to recover the voltage loss is boosting the reset pulse to a value above the power supply voltage [3]. An optimal reset pulse was determined to be $V_{RST} \approx 5$ V for $V_{PD\_RST} = 3.3$ V, as shown in Figure 2.

B. Read-out circuit

After the integration time, the remaining photodiode voltage is buffered by the source follower (common-drain) amplifier. Note in Figure 1 that M_{SF} acts as a buffer and M_{COL} as a current sink. Such amplifier has low voltage gain ($\lesssim 1$) and high current gain, which is needed to drive the capacitive load existing at the end of each column of pixels.

The minimum output voltage of the source follower amplifier is determined by the threshold voltage of the buffer device, V_{TH_SF}, since that for lower voltage values, the buffer device is off. On the other hand, the maximum output voltage is considerably lower than V_{DD} because of the body effect, which causes V_{TH_SF} to increase with the output voltage.

A bias voltage of $V_{GS\_COL} = 1$ V was set to determine the size of M_{COL}. The input voltage required by the source follower to operate linearly was determined to be $V_{PD\_MIN} \approx 1$ V.

M_{SF} was set to the minimum size in order to maximize the pixel's fill factor and M_{COL} was designed to sink a low bias current (≈ 1.5 μA) to achieve the widest output voltage range possible, which is related to a reduced noise level. A simulation was performed to determine the optimum size of M_{COL} and results are shown in Figure 3.

Figure 3.a shows that for an input voltage of $V_{IN} \approx 1$ V, the load transistor M_{COL} with an aspect ratio of $W/L = 0.1$ begins to operate in saturation at a lower bias current. For a bigger aspect ratio, the drain current increases and saturation starts at a greater input voltage, so the output voltage range is reduced, as can be seen in Figure 3.b. Also through simulation was observed that for smaller aspect ratios than $W/L = 0.1$, the load transistor area increased substantially and the output voltage range was not significantly augmented, so the optimum feature size for M_{COL} was determined to be $W/L = 0.1$.

From the results shown in Figure 3, it was obtained that applying a boosted pulse to reset the photodiode voltage level and biasing the source follower amplifier with optimum column current found through simulation, the output voltage range of the pixel was $V_{PR} = V_{DD} - V_{PD\_MIN} = 3.3 - 1 = 2.3$ V. This result is

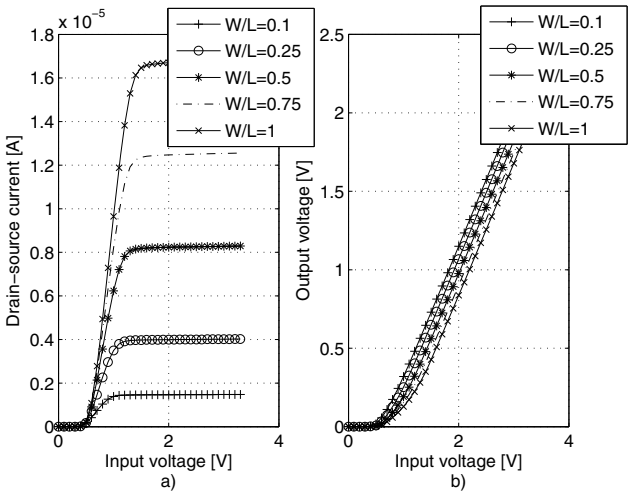

Figure 3. a) Source follower drain current and b) output voltage, for different aspect ratios of $\mathrm{M_{COL}}$.

about the 70% of the photodiode voltage swing or a voltage gain of $0.7\ \mathrm{V/V}$.

C. PN-junction photodiode

For scientific applications of Active Pixel CMOS image sensors, a typical charge capacity in the photodiode is between $\mathrm{N} = 100\ \mathrm{Ke^-}$ and $\mathrm{N} = 1\ \mathrm{Me^-}$ [3], so in this design a value of $\mathrm{N} = 1\ \mathrm{Me^-}$ was chosen. The conversion gain (CG) of the photodiode necessary to achieve such specifications was determined to be

$$\mathrm{CG} = \frac{\mathrm{V_{PD}}}{\mathrm{N}} = \frac{3.3}{1 \times 10^6} = 3.3\ \mu\mathrm{V/e^-}, \tag{1}$$

where $\mathrm{V_{PD}}$ is the photodiode voltage and N is the charge capacity in number of electrons.

The capacitance of the photodiode $\mathrm{C_{PD}}$ is evaluated as follows:

$$\mathrm{C_{PD}} = \frac{\mathrm{q}}{\mathrm{CG}} = \frac{1.602 \times 10^{-19}}{3.3 \times 10^{-6}} \approx 50\ \mathrm{fF}, \tag{2}$$

where q is the charge of the electron.

A simulation was performed to determine the photodiode capacitance performance for different light levels and sampling rates. The test circuit includes the reset transistor ($\mathrm{M_{RST}}$), the calculated capacitance represented by an ideal capacitor and a test current source ($\mathrm{I_{PD}}$) which represents the photo-generated carriers on the depletion region of the photodiode. Figure 4 shows the simulation results for a dark environment which is represented by setting $\mathrm{I_{PD}} = 0\ \mathrm{A}$.

It was obtained that, under dark conditions, a leakage current discharges the photodiode about $1.2\ \mathrm{V}$. The number of electrons accumulated by the leakage effect is

$$\mathrm{N_{dark}} = \frac{3.3 - 2.137}{3.3 \times 10^{-6}} = 350\ \mathrm{Ke^-}, \tag{3}$$

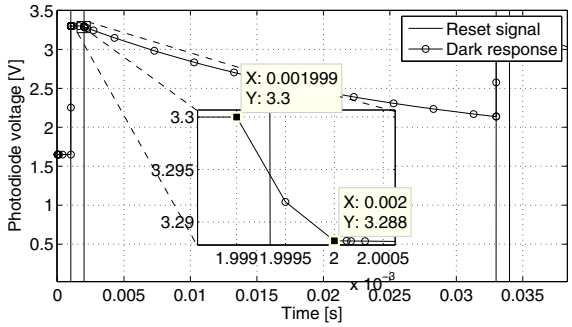

Figure 4. Photodiode response at dark environment at $33\ \mathrm{ms}$ of integration time.

so the dynamic range of the pixel at this sampling rate is

$$\mathrm{DR} = 20 \log\left(\frac{1 \times 10^6}{350 \times 10^3}\right) = 9\ \mathrm{dB}. \tag{4}$$

The charge distribution also affects the pixel performance by decreasing the pixel voltage when the reset device turns off. The inset in Figure 4 shows a close up at the time when $\mathrm{M_{RST}}$ turns off. It can be seen that the remaining electrons in the channel discharges the photodiode capacitance about $12\ \mathrm{mV}$.

At the same lighting conditions, it is expected that the dynamic range increases with the sampling rate. This is because for shorter integration times, the photodiode is less time exposed to the leakage current. The current required to completely discharge the photodiode for different sampling rates was also determined using sampling rates of 30 and $3,000$ frames per second. The width of the reset pulse in both cases is 30% of the total integration time and a boosted reset voltage $\mathrm{V_{RST}} = 5\ \mathrm{V}$ was set. Simulation results are shown in Figure 5.

Simulation results on Figure 5 show that the maximum photodiode voltage swing ($\mathrm{V_{PD}} = 3.3\ \mathrm{V}$) was reached in both cases. The current required to discharge the photodiode capacitance, $\mathrm{C_{PD}}$, in a) is $\mathrm{I_{PD}} \approx 6\ \mathrm{pA}$ and in b) is $\mathrm{I_{PD}} \approx 550\ \mathrm{pA}$. According to simulation, it can be noticed that if the integration time is shorter, a higher current is necessary to discharge the same capacitance.

In a more realistic scenario, for a charge pocket of $1\ \mathrm{Me^-}$, the pixel pitch using a standard $0.35\ \mu\mathrm{m}$ technology is about $17\ \mu\mathrm{m}$, which gives a pixel's fill factor between 15% and 45%, depending on the photodiode architecture and design rules of each specific foundry [3]. The total junction capacitance of the photodiode as a function of the area and perimeter is given by

$$\mathrm{C_{PD}} = \frac{\mathrm{C_J} \times \mathrm{A}}{\left(1 - \frac{\mathrm{V_{PD}}}{\Phi_\mathrm{B}}\right)^{\mathrm{MJ}}} + \frac{\mathrm{C_{JSW}} \times \mathrm{P}}{\left(1 - \frac{\mathrm{V_{PD}}}{\Phi_\mathrm{BSW}}\right)^{\mathrm{MJSW}}}, \tag{5}$$

where $\mathrm{C_J}$ and $\mathrm{C_{JSW}}$ are the unit zero-bias area and peripheral junction capacitances, A and P are the area and

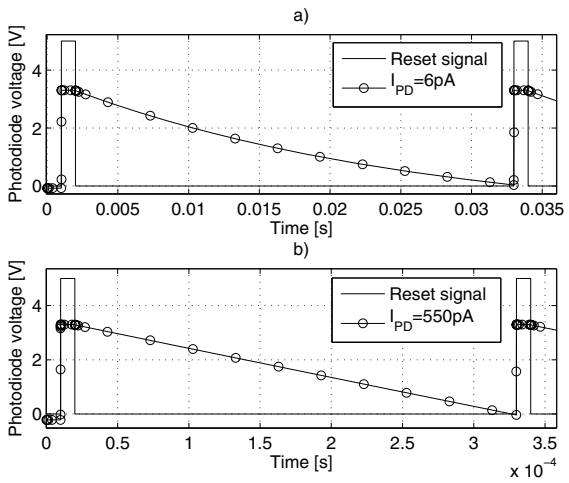

Figure 5. Full discharge of the 50 fF ideal capacitance at a) 30 frames per second and b) 3000 frames per second.

Table I
PHYSICAL PARAMETERS OF $\mathrm{M_{RST}}$ FOR SIMULATION OF A PHOTODIODE WITH A PN-JUNCTION CAPACITANCE, $\mathrm{C_{PD}} = 58.44$ fF.

Physical parameter	Value [m]
Channel width	0.4×10^{-6}
Channel lenght	0.35×10^{-6}
Drain area	0.18×10^{-12}
Drain perimeter	1.7×10^{-6}
Source area	100×10^{-12}
Source perimeter	40×10^{-6}

perimeter of the photodiode, respectively; Φ_{B} and Φ_{BSW} are the built-in potentials of area and side-wall junctions, $\mathrm{M_J}$ and $\mathrm{M_{JSW}}$ are the junction grading coefficients of area and sidewall junctions and $\mathrm{V_{PD}}$ is the photodiode junction voltage.

Equation (5) was solved for an square-shaped photodiode and it was obtained that for an area $\mathrm{A} = 100\ \mu\mathrm{m}^2$ and a perimeter $\mathrm{P} = 40\ \mu\mathrm{m}$, the capacitance of the photodiode is $\mathrm{C_{PD}} = 58.44$ fF, which represents a 16.8% higher capacitance than the defined for a $1\ \mathrm{Me}^-$ charge pocket using an ideal capacitor. For simulation purposes, the source area and perimeter of $\mathrm{M_{RST}}$ were adjusted to act as a pn-junction photodiode. Table I shows the physical parameters for $\mathrm{M_{RST}}$ that were set for simulation.

In the same way than in section II-C, a test current $\mathrm{I_{PD}} = 0$ A was set in order to obtain the dark current and charge distribution effects on the pn-junction photodiode. The results shows that the number of electrons that discharges the photodiode capacitance in the absence of light is $\mathrm{N_{dark}} = \frac{3.3-2.252}{3.3\times10^{-6}} = 317\ \mathrm{Ke}^-$ and the dynamic range of the pixel at 30 frames per second is $\mathrm{DR} = 20\log\left(\frac{1\times10^6}{317\times10^3}\right) = 10$ dB, and therefore, a slightly decrease in the number of accumulated electrons was appreciated due to the dark current when compared to the ideal capacitor and the dynamic range increases 1 dB. Moreover, due to the charge distribution effect, the photodiode voltage in this case is discharged about $10\ \mathrm{mV}$.

Table II
SIMULATION RESULTS AND PERCENTAGE ERROR OF THE FULL-DISCHARGE CURRENT OF THE IDEAL AND THE PN-JUNCTION CAPACITANCES

Samples [fps]	Ideal [pA]	PN-junction [pA]	Error [%]
3	6	7.5	25
30	55	70	27.3
300	550	700	27.3
3000	5500	7000	27.3

Table III
SIMULATION RESULTS AND PERCENTAGE ERROR OF THE FULL-DISCHARGE CURRENT OF THE IDEAL AND THE PN-JUNCTION CAPACITANCES FOR THE SAME CAPACITANCE VALUES

Samples [fps]	Ideal [pA]	PN-junction [pA]	Error [%]
3	7	7.5	7.1
30	65	70	7.7
300	650	700	7.7
3000	6500	7000	7.7

A more significant increase in the dynamic range is described when the sampling rate is increased. For instance, at 300 fps, the voltage reduction due to the dark current is $0.170\ \mathrm{V}$ which means a reduction of 15% when compared to the ideal capacitance; the dynamic range this time is $25.8\ \mathrm{dB}$, which represents a increase of 5% when compared to the ideal 50 fF capacitance.

In addition to this, the current necessary to completely discharge the pn-junction capacitance for different sampling rates was also obtained. As expected, more current is needed in this case due to the increased capacitance of the photodiode. Table II shows the current values for a full discharge of both capacitances, the ideal and the pn-junction, for different sampling rates. Also, the percent error between these two cases is showed. As can be seen, the maximum error is about 27.3% and occurs at the higher sampling rates.

The ideal capacitor was then fixed to the 58.44 fF determined through the physical parameters of the photodiode, so the charge capacity of the ideal capacitor is the same as for the pn-junction photodiode. A new simulation was set in order to determine the percentage error for a full discharge using the same capacitance values. This time, the percentage error was reduced considerably, as shown in Table III.

The maximum percent error in this case is 7.7% which is considerably lower than the 27.3% of the 50 fF capacitance.

III. PIXEL ARRAY SIMULATION

In order to validate the design, a pixel array was simulated using the APS modeled on section II. The corresponding control signals for vertical and horizontal accessing were included. The pixels were distributed in four rows and five columns (4×5) and each pixel in a row shares the reset and

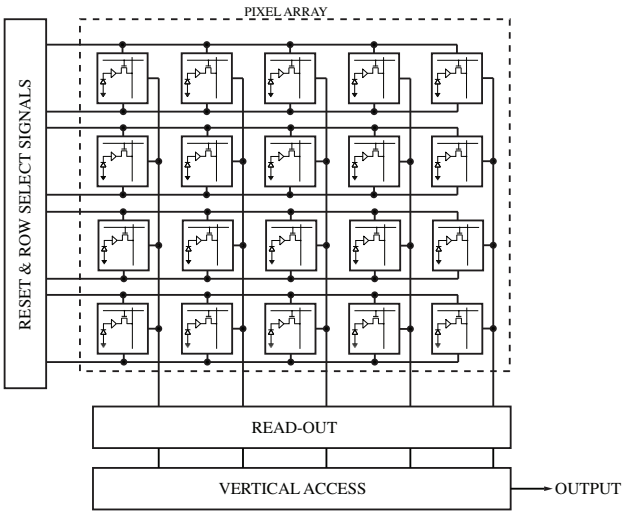

Figure 6. Active pixel sensor array including horizontal, vertical and read-out circuitry.

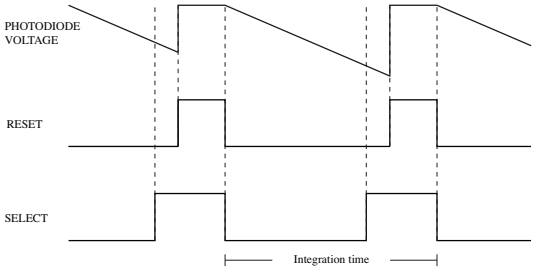

Figure 7. Timing signals for accessing and read-out pixels.

select signals, so the read-out was performed one row at a time. This arrangement is depicted in Figure 6.

At the bottom of each column was placed an NMOS device that acts as the active load of the buffer transistor of each pixel. Such load was biased with a voltage source in order to set a determined drain current and a capacitive load of 5 fF was connected at the output each column (read-out circuitry).

A. Pixel array setup

Each pixel in the array has a pn-junction photodiode with a capacitance of 58.44 fF, as designed in section II-C, and its corresponding reset, buffer and select transistors (see Figure 1).

The timing signals of the pixel array are shown in Figure 7. As can be seen, a reset pulse is applied to the photodiode to set the voltage across its terminals to a known value. Once the reset device is turned off, the integration time starts and it lasts until a new reset pulse is applied. During this period, the photodiode is floated and electron-hole pairs are generated on the depletion region of the junction, depending on the light intensity and wavelength of the photons. The select signal is applied just a moment before and during the reset pulse, so the voltage variation on that time lapse can be amplified, measured and sampled.

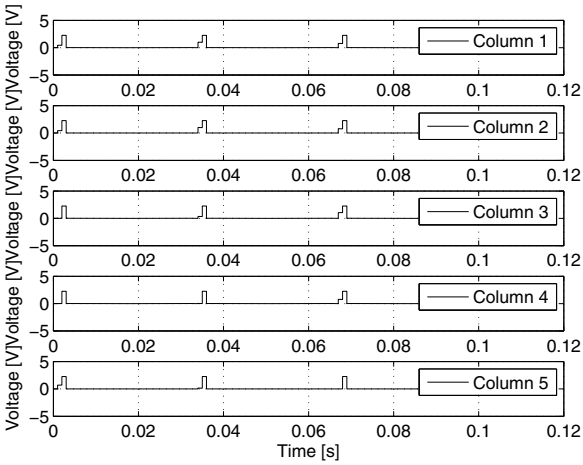

Figure 8. Output signals of the pixel array.

On the array there were implemented four reset signals, one per each row. The select signals were set on the same way so the read-out could be done row by row. A set 20 current sources emulated the impinging photons on each pixel. The values of each current source were chosen randomly.

B. Results

The voltage signals of each column of the array are shown in Figure 8. The reading is actually done in parallel for each column, so at 1 ms, there are five pulses, one for each column, and all those pulses are read at the same time. Then, at 3 ms, the second reading takes places and so on until the four rows are read.

IV. Conclusions

This paper has presented the modeling and simulation of both, a single active pixel sensor and a small array of pixels. Models were based on a standard 0.35 μm CMOS process.

In the single pixel analysis, it was observed that both, the charge distribution and the dark current considerably reduce the dynamic range of the sensor, so it is important to choose the optimum size of the reset transistor in order to minimize both effects. It was found that the charge distribution effect is minimum when a minimum feature size for $\mathrm{M_{RST}}$ is used. Also, if the channel length of the reset transistor is increased, a small reduction on the dark current is obtained.

A $1\,\mathrm{Me^-}$ charge pocket was defined for an ideal pn-junction photodiode and the calculated capacitance was 50 fF. Using the technology design rules, it was implemented a square-shaped photodiode presenting a capacitance of 58.44 fF.

Concerning the photodiode discharge due to dark current, the ideal photodiode presented 35% at $33\ \mathrm{ms}$ and the real photodiode presented 32% at the same sampling rate. The charge distribution effect was 3% for the real photodiode while 3.6% for the ideal photodiode. The real photodiode presented $1\ \mathrm{dB}$ wider dynamic range. This suggests that maximizing the area and/or perimeter of the photodiode and hence the charge capacity, increases the dynamic range.

In another experiment, the ideal and real photodiodes were fixed to have the same capacitance of $58.44\ \mathrm{fF}$, so the charge capacity is equal for both devices. It was observed that the error for the full-discharge current was considerably reduced.

A 4×5 pixel array was simulated using the obtained model for a real pixel and incorporating the control signals with voltage sources. A set of current sources emulated the impinging photons on the pixels where the values of the sources were chosen randomly. The resulting output signals show the functionality of the array, demonstrating that the model is capable of being integrated to form an array of pixels.

It is expected that the results in the modeling and simulations presented in this paper will help in the design of new specific image sensors that will be integrated with microfluidic devices.

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