A Boundary Scan Circuit with Time-to-Digital Converter for Delay Testing

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Abstract—This paper presents a design-for-testability method for detecting delay faults. In order to observe the effect of small delay defects, we present modified boundary scan cells which a time-to-digital converter (TDC) is embedded. In our boundary scan cells, flip-flops are utilized for both making a scan path and capturing circuit response. The architecture of the boundary scan design is proposed to detect delay from the other cores or chips or its interconnects. The basic operation of the design is evaluated by simulation and by experimental ICs. Experimental results show that the measurement of the transition delay can be achieved by the boundary scan design with the time-to-digital converter.

Keywords—delay testing, boundary scan, time-to-digital converter,

I. INTRODUCTION

In recent deep sub-micron (DSM) ICs, some of the faults do not behave like conventional stuck-at fault model and are hard to be detected [1], [2]. Since most of opens and shorts result in circuit delay, detecting delay faults is important for testing DSM ICs. The test patterns for detecting delay faults are generated such that the fault is propagated through a critical path. However, it is difficult to make such patterns for every target faults. Small delay defects may escape if the critical path is not used in test pattern generation.

Moreover, the size of delay caused by a defect may differ depends on input pattern especially when an open defect occurs since the voltage at the floating wire is unstable and is affected by its adjacent lines [3]–[5].

Several test methods to detect small delay faults have been proposed. In [6], [7] to detect timing failure caused by small delay faults, circuits are tested using multiple clock frequencies, which are higher than the normal clock. In [8], a delay sensor circuit using a sawtooth generator and a comparator has been proposed for testing delay faults. In [9], a ring-oscillator based on-chip path delay measurement technique has been proposed. In [10], a boundary scan cell for testing interconnects has been proposed. In the method, the multiple transitions are generated on interconnects by the enhanced boundary-scan architecture to detect signal integrity violations.

Several methods have been proposed to measure the delay using time-to-digital converters as on-chip jitter measurement circuits [11]. In [12]–[14], delay measurement circuit using time-to-digital converter has been proposed.

We propose the boundary scan cells that can form a time-to-digital converter to observe the delay caused by defects. To reduce the area overhead, scan flip-flops in boundary scan cells are also utilized for measuring delay. The delay line in the time-to-digital converter is designed such that it can form a loop and is used for testing multiple inputs. In our method, delay of incoming transitions from the other cores or chips is captured at the boundary scan cells. The operations of new boundary scan cells are examined by both simulation and experimental chips.

The rest of this paper is organized as follows: Section II describes the time-to-digital converter used in our design and Section III introduces the proposed boundary scan architecture in which a time-to-digital converter is embedded. Section IV shows some experimental results obtained both by simulation and by observing the experimental ICs. Section V concludes the paper.

II. DELAY FAULT DETECTION USING TIME-TO-DIGITAL CONVERTER

A time-to-digital converter is utilized for measuring delay or jitter [11]–[14]. Figure 1 shows an example of a time-to-digital converter (TDC) used in our design. The delay of an incoming transition from another core or chip is measured using a time-to-digital converter. The incoming transition is delayed by AND gates and is captured at flip-flops through POUT. If the number of gates on a delay line is large enough, the delay of the transition can be observed by the difference of the captured value at the flip-flops. In case of a rising transition, there exists POUTj such that the captured values are 1 at from POUT0 to POUTj−1 and 0 at POUTj to POUTn. To measure the delay more precisely, Vernier delay line TDC that has two delay lines is utilized [11]–[14]. However, in our method a simple TDC like Fig. 1 is used to combine with boundary scan cells as described in Section III.

The core with TDC is used in our method to detect delay faults occurred in the other cores connected to the core or at the interconnects between the cores. In testing, setting THRUN = 1 and the incoming signal transition is captured at the scan flip-flops in the scan path. If a delay fault
occurred in a circuit, the delay may be observed through scan path. If we put \( n \) delay elements in a delay line, \( n \) more logic values can be observed at different timing using a time-to-digital converter as shown in Fig. 2. Let \( T_{clk} \) be the clock period, \( d \) be the delay of a gate used as a delay element, and \( n \) be the number of flip-flop in the scan path. Using a TDC, we can capture a signal transition \( n \) times from \( t = T_{clk} - n \times d \) to \( t = T_{clk} \). The logic value captured at \( j \)-th flip-flop in the scan path is denoted as \( v_i^j \), where \( i \) denotes the \( i \)-th input. The expected value of \( v_i^j \) is \( \{0, 1, x\} \), which is calculated by simulation or is determined by good die in consideration of glitches or variation in the transition. We can measure how fast the transition arrived at the chip input and can measure the slack between the clock and the signal using a TDC.

III. BOUNDARY SCAN CELLS WITH TIME-TO-DIGITAL CONVERTER

To observe input transitions for each input with less hardware, we propose modified boundary scan cells in which a time-to-digital converter is embedded.

Figure 3 shows our boundary scan cells with time-to-digital converter called TDCBS. The TDCBS cells have four modes: One is NORMAL mode in which the output of the previous core is fed into inputs of the core. In THRU mode, the output transition of the previous core is propagated into the delay line and is captured at each flip-flop. In SHIFT mode, the captured response is shifted out to the SCANOUT terminal. The scan output SOUT is compared with the expected values to find the outliers with large delay.

SHIFT mode is also used for a scan shift operation as in the conventional boundary scan. TEST mode is used for providing the input pattern from scan cells into the core.

Table I shows the control signals for selecting modes of TDCBS among NORMAL, TEST, SHIFT, THRU. Setting NORMAL/TEST = 1, the circuit is in test mode of a conventional boundary scan that provides inputs from scan FFs. The THRUSWCONT block provides the control signal CONT[\( i \)] for each input \( i \) to select which input transitions to be observed. It also provides the signal LOOP to connect the terminals of the delay line to form a loop. Setting SHIFT/THRU = 1, the selected inputs are connected to the delay line that consists of an XOR and an AND gates.

The delay line make a loop by setting LOOP=1 to observe the delay of the input transition even if the input is connected to near the end of the delay line.

Figure 4 shows an example of a delay line configured for detecting small delay faults. In this example, the output transition from output OUT[1] is observed. The THRUSWCONT block provides the control signals CONT[1]=1, CONT[\( j \)]=0 (\( j \neq 1 \)), and LOOP=1 to observe OUT[1]. The input transition goes through XORs exout1, exout2, ..., exoutr and an AND gate, and then reach exout0.

Figure 5 shows the operation for testing in THRU mode. The transition delay can be observed by the following
procedure.
(1) Test input is applied for the previous core.
(2) Set LOOP=1 to configure a ring delay line.
(3) Capture the delayed response at each flip-flop. After
that, set LOOP=0 and all CONT to be 0.
(4) Observe the captured response to the SCANOUT using
scan shift by setting NORMAL/TEST = 1 and SHIFT/THRU
= 0.

The expected value of the \( k \)-th scan flip-flop, denoted as \( V^k \), is estimated by the following equation on the
assumption that the data delay of the AND gate and the
XOR gate in TDCBS cells are the same:

\[
V^k = \sum_{i} c_i \cdot v_i^2 + \sum_{i} c_i \cdot v_i^3 + \sum_{i} c_i \cdot v_i^4 + \sum_{i} c_i \cdot v_i^5 + \ldots + \sum_{i} c_i \cdot v_i^{k-1}
\]

where \( v_i^2 \) is the expected value of \( i \)-th input (OUT\([i]\) in
Fig. 4) at time \( t = T_{clk} - j \times d \) as defined in Section II; \( c_k \)
is the same as CONT\([k]\) that is set to 1 if the \( k \)-th output
is selected to be observed and is set to 0 for masking the
input.

The calculated \( V_k \) may not match exactly with the
measurements of the real chips since there exists variations
in delay of the gates on the delay line and also the flip-
flops do not capture the input correctly when it violates
setup/hold time [14]. Hence some margin should be set for
each transition paths to be observed in the measurement.
Moreover, when two or more outputs are selected by setting
CONT=1, some hazard may occur in a delay line. If a
transition only occurs in one of the selected output, we can
observe multiple outputs regardless of such hazard.

When only one input \( k \) is selected to be observed (\( c_k = 1 \) and \( c_i = 0 \) for all \( i \neq k \)), the expected values are the
following:

\[
V_k = v_k^2
\]
\[
V_i = v_k^{2+i-k}, \quad i = k + 1, \ldots, n.
\]
\[
V_j = v_k^{3+j-n}, \quad j = 0, \ldots, k-1.
\]

Since there exist two gates between OUT\([k]\) and \( FF_k \), the
expected value of \( FF_k \) is \( v_k^2 \). All inputs except \( k \) are masked.
Therefore the transition delay can be measured similar to
Fig. 1. When \( n \times d \) is small compared to the clock period, the
oscillation may occur in the delay line before capturing the
responses. In such a case, additional delay elements should
be placed in the delay line. If we observe the transition at
these gates, additional flip-flops are also needed like \( FF_L \),
which is connected from the AND gate that controls the loop
of the delay line.

The area overhead of the TDCBS compared to the con-
ventional boundary scan method consists of an AND gate,
a MUX gate, and an XOR gate for each flip-flop, one
AND gate to control the loop of a delay line, a controller
THRUSWCONT, and additional flip-flops to extend a delay
line if needed. The additional power consumption only
occurred in a delay line since the input transitions are not
propagated to a circuit by setting NORMAL/TEST to 0
during delay measurement.

Two or more inputs can be connected to the delay line if
they have no transition for the test pattern. Even if transitions
occurred at some inputs, they can be connected to the delay
line if the many stable logic value can be expected at \( V^K \).
By connecting many inputs at a time we can reduce test time
and may detect unexpected faults.
IV. EXPERIMENTAL EVALUATION

A. Simulation results of TDC

First, we designed a circuit to measure the signal transition using the delay measurement circuit as shown in Fig. 1. Figure 6 shows the design of our experimental test chip. It includes two cores to observe the transition delay occurred in and between the cores. In Core#1, 128-AND chain is placed to produce delay. The transition delay of the AND chain is almost 14.0 [nsec]. Core#2 has a time-to-digital converter and a delay line as shown in Fig. 1.

Figure 7 shows a simulation waveform obtained for the circuit shown in Fig. 6. It can be seen that the transition from H to L is captured near the flip-flops FF6, FF7, FF8 and propagated to SOUT terminal using scan chain. It can be found from the SOUT waveform that the position of the flip-flop that captured the transition is the seventh or eighth. In this case, the transition reaches the core earlier than the clock period by about 7 times of the gate delay.

When the transition delay increases, the transition occurred at SOUT will be late. Figure 8 shows the waveforms obtained for the circuit with more delay. In this simulation, four additional inverter gates are placed after the AND chain in Core#1. It can be seen that the transition was captured by the flip-flop nearer to the input of Core#2. The SOUT waveform remained H during about 11 clock cycles.

B. Simulation results of TDCBS

Next, simulations are performed for the boundary scan cells with time-to-digital converter (TDCBS). Figure 9 shows the circuit used in our simulation. In Core#1, sixteen 16-AND chains are connected serially. Each output of AND chains is output to the Core#2 and connected to each TDCBS as shown in the figure. Figure 10 shows some of the waveforms obtained by the simulation. The transition from L to H is applied to Core#1 at the first clock and is directly fed into the AND chains. Then, the flip-flops in Core#2 capture the input at the second clock. The captured value is observed at the third clock. Although flip-flops are connected to make a scan chain in the proposed TDCBS, the simulation is performed such that the captured values were output in parallel for simplicity.

In the first two period, the output from OUT[0] was observed using TDCBSs. The first transition is applied to Core#1 with setting LOOP=0 and CONT[0]=1. Hence the transition delay of 16-AND chain is about 1.6[nsec] and clock period is set to 20[nsec] in this simulation, the transition reached much earlier than the clock period. All flip-flops except $FF_L$ captured H value. The second transition is applied with setting LOOP=1 and CONT[0]=1 at the fourth clock. In this case, the delay line makes a loop and hence
the transition was propagated through the loop several times before the flip-flops captured the values.

The same transitions were applied for the cases that \text{CONT}[9]=1, \text{CONT}[10]=1, \text{CONT}[11]=1, and \text{CONT}[12]=1. In these cases, the transition was not propagated to \text{V}[16] since \text{LOOP} is set to 0. For \text{CONT}[11]=1, the transition reached \text{OUT}[11] in 19.2[nsec]. The logic H value was observed only at \text{V}[11] since the transition delay and the clock period are almost the same. For \text{CONT}[12]=1, the transition can not reach \text{OUT}[12] before the clock period, therefore all flip-flops can not capture the transition. If the delay fault occurred at Core#1 or on the interconnect, the captured value of flip-flops varies.

C. TDC measurement results for experimental ICs

The circuit shown in Fig. 6 is designed and fabricated in 0.18\mu m CMOS technology to observe the variation of the delay. The single transition from H to L is applied to the input of AND chain and observed at the time-to-digital converter.

Table II shows the experimental results. The delay of the circuit is measured using multiple clock cycles between 12.8 - 14.0 nsec. In the table, the number of flip-flops that capture the initial value of the transition is shown for each clock cycle and for each chip. The number equals to 0 when all captured value are L, which means the transition reaches faster than the clock even after propagating sixteen more AND gates than its normal path. The number equals to 16 when all captured value are H, which means the transition can not reaches the flip-flops within the clock period.

In the experimental results, when clock period is set to 13.4[nsec], the variability of transition delay among the ICs can be well observed. It is not necessary to apply multiple clock cycles using the boundary scan method since each flip-flop capture the transition delayed by the delay elements and it is the same as clock period is delayed for the flip-flop. In this TDC design, sixteen flip-flops capture the input transition with different additional delay. Using the TDCBS, two or more input transitions can be captured simultaneously if the transitions of these inputs can not mask the faulty effects each other. However, test patterns must be selected carefully to observe multiple transitions. If no transition occurred at some inputs, those can be connected to the delay line in order to detect some unexpected faults.

Figure 9. An example circuit using TDCBS

Figure 10. Simulation waveform of TDCBS
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V. Conclusion

In this paper, the testability design for detecting delay faults are proposed. A boundary scan cell is modified to form a time-to-digital converter in order to measure the transition delay of the other core and the interconnects. The experimental IC including the boundary scan cells with time-to-digital converter as shown in Fig. 3 has been designed and is currently in the fabrication. Although the proposed method has the ability to test two or more paths simultaneously, the condition of testing multiple paths should be considered. Test pattern generation for TDCBS are also still left as a future work.

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References


