Excess Loop Delay Effects in Continuous-Time Delta-Sigma Modulators and the Compensation Solution

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Abstract

In this paper, we show that excess loop delay seriously degrades the performance of continuous-time delta-sigma modulators (ΔΣM’s). It is then demonstrated in theory that the effect can be alleviated by tuning the feedback digital-to-analog converter pulse-shaping coefficients.

I. Introduction

The rapid development of wireless digital radio systems has led to a great effort to design high resolution and high speed analog-to-digital (A/D) converters. ΔΣ modulators including both lowpass modulators [1] and bandpass modulators [2] are the preferred architecture for high resolution A/D converters. A ΔΣ modulator can be implemented by designing the loop integrator/resonator either in the discrete-time domain such as with switched-capacitor filters [2] or in the continuous-time domain such as with RC [3], transconductor-C [4] and LC filters [5]. Continuous-time modulators are much faster [3] and provide anti-alias filtering [4]. Several continuous-time ΔΣ modulators with sampling rate in the GHz range have been reported recently to extend the application to RF frequencies [3] [6] [7]. It is known, however, that continuous-time ΔΣ modulators suffer from performance degradation due to nonidealities such as excess loop delay and clock jitter in the delta-sigma modulator loop.

In this paper, we first address loop filter transfer function design for continuous-time ΔΣ modulators. The effect of excess loop delay on the performance of continuous-time ΔΣ modulators is then discussed. Thereafter, a solution is proposed that compensates the excess loop delay effect by adjusting the digital-to-analog converter (DAC) pulse-shaping coefficients. Detailed analysis and simulation results are provided.

II. Loop Filter Transfer Function Design

A continuous-time ΔΣ modulator is internally a discrete-time system since there is a sampler inside the loop as shown in Fig. 1. This makes the loop transfer function from the output of the quantizer back to its input have an exact equivalent z-domain transfer function as illustrated in the figure, i.e., the pulse invariant transformation [4]

\[ Z^{-1}[\hat{A}(z)] = L^{-1}[DAC(s) \cdot A(s)]|_{s = nT} \] (1)

where \( DAC(s) = \frac{1 - e^{-spT}}{sp} \) is the zero-order-hold pulse transfer function of the DAC. The value of \( p \) determines the DAC pulse shape such as return-to-zero (RZ, \( p = 1/2 \)) and non-return-to-zero (NRZ, \( p = 1 \)). From the equivalent relationship, we can have the following equation to obtain mapping relations between s-domain and z-domain functions

\[ \hat{A}(z) = z^{-1} \sum_{\text{poles of } A(\lambda)} \frac{\text{residues of } A(\lambda)e^{\frac{\lambda T}{z}}(1-e^{-\lambda p T})}{\lambda (1-e^{\frac{\lambda T - 1}{z}})} \] (2)

where \( z^{-1} \) accounts for the fact that pulse invariant transformation absorbs one clock delay for causality.

There are two approaches described below for designing continuous-time ΔΣM’s.

An approach is that one starts a design from a discrete-time prototype loop transfer function \( \hat{A}(z) \) that meets the required specifications, and then transforms it to the continuous-time equivalent. A design example using this approach in [4] is a bandpass ΔΣM implemented using transconductor-C filters. The transfer function for the second-order and fourth-order ΔΣM’s are

\[ A(s) = \frac{(b_1 s + b_0)}{(s^2 + \omega_0^2)} \] (3)

Fig. 1. Block diagram of continuous-time ΔΣM’s.
and
\[
A(s) = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{(s^2 + \omega_0^2)^2}
\] (4)
respectively.

Another approach is that one starts a design from some simple function blocks. A general continuous-time \(\Delta\Sigma\) modulator shown in Fig. 2 can be formed by a cascade of a functional block \(F(s)\), where the functional block is an integrator for lowpass (LP) modulators and a resonator for bandpass (BP) modulators. The equivalent discrete-time domain transfer function using the \(Z\)-transform is
\[
\hat{A}_i(z) = \sum_{i=1}^{l} k_i \cdot Z^{-1} \left[ DAC(s) \cdot F^i(s) \right] |_{s=nT}
\] (5)
where \(l\) is the number of functional blocks in cascade, and \(k_i\) \((i = 1, 2, ..., l)\) are the DAC pulse-shaping coefficients. The pulse-shaping coefficients are calculated by equating \(\hat{A}_i(z)\) to the desired discrete-time prototype transfer function \(A_i(z)\). The functional block for lowpass modulators can be designed as a first-order integrator which has the transfer function \(1/s\), and for bandpass modulators it can be designed as an LC resonator which has the transfer function \(\omega_0 s/(s^2 + \omega_0^2)\).

![Fig. 2. A general topology of continuous-time \(\Delta\Sigma\)M's based on cascaded architecture.](image)

**III. Performance Degradation Due to Excess Loop Delay**

The building blocks in a \(\Delta\Sigma\) modulator loop including the comparator, the D flip-flops and the DAC's all have propagation delay. Therefore, a practical continuous-time \(\Delta\Sigma\) modulator contains an amount of excess loop delay that can be modeled as \(\delta T\), where \(0 < \delta \leq 1\).

With the unwanted excess loop delay in the delta-sigma modulator, the discrete-time domain loop transfer function moves away from the desired discrete-time delta-sigma prototype loop transfer function since the modulator pulse response at the sampling instants is changed. The actual realized discrete-time loop transfer functions shown below can be obtained from the modified \(Z\)-transform with \(\delta\) replaced by \((1 - m)\) \([8]\).

For the first-order lowpass \(\Delta\Sigma\) modulators
\[
\hat{A}_{1lp}(z, m) = Z^{-1} \left[ \left( z^{-1} - \frac{1}{z^{-1}} \right) \right]
\]
\[
= z^{-1} + \left( 1 - m \right) z^{-1}
\] (6)
and for the second-order lowpass \(\Delta\Sigma\) modulators
\[
\hat{A}_{2lp}(z, m) = Z^{-1} \left[ \left( \frac{2z^{-1} - z^{-2}}{1 - z^{-1}} \right) \right]
\]
\[
= z^{-2} + \left( 2 - 3m \right) z^{-1} + \left( m - 1 \right) z^{-2}
\] (7)

For the second-order bandpass \(\Delta\Sigma\) modulators
\[
\hat{A}_{2bp}(z, m) = Z^{-1} \left[ \left( \frac{z^{-2}}{1 + z^{-2}} \right) \right]
\]
\[
= z^{-1} \left( z^{-1} \sin \left( \frac{m\pi}{2} \right) + z^{-2} \sin \left( \frac{(1-m)\pi}{2} \right) \right)
\]
\[
= \frac{1 + z^{-2}}{1 + z^{-2}}
\] (8)

and for the fourth-order bandpass \(\Delta\Sigma\) modulators
\[
\hat{A}_{4bp}(z, m) = Z^{-1} \left[ \left( \frac{z^{-2} + z^{-2}}{1 + z^{-2}} \right) \right]
\]
\[
= z^{-1} \left( a_1z^{-1} + a_2z^{-2} + a_3z^{-3} + a_4z^{-4} \right)
\]
\[
= \frac{1 + z^{-2}}{1 + z^{-2}}
\] (9)

where
\[
a_1 = \frac{1}{2}(3 + m) \sin \left( \frac{m\pi}{2} \right)
\]
\[
a_2 = \frac{1}{2}(1 + m) \left[ \cos \left( \frac{m\pi}{2} \right) + 3 \sin \left( \frac{(1-m)\pi}{2} \right) \right]
\]
\[
a_3 = \frac{1}{2}(1 + m) \sin \left( \frac{m\pi}{2} \right)
\]
\[
a_4 = -\frac{1}{2}(1 - m) \cos \left( \frac{m\pi}{2} \right) - 3 \sin \left( \frac{(1-m)\pi}{2} \right)
\]

From Eqs. (6), (7), (8) and (9), we can see that the excess delay in the loop changes the numerator of the resultant equivalent discrete-time loop transfer function and therefore affects the noise shaping transfer function. The order of the feedback open loop is increased by one. Therefore, the actual noise transfer function for a continuous-time modulator would have a higher order than the one that was designed since the feedback open-
loop is never delay free. Fig. 3 plots the pole-zero loci of the actual realized noise transfer functions for these modulators based on the above equations. It shows how the poles move from the origin with an increment of excess loop delay in 0.05T (5% period) steps. One pole will move out of the unit circle after a certain excess loop delay for the second-order lowpass (38%), second-order bandpass (58%) and fourth-order bandpass (22%) modulators. This means that excess loop delay may eventually make continuous-time ΔΣ modulators unstable. All noise transfer function zeros are still on the unit circle with one more added to the origin. We can, therefore, expect that the signal-to-noise ratio will not degrade significantly up to a certain excess loop delay.

Fig. 4 gives s-domain simulated plots of signal-to-noise-ratio (SNR) loss versus the percentage of excess loop delay compared to a sampling clock period T for a second-order continuous-time BPΔΣM and a fourth-order continuous-time BPΔΣM. For a fourth-order BPΔΣM, a 20% excess delay is obviously serious. For a system clocking at 3.6Ghz in order to convert a 900MHz carrier, a 20% excess delay is only about 56ps.

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(a) First-order lowpass
(b) Second-order lowpass
(c) Second-order bandpass
(d) Fourth-order bandpass
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Fig. 3. Pole-zero locus diagrams of continuous-time ΔΣM's with excess loop delay.

Fig. 4 also shows that a fourth-order ΔΣM with 25% delay is still stable, which means that there is a disagreement between continuous-time domain simulation and the mathematical analysis. This disagreement also appeared in the continuous-time domain simulation of second-order lowpass modulators. The reason is that the quantizer gain is not always 1 since it is input signal dependent. Fig. 5 gives pole-zero locus plots for a second-order lowpass and a fourth-order bandpass modulators with quantizer gain varying from 1.2 to 0.4 and excess delay in 5% period steps. It shows that smaller quantizer gain would make the system more stable in the presence of large delay.

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Fig. 4. SNR loss vs. excess loop delay for BPΔΣM's.
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Fig. 5. Pole-zero loci of an LPΔΣM and a BPΔΣM with different quantizer gain shown in the figure.
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IV. DAC Pulse-Shaping Coefficient Tuning

The conventional design of continuous-time ΔΣ modulators without consideration of excess loop delay would result in poor noise shaping performance and might even result in an unstable system, especially for high speed continuous-time delta-sigma modulators. From Eqs (6), (7), (8) and (9), it can be seen that actual realized Z-domain loop transfer functions with excess loop delay move away from the desired prototype transfer functions with some extra terms appearing in the numerators. To obtain the correct equivalent discrete-time loop transfer function, these terms need to be removed. A topology that adds an extra feedback as shown in Fig. 6 provides a full degree of freedom to approach this. Tuning the pulse-shaping coefficients would result in a match between the desired prototype transfer function and the actual realized loop transfer function. With an amount of extra loop delay $\delta T$ added in the delta-sigma feedback loop, the resultant equivalent discrete-time loop transfer function using the modified Z-transform is

$\tilde{A}_l(z, m) = \sum_{i=1}^{i} k_dZ_m\left[Z^{-1}\left[\frac{DAC_a(s) \cdot F^l(s)}{l \cdot nT}\right]\right]$

$k_dZ_m\left[Z^{-1}\left[\frac{DAC_b(s) \cdot F^l(s)}{l \cdot nT}\right]\right]$

Equating $\tilde{A}_l(z, m)$ to $\tilde{A}_l(z)$, we obtain the new pulse-shaping coefficients. As an example, LC resonator based delta-sigma modulators are used in this study to show how pulse-shaping coefficient tuning works, though the theory applies to any other type of continuous-time
delta-sigma modulator design. Table 1 lists some typical tuned coefficients for the second-order and fourth-order LC bandpass delta-sigma modulators with different percentages of excess loop delays. We can see that DAC pulse shaping coefficients vary logically with the change of excess delay. ELD simulation shows that LC bandpass delta-sigma modulators with excess loop delay can achieve the SNR of the ideal modulator by using the new pulse shaping coefficients. Fig. 7 shows output bit stream spectrum plots for a fourth-order LC bandpass delta-sigma modulator with a 25% loop delay. The coefficient-tuned modulator has a good noise shaping performance (Fig. 7b), while the one with the coefficients designed for the case without excess loop delay has a very poor SNR (Fig. 7a). Further, if there is an excess loop delay difference between DAC-A and DAC-B loops, we can modify Eq. (10) by writing δ_aT = (1 - m_a)T for the DAC-A loop and δ_bT = (1 - m_b)T for the DAC-B loop.

![Fig. 6. A topology of multi-feedback ΔΣM's.](image)

![Fig. 7. Output spectrum of a 4th-order LC BΔΣM.](image)

**Table 1: DAC Pulse-shaping coefficients for a second-order LC BΔΣM and a fourth-order LC BΔΣM.**

<table>
<thead>
<tr>
<th>BΔΣM’s</th>
<th>%T</th>
<th>k_a1</th>
<th>k_b1</th>
<th>k_a2</th>
<th>k_b2</th>
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<tr>
<td>2nd-order</td>
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<td>1.71</td>
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<tr>
<td></td>
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<td>-0.43</td>
<td>1.58</td>
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<td>20%</td>
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<td>1.41</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>30%</td>
<td>0.14</td>
<td>1.20</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4th-order</td>
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<td>30%</td>
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<td>0.09</td>
<td>0.76</td>
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**V. Conclusion**

The performance of continuous-time ΔΣ modulators is very sensitive to unwanted excess loop delay. Designing a continuous-time ΔΣ modulator without consideration of excess loop delay may result in very poor performance. We should therefore start the continuous-time ΔΣ modulator design based on the estimation of the total loop delay in the feedback loop or provide an adaptive tuning approach. The pulse-shaping tuning strategy can be generalized to correct for other nonidealities, such as finite DAC rise and fall times.

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**References**


