Test Stimulus Generation for Steady-State Analysis of Analogue and Mixed-Signal Circuits

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Abstract

The technique of monitoring the RMS value of the AC component of the supply current of an analogue integrated circuit has been shown to be very effective at detecting hard faults. A suitable input stimulus must be derived but this has been done by trial and error. In this paper we present a novel algorithm for deriving suitable stimuli for particular faults.

1. Introduction

Quiescent supply current monitoring has been widely advocated as a means to detect faults in digital CMOS circuits. In analogue circuits, however, the quiescent supply current is likely to be relatively large as transistors in bias networks are always conducting. A technique for monitoring the AC component of the supply current in response to a periodic waveform was therefore suggested [1]. If the RMS value of this signal is calculated, a pass/fail test may be easily derived by comparing scalar quantities. It has been further shown that even taking into account process variations, a high degree of discrimination between good and faulty circuits can be obtained [2].

To determine the steady-state value of a component of the supply current one or more periodic waveforms must be applied to the circuit inputs, typically in the form of sinusoids. A sinusoid can be described in terms of its frequency, amplitude, DC offset and in the case of two or more stimuli, their relative phases. Determining suitable values for these parameters has been an imprecise science, in which each stimulus is used in repeated fault simulations of the circuit. Thus, the best stimulus is not guaranteed to be found and moreover a large number of fault simulations are performed, just in case a stimulus should be suitable for detecting a given fault.

Some work has been done to determine suitable frequencies for test stimuli using AC sensitivity analysis [3]. This approach has to be applied with care as an AC analysis uses a model of the circuit linearized at its operating point. However, a fault might change the operating point and so the AC analysis is invalid.

We propose here a novel algorithm for finding suitable test stimuli for analogue circuits under steady-state conditions. This approach is analogous to the sensitive path algorithm and its variants used in digital test pattern generation. The overall strategy is to determine whether we can control a node and then observe the effect of a fault at a suitable output, such as the supply current. Our motivation is to reduce the large number of fault simulations currently deemed necessary to select suitable test stimuli.

The structure of the paper is as follows. In section 2 we present some other approaches to test stimulus generation. We then consider which factors affect the choice of test stimulus in section 3. Section 4 describes our proposed algorithm in detail and describes the types of analysis and tools required to implement the algorithm. Section 5 presents the results of two example circuits chosen to evaluate the algorithm.

2. Background

Several structural tests methodologies have been proposed [4] but perhaps the most effective are based on monitoring the power supply current and detecting any change from the fault free current because of a fault. Measuring the DC power supply current is
now routine for CMOS digital circuits (IDDQ) [5] and an extension of this technique to analog circuits was proposed by Bell, et al [6]. Because of the high quiescent current drawn by many analog circuits, the difference between the fault and fault-free current is in many cases not enough to ensure unambiguous detection of faults, particularly given the effects of process variations. We have previously proposed a technique that measures the RMS value of the AC component of the power supply current [1], which has proved both a more sensitive test, and which also allows detection of faults that affect the steady-state behavior of the circuit.

Structural tests are usually evaluated by fault simulation. It has been suggested that over 95% of faults are likely to be short circuits [7]. A model of the defect, i.e. an open or short circuit, is included in the netlist and the circuit is simulated. The number of simulations required is simply the number of faults included. For a circuit of moderate size the simulation time for the evaluation of time-domain tests can run into months. Macromodeling [8] and fault grouping [9] have been proposed to reduce this time penalty but the time taken to capture the faulty response of a circuit and build models of there behaviour can be comparable to sequential fault simulation. In addition behavioural macromodels of circuit blocks designed for one circuit cannot always be used for similar structures used in other circuits.

Inductive fault analysis [10] of circuit layout can significantly reduce the number of fault simulations as faults with a low probability of occurrence are not considered. This cannot, however, be applied at the time of circuit design where test requirements should be considered.

Sensitivity analysis can give an indication of how a fault might influence the output response. The adjoint network analysis technique [11] can achieve this in only two circuit simulations. Hemink, et al [12] and Hamida, et al [3] have applied AC sensitivity analysis to find the best test frequency to excite faults within filter circuits. Only small changes in the circuit elements, such as parametric faults, were considered in [3], thus ensuring that the adjoint network method could give accurate prediction of the best stimulus. However, it is questionable whether AC sensitivity analysis is valid for circuits that contain catastrophic faults, because not only will a fault affect the response but also and more importantly the fault will change the operating point of the circuit.

Other research into analog ATPG has concentrated on the application of DC sensitivity analysis to the detection of faults using DC node voltage measurements. Marlett [13] proposed a test generation technique based on choosing the most sensitive path from the fault to the output and deriving an input that would cause this path to be sensitized. The algorithm uses high level reasoning with a DC iteration to find DC inputs that will detect catastrophic faults.

3. Test stimulus selection

Let us consider why changing the parameters of a test stimulus influences the detection of faults. We first consider the choice of stimulus for DC-based tests. Many analog circuits contain nonlinear elements whose state depends on the input voltage. Certain elements might be turned off, blocking the path from a possible fault site to the output. High-level knowledge could guide the test engineer to the choice of offset, but equally, measurement of the DC power supply current may give some clues. To highlight a possible nonlinearity, the input voltages may be swept between the supply rails, and any step changes in the DC power supply current would therefore indicate that different parts of the circuit are switched on and off. DC fault simulations would then be carried out at each change in the current to determine suitable DC tests.

Choosing suitable tests to detect those faults not sensitized by DC stimuli is in general very difficult. We are concerned here only with developing stimuli to detect faults by measuring the RMS value of the AC component of the power supply current. Thus we limit ourselves to determining suitable periodic and specifically sinusoidal stimuli. A sinusoidal signal is defined by:

\[ f(V_{\text{off}}, A, f, t, \phi) = V_{\text{off}} + A \sin(2\pi ft + \phi) \]  

where \( V_{\text{off}} \) is the DC offset voltage, \( A \) is the amplitude, \( f \) is the frequency and \( \phi \) is the phase of the stimulus. Let us consider why changing any of these parameters might affect the fault coverage of a test.

Frequency. Different frequencies will be propagated through DC decoupling capacitances, and careful choice of frequency can
increase the detectability of faults. Application of a certain frequency stimulus can in some cases cause the supply current in one part of the circuit to dominate, increasing the detectability of faults within it. The supply current though a large circuit is the vector sum of the currents though each subcircuit. If there is a fault in one part of the circuit, the change in supply current due to the fault may not be large enough to ensure unequivocal detection, particularly if the thresholds of detection are based on limits determined by process variation. However the frequency response of the supply current though each partition is likely to be different and therefore by adjusting the frequency of the stimulus, one partition can be made to dominate the AC component of the power supply current.

Offset voltage. An input offset voltage will affect the DC operating point of the circuit (unless it is AC coupled). The DC input voltage will therefore determine the small signal parameters of each transistor. The AC supply current is dependent on these parameters, perhaps more so than the output voltage. Thus the nominal frequency response of the circuit can be made dependent on the DC input voltage, allowing adjustment of the AC supply current flowing though different parts of the circuit.

Amplitude. Changing the amplitude of the stimulus will change the RMS supply current though the circuit. There is a compromise, however, between signal to noise ratio and the linearity of the response. To find the best compromise we need a measure of the nonlinearity. This can be achieved with a distortion or a Fourier analysis, but a more straight-forward method is to measure the small signal transfer admittance of the supply current over a range of input offsets. The optimum peak-to-peak range would then be within the linear portion of the transfer characteristic.

Phase. If the circuit has multiple inputs, changing the phase of one signal relative to the other can also change the overall AC power supply current. For example if a circuit has two identical input stages, application of out-of-phase signals to the two inputs can cause the supply current from each to cancel (dependent again on the nonlinearity of the supply current transfer function), thus sensitizing other parts of the circuit so they dominate the power supply response.


Having explained the need to adjust the parameters of a sinusoidal stimulus we will now consider how this can be achieved automatically. In all cases we are trying to find the simplest test patterns that can detect as many faults as possible with a DC supply current test. An AC stimulus is only considered if a DC test fails to detect the fault.

1. Perform a DC sweep of the input stimulus, and at each DC value perform a sensitivity analysis to determine the sensitivity of the output signal (e.g. supply current) to each possible parametric fault and open and short circuits. If the sensitivity analysis is performed using Tellegen’s theorem, only one analysis is required to find all of these sensitivities for one output signal [11]. The sensitivity of the output to “virtual components” such as possible opens and shorts is automatically found by this method.

2. For those faults that do not appear to be sensitized by an input stimulus, perform a sensitivity analysis to determine if that fault is sensitive to the input, i.e. if a DC path exists. Again this requires one sensitivity analysis per node, but this type of analysis is not normally available in circuit simulators. If a DC path does not exist, there is clearly no point in varying the DC offset of the stimulus to try to detect that node. If a DC path does exist, but a particular fault is not sensitized, it is worthwhile to continue with the DC sweep of step 1.

3. For all those faults that appear to be sensitized, perform DC fault simulations to determine if they really are detectable. If so, those faults may be dropped from the fault list.

4. For each DC input offset perform an AC sweep, with one or more AC sensitivity analyses at each frequency point. Each sensitivity analysis will determine either the sensitivity of the output to all the remaining faults or the sensitivity of a node to the input stimulus.

5. Using a sinusoidal stimulus, for each likely frequency at each likely offset, perform transient fault simulations for those faults that appear to be sensitized. Because of the problem of faults affecting the operating point of a circuit, this approach is not guaranteed to find the best stimulus
for each fault. Instead, the objective is to find a stimulus that is likely to detect a particular fault, to determine which other faults are likely to be detectable with that stimulus and hence to perform costly fault simulations only for those faults that may be detectable and not for those faults that are very unlikely to be detected by the stimulus. Because of this uncertainty, we propose this algorithm as a strategy, rather than as a fully automated procedure, although we hope to implement a full test generation framework. Moreover, it should be noted that the analysis capabilities of many commercial simulators are not at present suited to the types of analysis we wish to perform. Step 5 implies that fault simulations should proceed until steady-state is reached, which may take many cycles.

Implementation

To be fully automated, the algorithm needs certain analysis tools that are not readily available. We have however evaluated the method by using a combination of available simulation tools and a spreadsheet. HSPICE was used as the simulation engine, it provides a DC sensitivity analysis but does not include sensitivity analysis for virtual fault sites, i.e. possible locations of open and short circuits. We have modeled virtual faults by inserting a high value resistance at the fault site and used HSPICE to calculate the sensitivity and we have normalized the sensitivity of each virtual fault to the sensitivity of the output (in this case the supply current) to a fault between Vdd and ground.

AC sensitivity is not available in HSPICE, and SPICE3f4 was found to give unreliable results. Therefore a more direct manual approach was used. The difference in the AC transfer admittance from the input to the supply terminal (IddTF) was measured at each frequency for the fault free case (IddTF_{ff}) and for each instance of a virtual fault (IddTF_{f}). The AC sensitivity was calculated from equation (2).

\[
ACsen = \frac{IddTF - IddTF_{ff}}{IddTF_{ff}}
\]  

(2)

5. Example

We illustrate the technique with an analog multiplier. This circuit was chosen because when RMS supply current monitoring had been attempted with an arbitrary test pattern the fault coverage results were disappointing (less than 50% cover).

The block diagram of the multiplier is illustrated in Fig. 1. The circuit is constructed from analog cells with a class AB opamp for the current to voltage converter (C/V), a current reference and a number of transistor arrays for the input attenuators, the voltage...
level shifters and the Gilbert cell. The circuit used contained some power-down circuitry. This is effectively redundant in terms of circuit functionality and, as will be seen, faults in this circuitry are commonly undetectable. The result of a DC input sweep for the multiplier is illustrated in Fig. 2. Both inputs had the same DC voltage applied. Again there is a noticeable step in the response at approximately -4.5 V indicating certain transistors are changing state. In addition there is a large (approximately 35%) change in the supply current between -4 V and 4 V. Therefore it would seem likely that a change in the DC offset voltage would affect the fault coverage of a DC current test and hence three DC offset voltages were chosen: -4.7 V, -3.7 V and 4 V. A DC sensitivity test was performed at each of these offsets and the percentage of faults with high sensitivity are presented in Table 1. Table 1 also shows the percentages of faults detectable by fault simulation. The third row of Table 1 gives the percentage of faults that were correctly predicted to be detectable (or not) by fault simulation. The final row shows the percentage of total faults that were predicted to be detectable and hence found to be so by fault simulation.

Combining the results of the three tests, 28 out of the 118 possible short circuit transistor faults can be removed from the fault list to be passed to the AC sensitivity analysis. First the $I_{ddTF}$ response is plotted for all input offsets of the multiplier, Fig. 3.

It can be seen that $I_{ddTF}$ is approximately linear over the range -4 to 5 volts. Over the range -5 volts to -4 volts the response is unpredictable and so input stimuli were not chosen in this range. The change in $I_{ddTF}$ over the range -4 to 5 V indicates a (slightly) nonlinear relationship between the input voltage and AC component of the supply current. This is due to the biasing arrangement used in the attenuators that causes the operating point of the transistors to depend on the DC input voltage. The effect of this is to cause the small signal resistance of the transistors to change. Therefore if a large amplitude sinusoid is applied to this circuit the supply current response will contain significant distortion. In order for the essentially linear AC sensitivity analysis to give predictable results a small amplitude sinusoid will be employed for subsequent tests.

<table>
<thead>
<tr>
<th>Percentage of faults.</th>
<th>Input offset voltage</th>
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<tbody>
<tr>
<td></td>
<td>-4.75V -3.75V 4V</td>
</tr>
<tr>
<td>High sensitivity</td>
<td>36% 26% 34%</td>
</tr>
<tr>
<td>IDDQ detected by fault simulation</td>
<td>29% 36% 24%</td>
</tr>
<tr>
<td>Correctly classified as detectable or undetectable</td>
<td>75% 75% 69%</td>
</tr>
<tr>
<td>Correctly classified as detectable</td>
<td>20% 17% 16%</td>
</tr>
</tbody>
</table>

Table 1. Comparison of faults identified as detectable by DC sensitivity analysis compared with fault simulations.

AC sensitivity tests with respect to one input were performed at -3.75, 0 and 3.75 V offsets; the frequency was swept over the range 10Hz to 10MHz. For each fault the maximum sensitivity was found. The results are presented in Table 2.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Frequency</th>
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<tbody>
<tr>
<td></td>
<td>10MHz</td>
</tr>
<tr>
<td>3.75V</td>
<td>0</td>
</tr>
<tr>
<td>0V</td>
<td>0</td>
</tr>
<tr>
<td>-3.75V</td>
<td>60</td>
</tr>
</tbody>
</table>

Table 2. The number of faults identified as detectable (total=90) with an AC sensitivity analysis for each offset and frequency.
The highest sensitivity for all faults occurred at -3.75 V DC offset, with 10MHz being the best frequency. The analysis predicted that 5 stimuli were necessary to give the highest fault cover: 100Hz, 1.8MHz, 3MHz, 5.6MHz and 10MHz. In order to test these predictions, fault simulations of all the faults considered for AC tests were performed with an input stimulus of amplitude 0.25 V and DC offset of -3.75 V applied to the Vx input and a constant offset of -3.75 V applied to the Vy input.
Fig. 4 plots the results of the tests, the first column show the fault coverage of just the 10MHz test, the next column that of the combined cover of the 10MHz and the next best test (100Hz) and the third column is the combined fault cover of the 10MHz, 100Hz and 3MHz tests.

It is seen that the 10MHz test does indeed give the best fault cover and by adding the 100Hz test, the fault coverage can be increased, but there does not seem to be any apparent benefit from adding the other tests.

The fault coverage of the tests derived from AC sensitivity analysis should be compared to that of an arbitrary test pattern generation scheme (Fig. 5) i.e. changing the input offset voltage in steps of 1 V and calculating the fault coverage for each stimulus; the amplitude of the sinusoid was again 0.25 V. It is clear that our proposed test generation scheme achieves far higher fault coverage than any arbitrary scheme but also this is achieved in only three transient fault simulations of the circuit while an arbitrary scheme will need one complete fault simulation for each change in stimulus, and may not achieve as high a fault coverage in a viable time.

The remaining faults are not detectable because they have no effect either on the supply current or the functionality of the circuit, typically because they affect the redundant circuitry of the power-down components.

6. Conclusion

This paper has described the principle of an automatic test stimulus generation technique for analog circuits. It has been shown to be both effective and easy to implement. It is directed specifically at the generation of stimuli for structural tests to detect catastrophic faults in analog circuits, with particular emphasis on using the RMS value of the AC component of the supply current.
as a testing metric.

The aim of the technique is to find the least expensive test for each fault. A fast DC power supply current test is applied first with the stimulus generated from a DC sensitivity analysis of the circuit. This will remove many of the faults that cause gross malfunction of the circuit and can therefore be done ahead of more sophisticated time domain tests. DC-based tests detect approximately 25% of faults in a multiplier circuit.

The faults that were not detected with the DC tests are passed to the next stage of the test generation algorithm. Here the best DC offset and frequency for the sinusoidal input stimulus are found using an AC sensitivity analysis. The amplitude is chosen based on the linearity of the power supply current transfer admittance of the fault-free circuit. A small amplitude gives more predictable results for circuits that are nonlinear, e.g., the multiplier circuit. The generation technique has correctly predicted a range of frequencies that are necessary to detect faults and the low fault coverage figure obtained for the multiplier from arbitrary tests was increased to over 80%.

Because this technique reduces the number of fault simulations by only investigating faults that appear to be sensitized, approximations such as inductive fault analysis may be avoidable, thus allowing pre-layout fault simulations to be conducted with greater confidence. This will be investigated further. Automation of the procedure requires further development of DC and AC sensitivity analysis techniques for virtual faults and to minimize fault simulation effort by developing steady state fault simulation methods.

Acknowledgement

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References