In this paper a comparison between Fuzzy Logic Current Controller (FLC) and classical PI current Controller for a LCL-filter based PWM rectifier is presented. Both simulations and experimental results are included. The current control of PWM rectifiers is implemented in voltage oriented coordinates, known as Voltage Oriented Control (VOC). This paper also presents design process of the Fuzzy Logic Controller based on well-known proportional-integral current controller made by backward rule. The simulations (Matlab™, Simulink™) of the current controllers are performed in model of the existing laboratory setup. The paper shows the step-response of the id current for conventional PI-controller and the proposed FLC which provides good tracking of the reference current waveform with smaller overshoot in transients for the same step in \( U_{dc} \).

I. INTRODUCTION

Current control technique of PWM rectifier has very important impact on performances of the system, such as unity power factor, low harmonics distortion, robustness for disturbances and load parameter changes. Also, provides peak current and overload protection. Several current control strategies have been developed \([1,8,9,13-15]\). Fuzzy logic controlled rectifier seems to be a good alternative to classical solutions because of its fast computing time in new decision processor \([17]\). This paper proposes a Fuzzy Logic Controller (FLC) based on the classical PI-current controller analogy \([2]\). The FLC, in comparison to conventional PI-controller has almost the same current tracking performance with smaller overshoot in transients. Moreover, for design of the FLC knowledge of plant parameters is not required. It can instead be designed based on a practical and heuristic knowledge. However, when the designer knows parameter variation range, it can be helpful for calculation of the output gains of the FLC \([3,10,11]\).

This paper presents the design process of conventional current controller for the LCL-filter based active rectifier \([5]\). It also presents a design process of the FLC based on the proportional-integral current controller. A comparison between FLC and PI controller applied to Voltage Oriented Control (VOC) of PWM rectifier is presented.

II. PI AND FLC CONTROLLERS FOR THE LCL-FILTER BASED PWM RECTIFIER

The VOC scheme for the LCL-filter based active rectifier is shown in Fig. 1. The unity power factor (UPF) condition is achieved when the line current vector, \( \tilde{i}(t) \), is in phase with the line voltage vector, \( e(t) \) as shown in Fig. 2. Therefore, a line voltage oriented synchronous-rotating coordinates \( d-q \) are used, and the reference value, \( i_{ref} \), of \( \tilde{i}(t) \) is set to zero \([5,8]\).

Fig. 1. Control circuit for testing PI and FLC for LCL-filter based active rectifier

Fig. 2. Vector diagram of active rectifier

A. Design of PI Controller

In Fig. 3, a LCL-filter based PWM rectifier is shown \([6]\). This topology is applied in a real working system in Fig. 4.
I
I

Fig. 3. Three-phase LCL-filter based active rectifier

CONTR,Z

&MODULATION

J
u
b

Fig. 4. The laboratory setup for the PWM rectifier with LCL-filter

With defined space-vectors: $\bar{v}_c(t)$ - voltage across the input filter capacitor, $\bar{v}_{id}(t)$ - converter side current, $\bar{v}(t)$ - converter side voltage, the following equation can be written:

$$\bar{v}_c(t) = R_c \bar{i}(t) + L \frac{d}{dt} \bar{i}(t) + \bar{v}(t)$$  (1)

where:

$$L = L_1 + L_2 + L_3$$

In dq coordinates two voltage equations can be written as:

$$\begin{align*}
\bar{v}_{cd}(t) &= R_c \bar{i}_{d}(t) + L \frac{d}{dt} \bar{i}_{d}(t) + \bar{v}_{q}(t) + \alpha \omega L \bar{i}_{q}(t) \\
\bar{v}_{cq}(t) &= R_c \bar{i}_{q}(t) + L \frac{d}{dt} \bar{i}_{q}(t) + \bar{v}_{d}(t) + \omega \omega L \bar{i}_{d}(t) \\
\end{align*}$$  (2)

where: $\alpha \omega L \bar{i}_{d}(t), \alpha \omega L \bar{i}_{q}(t)$ are feedforward compensation (Fig. 5) of the cross coupling effects. The controllers for both d and q axis can be designed on the basis of the following plant transfer function:

$$G(s) = \frac{1}{I + Ts}$$  (3)

The d,q currents are controlled by means of the d,q converter side voltages.

The two PI-controllers generate commands for space-vector modulator. The control plant for the d,q-currents control have the same time constant $T_{M} = L/R_c$ Two PI-based controllers can be used to perform the control action. They have the following form in the S-domain:

$$D(s) = \frac{k_p (I + T_s)}{T_s}$$  (4)

where: $k_p$ proportional gain and $T_s$ time constant of the integrator.

The processing and modulation delays are taken into account in the design [7].

The current control loop (Fig. 6) consists: the pulse width modulator $M(s)$ and the antialiasing filter on the feedback current $C(s)$.

Fortunately if a symmetrical switching function is adopted by the modulator, the sampled signal is free of switching harmonics. Thus the sampling theorem can be complied with a high cut-off frequency such as the delay introduced is a negligible fraction of the sampling period.

The variations in the grid voltage and uncompensated nonlinearities have been modeled with the disturbance $w$.

The processing delay $T_p$ and one sampling period due to the microcontroller is taken into account with the first order transfer function $P(s)$:

$$P(s) = \frac{1}{1 + T_p}$$  (5)

One block is substituted to the two blocks with the smallest time constants ($M(s)$ and $P(s)$) that are grouped together. Its time constant is the sum of the $M(s)$'s and $P(s)$'s time constants. In Fig. 7 the current loops used for the PI design in S-domain is reported.

The digital version of the Fig. 7's current loop in the Z-domain is reported in Fig. 8, $Z^s$ is the processing delay, $D(s)$ is the digital version obtained with the backward rule of the controller $D(s)$ and $G(s)$ is the zero order hold equivalent of the system $G(s)$ that includes also the effects of the modulator as will be explained in the following. $F(s)$ is the filter.

Fig. 5. Ac current control in d-q rotating frame

Fig. 6. Current control loop in S-domain

Fig. 7. Equivalent current control loop in S-domain
The PI-based regulator obtained with the backward discretization rule (Fig.9) is:

\[
G(z) = \frac{G(s)}{1 - z^{-1}}
\]

The plant \( G(z) \) is the Zero Order Hold (ZOH) equivalent of the plant transfer function \( G(s) \). This is justified by the fact that the Zero Order Hold is a suitable model of the Analogue to Digital (A/D) conversion:

\[
G(z) = (1 - z^{-1})G(s)
\]

However the ZOH introduces half a sampling period delay that is exactly how much should be considered to take into account the modulator influence. In Fig. 10 the current control loop in Z-domain is reported. The PI controller can be designed both in S-domain and in Z-domain. The first approach offers a better mathematical basis for the design procedures, the second approach offers an easier verification in the z-plane of the desired dynamic performances and stability margins. Moreover one should consider that in view of a digital implementation of the controller it is always better to verify the controller with a Z-plane analysis. The best approach seems to be a mixture of the two procedure: make a rough design in the S-domain and then use the Z-plane to verify the obtained controller and maybe to adjust it considering filtering and processing delays.

The zero/pole placement method with 0.7 damping is used for calculate of the PI-controllers. So the system was critically damped.

\[
G(s) = \frac{K_p}{s} = \frac{1}{s}\left(\frac{1}{s^2 + \omega_n^2}\right)
\]

where: \( \omega_n = \sqrt{\frac{L_C}{L}} \) and \( \omega_{n0} = \frac{\omega_n}{2} \).

Thus the LCL filter has two zero and two poles more, in the open loop transfer function, compared to consider only the L-filter. If the transfer function expressed by (8) is discretized and the closed loop root locus is considered, with the PI controller tuned using the previously reported criteria (i.e. considering only the inductance \( L_R \)), the new zero and poles can make the system unstable if a proper damping is not adopted. The damping is performed by a resistor in series with the filter capacitor: this will move the unstable poles more inside the stability region [5].

### B. Design of FLC Controller

The block scheme of the Fuzzy Logic Current Controller is shown in Fig. 11. The FLC has two inputs (feedback) and two outputs (control variables). The input signals are defined as error and error change. Two outputs are responsible for proportional gain \( K_p \) and integral time \( K_i \). Hence, four linguistic variables are available.

In the proposed FLC (Fig.11), in fuzzification block F1 input crisp values (real numbers) are converted into linguistic variables (fuzzy numbers). Rules Base describes interactions between input and output linguistic variables based on simple relation. In defuzzification block DFI input linguistic variables are transferred into crisp values. There are various defuzzification criterion strategies: Center of Gravity - COG, Mean of Maximum Method - MOM and Max. MOM provides better performances in transient but COG yields superior results in steady-states. COG provides results, which are similar to those obtainable with conventional PI controller [16].

The controller based on analogy with classical PI controller made by backward rule. The \( e, \Delta e, K_p, K_i \) - describe linguistic variables in the universes of error, error change, proportional and integral gain, respectively. From reference and actual values, by equation (9) and (10) are made two input variables.

There is no theory about how many terms (fuzzy sets) are

![Fig. 11. Block Scheme of the proposed Fuzzy Logic Controller (FLC) for the active rectifier](image)
necessary to describe the linguistic variables [4]. It depends on the chosen methodology. The error and error change are calculated from:

\[ e = i_{\text{ref}} - i \]  

(9)

\[ \Delta e = e_k - e_{(k-1)} \]  

(10)

where:
- \( e \) - error,
- \( e_k \) - error values in \( k \) step,
- \( e_{(k-1)} \) - error values in \((k-1)\) step,
- \( i_{\text{ref}} \) - reference current.

Scale factors at the inputs \((k_e, k_{AE})\) and outputs \((k_{pi}, k_{pi})\) are introduced. Main aim of those factors is to convert the input crisp values to linguistic variable in demanded universe of discourse, and outputs' linguistic variable to demanded proportional and integral gain. The base values for \( k_{pi} \) and \( k_{pi} \) can be taken from calculated gains for classical PI.

The proposed FLC has five fuzzy sets for \( e \) error input and three for \( \Delta e \) error change input. They have been defined respectively as: NB - negative big; NS - negative small; Z - zero; PS - positive small; PB - positive big; and N - negative; P - positive; Z - zero.

For both output the three outputs fuzzy sets have been defined as: S - small; M - medium; B - big.

The defined membership functions are triangular and trapezoidal in shapes as illustrated in Fig. 12. The fuzzy rules are described in TABLE I. The rules for \( kp \) and \( ki \) output are chosen separately.

The fuzzy rules have been set by formula:

- \( R, : \) if error, and error change, then \( kp \)
- \( R, : \) if error, and error change, then \( ki \)

where: \( j = 1,2,\ldots \)

The control actions on the linguistic variables are translated into crisp values in the defuzzification block.

At the output of the FLC the crisp value that is defined as nonlinear function (control surface) is obtained:

\[ u = f(u_{kp}, u_{ki}) \]  

(11.1)

\[ u = u_{kp} + u_{ki} \]  

(11.2)

where:

\[ u_{kp} = \Delta e K_p \]  

(11.3)

\[ K_p = k_p \cdot k_{pl} \]  

(11.4)

\[ u_{ki} = \Delta e K_i \]  

(11.5)

\[ K_i = k_i \cdot k_{ii}, \quad K_{i-1} = k_{i-1} \cdot k_{ii} \]  

(11.6)

\( K_{i-1} - K_i \) integration time in \( z-1 \) step

The advantage of FLC is variable gains. The classical PI controller has fixed values of the proportional and the integration gains. The FLC has variable outputs gains dependent on values of the controlled error and error change.

<table>
<thead>
<tr>
<th>( \Delta e )</th>
<th>NB</th>
<th>NS</th>
<th>Z</th>
<th>PS</th>
<th>PB</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>M</td>
<td>M</td>
<td>M</td>
<td>B</td>
<td>B</td>
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<tr>
<td>Z</td>
<td>B</td>
<td>B</td>
<td>S</td>
<td>M</td>
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<td>P</td>
<td>B</td>
<td>B</td>
<td>S</td>
<td>S</td>
<td>S</td>
</tr>
</tbody>
</table>

When the system works in steady state then \( e \) and \( \Delta e \) are small. It means that in this case the control process should be very smooth.

In transient when \( e \) and \( \Delta e \) have high values the dynamics of the FLC should be very fast. Therefore, fuzzy rules for big and small values of the input should be chosen in different way.

III. SIMULATION AND EXPERIMENTAL RESULTS.

The simulations of the current controllers are performed in Matlab™, Simulink™ model of the existing laboratory setup (Fig. 4) [5].

All simulations are performed for parameters as shown in TABLE I.

The step-response of the \( i_d \) current for conventional PI-controller (Fig. 13a) and FLC controller (Fig. 13b) provides tracking of the reference current waveform with 10% smaller overshoot in transient for the same step in \( U_{DC} \).
The steady state for investigated controllers is reported in Fig. 14.

The experimental set-up, consists of a three-phase 3 kVA programmable power supply, a commercially available Danfoss inverter VLT™ 5005 (TABLE III) without control board. The control is implemented on a dSPACE DS1103 board with floating-point Motorola processor and TI TMS320F240 fixed-point Digital Signal Processor; the timing of the system and the PWM generation are performed by the DSP [12].

The experimental results have been measured for classical PI and FLC current controllers and they are shown in Fig. 15. As shown in Fig. 15a, and Fig.15b performance of the proposed FLC and classical PI-controller are very similar in steady state.

<table>
<thead>
<tr>
<th>Parameters of the LCL-filter based PWM Rectifier</th>
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<tbody>
<tr>
<td>$L_1$</td>
</tr>
<tr>
<td>$L_2$</td>
</tr>
<tr>
<td>$C_1$</td>
</tr>
<tr>
<td>$C_2$</td>
</tr>
<tr>
<td>Switching frequency</td>
</tr>
<tr>
<td>Sampling frequency</td>
</tr>
<tr>
<td>$k_{c}$</td>
</tr>
<tr>
<td>$k_{pm}(T/T_1)$</td>
</tr>
</tbody>
</table>

Table II

The steady state for investigated controllers is reported in Fig. 14.

The experimental set-up, consists of a three-phase 3 kVA programmable power supply, a commercially available Danfoss inverter VLT™ 5005 (TABLE III) without control board. The control is implemented on a dSPACE DS1103 board with floating-point Motorola processor and TI TMS320F240 fixed-point Digital Signal Processor; the timing of the system and the PWM generation are performed by the DSP [12].

The experimental results have been measured for classical PI and FLC current controllers and they are shown in Fig. 15. As shown in Fig. 15a, and Fig.15b performance of the proposed FLC and classical PI-controller are very similar in steady state.
IV. CONCLUSIONS

As shown in this paper the fuzzy logic control (FLC) technique can be used for PWM line current controller. In steady state FLC works like classical PI because used defuzzification criterion strategy (Center of Gravity yields similar results to conventional PI controller [16]). Thanks to variable gain and integration time dependent on the value of control error and error changes the FLC provides better line current tracking with about 10% smaller overshoots in transient.

The implementation is relatively simple because the FLC is no computational burden for processors, especially, for new decision processors, which allow to implement the fuzzy logic in practice in easy, end non-costly way. The advantage of this solution is faster computing in comparison with classical PI [17].

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