MODELING OF A DSTATCOM WITH ULTRA-CAPACITAR ENERGY STORAGE FOR POWER DISTRIBUTION SYSTEM APPLICATIONS

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Summary – This paper describes the dynamic modeling of a distribution static synchronous compensator (DSTATCOM) coupled with ultra-capacitor energy storage (UCES) for improving the power quality of power distribution systems. Two modes of operation are assessed, i.e. voltage control for voltage fluctuations ride-through and dynamic active power control for power flow compensation. New detailed models and dynamic control schemes are proposed. The control technique employed is based on the instantaneous power theory on the synchronous-rotating dq reference frame. Validation of models and control algorithms is carried out through simulations in SimPowerSystems of MATLAB/Simulink.

Keywords: Custom power (CP) – Distributed generation – Distribution static synchronous compensator (DSTATCOM) – Super-capacitor energy storage (SCES) – Ultra-capacitor energy storage (UCES).

1 INTRODUCTION

Utility and customer-side disturbances result in bus voltage fluctuations, transients, and waveform distortions on the distribution system. Just as flexible AC transmission systems (FACTS) permit to improve the reliability and quality of transmission systems, these controllers can be used in the distribution level with comparable benefits for bringing solutions to a wide range of problems. In this sense, FACTS-based power electronic controllers for electric distribution systems, namely custom power (CP) devices, are able to enhance the reliability and quality of power provided to customers. This situation is especially significant when dispersed or distributed generation (DG) based on wind generation is connected in the area, so that stabilizing devices are strongly needed to maintain reliable and stable operation of the power system [1].

A DSTATCOM is a fast response, solid-state power controller that provides flexible voltage control at the point of connection (PCC) to the utility distribution feeder for power quality (PQ) improvements. It can continuously generate reactive power by varying the amplitude of the inverter voltage with respect to the line bus voltage so that a controlled current flows through the tie reactance between the DSTATCOM and the distribution network. This enables the DSTATCOM to mitigate voltage fluctuations such as sags, swells, transients and to provide voltage regulation, power factor correction and harmonics compensation. [2].

The addition of energy storage through an appropriate interface to the CP device leads to a more flexible integrated controller. The ability of the DSTATCOM-ESS for supplying effectively extra active power allows expanding its compensating actions, reducing transmission losses and enhancing the operation of the electric grid. Various types of advanced energy storage technologies can be incorporated into the DC bus of the DSTATCOM, namely superconducting magnetic energy storage (SMES), ultra-capacitor energy storage (UCES) and flywheel energy storage (FES), among others. However, ultra-capacitors have distinct potential advantages for energy storage which make them almost unbeatable in many applications [3]. Because they have no moving parts, and require neither cooling nor heating, and because they undergo no internal chemical changes as part of their function, they are very efficient and robust. Also, they require practically
no maintenance and the lifetime is measured in decades, with no lifetime degradation due to frequent and deep cycling. They have no significant fringe fields and they are intrinsically modular which enhances reparability and allows capacity to be easily incremented. Ultra-capacitors store only a relatively modest quantity of energy, but they are capable of high power discharge rates and fast recharge. This paper discusses the dynamic performance and the modeling of a DSTATCOM with UCES for improving the operation of power distribution systems. The proposed integrated DSTATCOM-UCES controller is studied for riding through voltage fluctuations such as sags/swells and dynamically controlling active power independently of reactive power for stability augmentation purposes. The control technique employed comprises a full decoupled current control strategy using the instantaneous power theory in the synchronous-rotating d-q reference frame. The integrated controller is modeled and simulated using SimPowerSystems of MATLAB/Simulink to validate the proposed global system.

2 MODELING OF THE DSTATCOM-UCES

A DSTATCOM consists of a three-phase inverter shunt-connected to the distribution network by means of a coupling transformer and the corresponding control scheme, as depicted through the block diagram of Fig. 1. Its topology allows the device to generate a set of three almost sinusoidal voltages at the fundamental frequency, with controllable amplitude and phase angle. The addition of ultra-capacitor energy storage through an appropriate interface to the DSTATCOM device allows supplying effectively extra active power and thus expanding its compensating actions so that the operation of the electric grid can be improved. The ultra-capacitor (UC) is a relative recent technology in the field of energy storage systems based on the electric double layer capacitor (EDLC or simply DLC). The construction and theory of operation of a DLC can be understood by examining the schematic view of its internal components presented in Fig. 2 [4]. The elementary structure consists of two activated porous carbon electrodes immersed into an electrolytic solution, and a separator that prevents physical contact of the electrodes but allows ion transfer between them. Energy is stored in the EDLC as a charge separation in the double layer formed at the interface between the solid electrode material surface and the liquid electrolyte in the micropores of the electrodes. This effectively creates two equivalent capacitors connected in series, which gives the name to the structure. The ultra-capacitor performance is based mainly on an electrostatic effect, which is purely physical reversible, rather than employing faradic reactions, although includes an additional pseudocapacitive layer contributing to the overall capacitance. Because of the complex physical phenomena in the double layer interface, traditional simple models such as the classical lumped-parameter electrical model [5] represented by a simple RC circuit are inadequate for modeling EDLCs. Thus, this work proposes the use of an enhanced electric model of an UC based on [6] that reflects accurately the effects of frequency, voltage and temperature in the dynamic behavior. The model proposed, which is summarized in Fig. 2, describes the terminal behavior of the EDLC unit over the frequency range from DC to several thousand Hertz. Fig. 3 describes the dynamic simulation model of the proposed DSTATCOM-UCES system. This model consists of the voltage source inverter (VSI), the coupling step-up transformer, the line filter, the DC bus.
capacitors, the buck-boost converter, and the bank of ultra-capacitors. The VSI presented corresponds to a DC to AC switching power inverter using Insulated Gate Bipolar Transistors (IGBT). In the distribution voltage level, the switching device is generally the IGBT due to its lower switching losses and reduced size. In addition, the power rating of custom power devices is relatively low. As a result, the output voltage control of the DSTATCOM-UCES can be achieved through pulse width modulation (PWM) by using high-power fast-switched IGBTs. The inverter structure is based on a three-level pole structure, also called neutral point clamped (NPC), instead of a standard two-level six-pulse inverter structure. This three-level VSI topology generates a more smoothly sinusoidal output voltage waveform than conventional structures without increasing the switching frequency. The flexibility of an extra level in the output voltage is used to assist in the output waveform construction. In this way, the harmonic performance of the inverter is improved, also obtaining better efficiency and reliability respect to the conventional two-level inverter. The connection through the step-up coupling transformer to the utility grid is made by using low pass sine wave filters in order to reduce the perturbation on the distribution system from high-frequency switching harmonics generated by PWM control.

In practical applications, the required amount of terminal voltage and energy of the UCES system can be achieved by using multiple UC modules in series and parallel. The terminal voltage determines the number of capacitors $N_s$ which must be connected in series to form a string, and the total capacitance determines the number of capacitor strings $N_p$ which must be connected in parallel in the bank. The amount of energy drawn from the ultra-capacitors bank is directly proportional to the total capacitance and the change in the terminal voltage ($V_{UCB}$-initial and $V_{UCB}$-final voltages), as given by Eq. 1.

$$E_{UCB} = \frac{1}{2}C_{UCB}\left(V_{UCB}^2 - V_{UCB}^{2f}\right), \quad (1)$$

The integration of the UCES system into the DC bus of the DSTATCOM device requires a rapid bidirectional interface capable of both a step-down and a step-up function in the two directions (two quadrants) to obtain a suitable control performance of the overall system. In this work, a combined buck-boost DC–DC converter topology by using high-power fast-switched IGBTs is adopted to this aim. The bidirectional DC–DC converter (aka chopper) has basically two modes of operation, namely the buck or charge mode and the boost or discharge mode. In the charge mode, the chopper works as a step-down (buck) converter. This topology makes use of modulation of the switch $T_{bck}$ (upper IGBT in the leg), while keeping the switch $T_{bst}$ off at all times, in order to produce a power flow from the DSTATCOM DC bus to the ultra-capacitors bank. In the discharge mode, the chopper operates as a step up (boost) converter in collaboration with the DC bus capacitors. This topology employs the modulation of the lower IGBT of the leg, i.e. $T_{bst}$, and maintains $T_{bck}$ off all the time to produce a power flow from the UC bank to the DSTATCOM DC bus.

A general expression relating the bidirectional chopper average output voltage $V_{UCB}$ to the VSI average DC bus voltage $V_d$ can be derived through Eq. 2.

$$V_{UCB} = mV_d, \quad (2)$$

being $m \in [0, 1]$ the modulation index expressed as:

$m = D$ for the chopper in buck mode (charge),

$m = (1-D)$ for the chopper in boost mode (discharge),

where $D$ is the duty cycle for switching $T_{bck}$ or $T_{bst}$ according to the operation mode.

Fig. 3. Detailed model of the proposed DSTATCOM-UCES.
3 CONTROL OF THE DSTATCOM-UCES

The proposed multi-level control scheme for the integrated DSTATCOM-UCES device, consisting of external, middle and internal levels, is based on concepts of instantaneous power on the synchronous-rotating $dq$ reference frame [7] as depicted in Fig. 4. Rotating reference frame is used because it offers higher accuracy than stationary frame-based techniques.

3.1 External Level Control

The external level control is responsible for determining the active and reactive powers exchange between the DSTATCOM-UCES device and the utility electric system. The proposed external level control scheme is designed for performing two major control objectives: the voltage control mode (VCM) for ride-through voltage fluctuations and the active power control mode (APCM) for dynamic active power exchange between the UCES and the electric grid.

The standard control loop of the external level is the VCM described in Fig. 4. This control block regulates the voltage at the point of connection through the modulation of the reactive component of the output current, $i_q$, for riding-through voltage fluctuations such as sags/swells [8]. To this aim, the instantaneous voltage at the PCC is computed by using a synchronous rotating orthogonal reference frame. Hence, the instantaneous values of the three-phase AC bus voltages are transformed into $dq$ components, $v_d$ and $v_q$, respectively, and then filtered to extract the fundamental components, $v_{d1}$ and $v_{q1}$. As a result, the design of the control loop is simpler than using stationary frame techniques, by employing standard proportional-integral (PI) compensators. A voltage regulation droop $R_d$ is included in order to allow the terminal voltage of the DSTATCOM-UCES to vary in proportion with the compensating reactive current. Thus, the PI controller with droop characteristic becomes a simple phase-lag compensator (LC1), resulting in a stable fast response compensator.

The APCM depicted in Fig. 4 allows controlling the active power exchange between the ultra-capacitor energy storage system and the utility grid by means of the DC-DC converter. This control mode compares the reference power set by an external input with the actual measured value in order to eliminate the steady-state in-phase output current component of the custom power device via a PI compensator. In this way, the active power flow between the DSTATCOM-UCES and the power system can be controlled so as to force the ultra-capacitors to absorb active power when $P_r$ is negative, i.e. operating in the charge mode, or to inject active power when $P_r$ is positive, that is operating in the discharge mode.

![Fig. 3. Multi-level control scheme for the DSTATCOM-UCES compensator.](image-url)
3.2 Middle Level Control

The middle level control makes the expected output to dynamically track the reference values set by the external level. In order to derive the control laws for this block, a dynamic model of the DSTATCOM-UCES in the $dq$ reference frame is used, which is described in depth in [8]. By applying Kirchhoff’s voltage law, the steady-state model is derived and summarized in the state-space as follows:

$$
\begin{bmatrix}
i_d \\
i_q \\V_d
\end{bmatrix}
=\begin{bmatrix}
\frac{-R_s}{L_s} & \omega & \frac{maS_d}{2L_s} \\
-\omega & \frac{-R_q}{L_q} & \frac{maS_q}{2L_q} \\
\frac{-3}{2C_d}maS_d & \frac{-3}{2C_d}maS_q & \frac{-2}{R_pC_d}
\end{bmatrix}
\begin{bmatrix}
i_d \\
i_q \\V_d
\end{bmatrix}
-\begin{bmatrix}
i_d \\
i_q \\0
\end{bmatrix}
\frac{V}{L_s}
$$

being,

- $R_s$: series resistance representing the transformer winding resistance and VSI IGBTs conduction losses.
- $R_p$: parallel resistance accounting for the VSI switching losses and the power loss in the DC capacitors.
- $L_s = L_s - M$: series inductance accounting for the equivalent leakage $L_s$ and the mutual equivalent inductance $M$ of the step-up transformer.
- $C_d$: equivalent capacitance of the two DC bus capacitors of the VSI, computed as the series of $C_f$ and $C_2$.
- $a = \frac{\sqrt{3}n_2}{\sqrt{2}n_1}$: voltage ratio of the coupling transformer.
- $S$: average switching factor matrix in $dq$ frame.
- $\alpha$: phase-shift of the VSI output voltage from the reference position
- $\omega$: synchronous angular speed of the network voltage at the fundamental system frequency (50 Hz)

Inspection of Eq. 3 shows a cross-coupling of both components of the DSTATCOM-UCES output current (through $\omega$). Therefore, for achieving a decoupled active and reactive power control, it is simply required to decouple the control of $i_d$ and $i_q$. Thus, by generating the appropriate control signals $\chi_1$ and $\chi_2$ derived from setting to zero derivatives of currents in Eq. 3 via conventional PI controllers with feedback of VSI output current components $i_{d1}$ and $i_{q1}$, a decoupled VSI control algorithm is obtained.

Assessment of Eq. 3 also shows an additional coupling of derivatives of $i_d$ and $i_q$ with respect to the DC voltage $V_d$. This issue requires maintaining the DC bus voltage as constant as possible in order to decrease the influence of the dynamics of $V_d$. The solution to this problem is obtained by using a DC bus voltage controller according to the operation mode of the DSTATCOM-UCES via a PI compensator for eliminating the steady-state voltage variations at the DC bus. In the case that the UCES is not used, i.e. using a conventional DSTATCOM, or when the DSTATCOM-UCES is in charging operation mode, the DC bus voltage control is achieved by forcing a small active power exchange with the electric grid for compensating VSI losses. This is obtained with the switch $S_2$, in the middle level control, set at position L (low). In the case that the DSTATCOM-UCES is in discharging operation mode, the DC bus voltage control is achieved through the ultra-capacitors banks themselves by setting the switch $S_2$ at position H (high).

In the charging operation mode of the UCES, switches $S_1$ to $S_4$ are set at position L, so that the DC-DC converter acts as a buck or step-down chopper. In this way, only the upper IGBT is switched while the lower one is kept off all the time. Since the ultra-capacitor current is highly responsive to the voltage applied, an adaptive hysteresis (nearly constant-frequency) current control technique (AHCC) for the DC-DC converter operating in continuous conduction mode of $I_{UCB}$ is proposed [9]. The AHCC is based on cycle-by-cycle hysteresis calculator, which generates the hysteresis window that will keep the switching frequency in a very narrow band centered on a programmed average value. In this way, the charging of the UCES is rapidly accomplished at a constant current near $I_{UCB}$ while the voltage $V_{UCB}$ is below the limit $V_{UCB}$. During this process, the VSI DC bus voltage is controlled through the inverter control itself in the same way used for a standard DSTATCOM with no energy storage. Thus, the VSI will provide the power required to charge the UCES, while maintaining the DC link voltage nearly constant. When the ultra-capacitor maximum voltage is reached, the DC-DC buck converter IGBT is switched-off and the charging operation mode of the UCES is ended.
In the discharging operation mode of the UCES, switches \( S_1 \) to \( S_4 \) are set at position H, so that the DC-DC converter acts as a boost or step-up chopper. In this way, only the lower IGBT is switched while the upper one is kept off at all times. In this operating mode, the external level control determines the power required to be exchanged with the electric system. Since the ultra-capacitor discharge current is to be controlled by the DC-DC converter input impedance, a pulse-width modulation (PWM) control technique with double-loop control strategy is proposed to be employed. This control mode has low harmonic content at a constant-frequency and reduced switching losses. In this case, the VSI DC bus voltage is controlled through an UCES voltage loop, by managing the energy released from the ultra-capacitor banks towards the VSI. Thus, by adjusting the duty cycle \( D \) of the boost chopper through a proportional-integral (PI) control of the error signal between the reference and the measured voltage at the DC bus, the steady-state DC link voltage variations can be eliminated. An inner current loop is introduced into the voltage loop to achieve an enhanced dynamic response of the ultra-capacitor current \( I_{UCB} \).

3.3 Internal Level Control

Fig. 4 (right side) sketches a basic scheme of the internal level control of the DSTATCOM-UCES. This level is responsible for generating the switching signals for the twelve IGBTs of the three-level VSI, and the two ones of the bidirectional DC-DC converter. The internal level is mainly composed of a line synchronization module, a double PWM firing pulses generator for both the VSI and the lower IGBT of the bidirectional dc-dc converter (step-up operation) and a hysteresis control firing pulses generator for the upper IGBT of the DC-DC converter (step-down operation). The line synchronization module consists mainly of a phase locked loop (PLL). This circuit is a feedback control system used to automatically synchronize the DSTATCOM-UCES device switching pulses, through the phase \( \theta_s \) of the inverse coordinate transformation from \( dq \) to \( abc \) components, with the positive sequence components of the ac voltage vector at the PCC \( (v_q) \).

4 DIGITAL SIMULATION RESULTS

Performance of models and control strategies are assessed by computer simulation carried out in SimPowerSystems of MATLAB/Simulink [10]. The test distribution power system is depicted in Fig. 5 as a single-line diagram. Such a system implements a 50 MVA substation represented by a Thevenin equivalent, which feeds a distribution network operating at 25 kV/50 Hz. A set of linear loads grouped at bus 3 are linked to the substation via a 20 km distribution line. The proposed DSTATCOM-UCES device is connected at bus 3 and includes a 25/1.2 kV step-up transformer with a ±1.5 MVA VSI and a 750 kW UCES.

4.1 Base case

The topology presented in the test system without the connection of the DSTATCOM-UCES (B1 is open), the so-called base case, is used as a benchmark for all the subsequent studies. Under this situation, the distribution utility feeds a linear load of 1.5 MW/0.35 Mvar, i.e. only the breaker B2 is closed. The supply voltages and currents are balanced and in steady state. At \( t=0.4 \) s, a linear reactive load of 0.8 Mvar is suddenly connected at bus 3 by closing B3 and later disconnected at \( t=0.6 \) s. Fig. 6 presents the system voltage response at bus 3 before, during and after the contingency described. As can be seen, the increase of the inductive reactive load produces a voltage sag of near 21% with respect to the value in steady-state during 200 ms, until the reactive load is disconnected. This voltage perturbation can be cleared observed as much in the phase voltage, \( v_a \), as in the \( d \) voltage component at the PCC, \( v_d \).

![Fig. 5. Single-line diagram of the test power system.](image-url)
4.2 Case a: Connection of DSTATCOM-UCES in Voltage Control Mode (VCM)

The impact of the inclusion of a DSTATCOM-UCES controller at bus 3 operating in VCM can be analyzed through the simulation results of Fig. 7. The good performance of the voltage regulator of the DSTATCOM device is evidently depicted by the rapid compensation of reactive power, after connection at \( t = 0.2 \) s by closing the breaker B1, and even more during the voltage sag between 0.4 s and 0.6 s. As can be noted from actual and reference values of \( i_q \), the only reactive power exchange with the utility system, independent of the active power, allows to quickly restore the voltage back to the reference value of near 1 p.u. and thus mitigating completely the voltage sag. The DSTATCOM-UCES provides near 0.83 Mvar of capacitive reactive power for improving the voltage profile. The active power demanded by loads is slightly enlarged by the global improvement of the voltage profile at bus 3.

4.3 Case b: Connection of DSTATCOM-UCES in Active Power Control Mode (APCM)

In case b, which is shown in Fig. 8, the main goal of the DSTATCOM-UCES is to control the active power flow injected/absorbed by the integrated compensator. The bank of UC simulated is composed of a string of 3 Maxwell Boostcap® modules BMOD0018-P390 (18 F/390V), yielding an equivalent structure of 6F/1170V/2.5MJ [12]. As in the previous case, the DSTATCOM-UCES is activated at \( t = 0.2 \) s but now in APCM, and is set to provide 0.6 MW of active power to the utility grid between 0.4 s and 0.6 s, that is to say during the voltage sag. As can be noted, all the active power managed through the VSI is discharged from the UC bank, and is independent of the reactive power exchange. During the voltage sag, the injection of active power allows supporting the PCC voltage at approximately 0.97 p.u. and thus mitigating entirely the sag. In such situation, the UCES operates in the discharging mode for delivering almost 0.12 MJ of energy, by varying its voltage from an initial value of 1 kV to 979 V.

5 CONCLUSIONS

This paper proposed a new model and a control scheme of a distribution static compensator (DSTATCOM) coupled with ultra-capacitor energy storage (UCES) for improving the operation of power distribution systems. A realistic detailed full model of the enhanced compensator was presented, including a new
approach of modelling the electric behaviour of a bank of ultra-capacitors in highly dynamic applications. Dynamic system simulation studies demonstrate the effectiveness of the proposed models and control approaches in the synchronous-rotating $dq$ reference frame. The improved capabilities of the integrated DSTATCOM-UCES controller to rapidly control the active power exchange between the UC bank and the utility system, simultaneously and independently of the reactive power exchange, permit to greatly enhance the operation and control of the electric system. The fast response device shows to be very effective in enhancing the distribution power quality, successfully mitigating disturbances such as voltage sags, among others.

6 REFERENCES