A ZVS-PWM Single-Phase Inverter Using a Simple ZVS-PWM Commutation Cell

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***Abstract*—A new zero-voltage-switching (ZVS) pulsewidth-modulated (PWM) single-phase inverter using a simple ZVS-PWM commutation cell is presented in this paper. Except for the auxiliary switches, all switching devices in the ZVS-PWM single-phase inverter operate at ZVS turn on and turn off. The auxiliary switches operate at zero-current-switching turned-on and turned-off. Besides operating at constant frequency, the proposed inverter has no overvoltage across the switches on the main switch compared to the hard switching inverter counterpart. Auxiliary components rated at very small current are used. The principle of operation, theoretical analysis, and experimental results of the new ZVS-PWM single-phase inverter, rated 1 kW and operated at 40 kHz, are provided in this paper to verify the performance.**

***Index Terms*—Inverter, zero-voltage-switching (ZVS).**

I. Introduction

MUCH EFFORT has been exerted by researchers all over the world in an attempt to reduce harmonic distortion and audible noise in the output of the inverter. Their objectives have been attained through an increase in inverter commutation frequencies and appropriate modulation strategy. These measures have provided some benefits, such as a reduction in the weight and volume of the magnetic elements. However, they have caused some difficulties due to the high commutation losses in the switches and the appearance of electromagnetic interference. These factors occur mainly in inverter topologies that use the bridge inverter configuration. At the moment that the main switch turns on, the antiparallel diode of the bridge complementary switch begins its reverse recovery current. Both contribute significantly to increasing the commutation losses and producing electromagnetic interference.

Recently, to address this problem, a number of soft-switching pulsewidth modulation (PWM) techniques were proposed aimed at combining desirable features of both the conventional PWM and resonant techniques. The zero-voltage-switching (ZVS) approaches are desirable for a majority of carrier semiconductor devices such as MOSFETs, since the turn-on loss caused by the output capacitance is large. The zero-current-switching (ZCS) approaches are suitable for the minority of carrier semiconductor devices such as insulated gate bipolar transistors (IGBTs), since the turn-off loss is large due to the current tail characteristics. IGBTs are preferred for high-power application, since they have a higher voltage rating. However, IGBTs are relatively slow in switching speed, so the switching losses and the high frequency of operation are two well-known problems. Thus, IGBTs are not suitable for high frequency converter application. IGBTs have been replaced by MOSFETs for high frequency and medium power converter applications. For improving MOSFETs' switching losses problem, several soft switching techniques have been proposed for the PWM inverter, and nearly all of them accomplish ZVS. Typical examples are the auxiliary resonant commutated pole inverter (ARCP) [1]–[3] and the ZVS and zero voltage transition (ZVT) inverter [4]–[14]. The ARCP is composed of one bidirectional switch, one resonant inductor, resonant capacitors, and two ac sources or two low-frequency capacitors. The arrangement of the capacitors can be considered a single capacitor connected to the midpoint of the input source. Therefore, the low-frequency capacitors provide the input voltage share. This topology is interesting whenever half-bridge topologies are employed. Now, if the full-bridge topology is considered, two ARCPs will be necessary, one for each leg, besides two large input capacitors to divide the input voltage source. This practice may increase the volume of the converter. It is important to comment that, in some cases, as in high voltage, the capacitors may be center-tapped ones. In these cases, the volume is not penalized. Furthermore, the auxiliary commutation circuit only helps main switches turn-on to perform ZVS, while snubber capacitors reduce turn-off losses. At main switches turn-off, the load current charges these capacitors, and as a result, there is an important dependence between the load current value and the conduction time of the main diodes. Main switches turn-off with ZVS cannot be achieved for small load current values. To overcome some drawbacks of the aforementioned soft switching techniques, this paper proposes a new simple ZVS-PWM commutation cell for a single-phase inverter. The presented circuit is illustrated in Fig. 1. This circuit discards the use of auxiliary voltage source or an input low-frequency center-tap capacitor. Also, in the proposed cell (except for the auxiliary switches), all switching devices in the ZVS-PWM single-phase inverter are turned on and turned off with ZVS. The auxiliary switches operate at ZCS turn-on and turn-off. Besides operating at constant frequency, the new ZVS-PWM single-phase inverter has no additional voltage stress on the main switches compared with the corresponding hard switching single-phase inverter. To achieve good dynamic regulation and properly gating the power switches, the sinusoidal pulsewidth modulation (SPWM)

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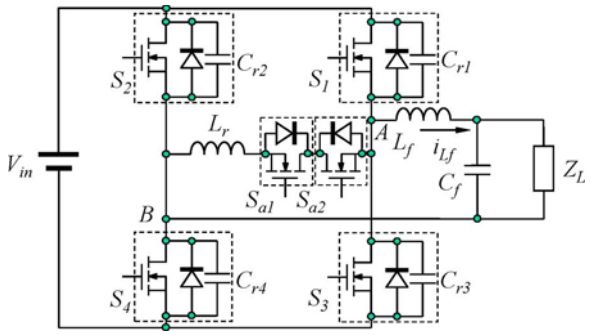

Fig. 1. Proposed ZVS-PWM single-phase inverter using a new simple ZVS-PWM commutation cell.

control strategy is designed in the proposed converter. System analysis for predicting and evaluating the inverter performance is conducted.

II. Principle of the Novel ZVS-PWM Single-Phase Inverter

The power stage diagram of the proposed ZVS-PWM single-phase inverter is shown in Fig. 1. The circuit can be divided into two sections. The first section is a conventional PWM buck inverter with bipolar voltage switching. It is composed of the switches S_1, S_2, S_3, S_4, their body diodes, and output filter L_f, C_f. This section performs the operation of the conventional PWM buck inverter with bipolar voltage switching. The second section is the proposed new simple ZVS-PWM commutation cell, composed of S_a1, S_a2, L_r, C_r1, C_r2, C_r3, C_r4, which are rated for a small power when compared to the output power. This section is synchronous with the circuit of the first section. It provides the ZVS on all semiconductors in the PWM buck inverter with bipolar voltage switching. To simplify the analysis, it is assumed that the proposed ZVS-PWM single-phase inverter is operating in the kth switching period and the following assumptions are made during one switching cycle.

1) All components and devices are ideal.
2) The output filter inductance L_f is large enough to assume that the output current I_Lfk is constant during the kth switching period.
3) Input voltage V_in is constant.
4) During the kth switching period, the resonant voltages $v_\mathrm{Cr1}(t)$ and $v_\mathrm{Cr4}(t)$ equal zero, the resonant voltages $v_\mathrm{Cr2}(t)$ and $v_\mathrm{Cr3}(t)$ equal V_in, and the resonant current $i_\mathrm{Lr}(t)$ equals zero.

Based on these assumptions, circuit operations in one switching cycle can be divided into eight stages. The eight dynamic equivalent circuits of the novel ZVS-PWM single-phase inverter during the kth switching period are shown in Fig. 2. The ideal relevant waveforms of the novel ZVS-PWM single-phase inverter are shown in Fig. 3.

A. Stage of Operation of the New ZVS-PWM Single-Phase Inverter

STAGE 1 [Fig. 2(a)— $t_0 < t < t_1$]: Before $t = t_0$, the switches S_2 and S_3 maintain turn-off state, and the switches S_1 and S_4 maintain turn-on state. The input dc voltage source V_in supplies the output stage composed of output filter L_f, C_f, and the load Z_L. This stage begins when S_a1 turns on with ZCS at $t = t_0$. The resonant inductor L_r charges linearly from input dc voltage source V_in. The resonant current $i_\mathrm{Lr}(t)$ is increased linearly. The stage ends when the predecision time $\Delta t_1 = t_1 - t_0$ is completed and the switches S_1 and S_4 turn off with ZVS at $t = t_1$. The resonant current $i_\mathrm{Lr}(t)$, voltages $v_\mathrm{Cr1}(t)$, $v_\mathrm{Cr2}(t)$, $v_\mathrm{Cr3}(t)$, and $v_\mathrm{Cr4}(t)$ can be respectively described as

$$i_\mathrm{Lr}(t) = \frac{V_\mathrm{in}}{L_\mathrm{r}}(t - t_0) \tag{1}$$

$$v_\mathrm{Cr1}(t) = v_\mathrm{Cr4}(t) = 0 \tag{2}$$

$$v_\mathrm{Cr2}(t) = v_\mathrm{Cr3}(t) = V_\mathrm{in}. \tag{3}$$

STAGE 2 [Fig. 2(b)— $t_1 < t < t_2$]: During this stage, the ZVS-PWM commutation cell performs resonance behavior. The resonant inductor L_r resonates with the resonant capacitors C_r1, C_r2, C_r3, and C_r4. The resonant current $i_\mathrm{Lr}(t)$ increases and then decreases when it reaches its peak value. The resonant voltages $v_\mathrm{Cr1}(t)$ and $v_\mathrm{Cr4}(t)$ are increased. The resonant voltages $v_\mathrm{Cr2}(t)$ and $v_\mathrm{Cr3}(t)$ are decreased. The voltage $v_\mathrm{AB}(t)$ is also decreased. The stage is finished when the resonant voltages $v_\mathrm{Cr2}(t)$, $v_\mathrm{Cr3}(t)$ drop to zero and the resonant voltages $v_\mathrm{Cr1}(t)$ and $v_\mathrm{Cr4}(t)$ reach V_in. The resonant current $i_\mathrm{Lr}(t)$, voltages $v_\mathrm{Cr1}(t)$, $v_\mathrm{Cr2}(t)$, $v_\mathrm{Cr3}(t)$, and $v_\mathrm{Cr4}(t)$ can be respectively described as

$$\begin{aligned} i_\mathrm{Lr}(t) &= i_\mathrm{Lr}(t_1)\cos\omega_\mathrm{r}(t - t_1) - I_\mathrm{o}\left(1 - \cos\omega_\mathrm{r}(t - t_1)\right) \\ &\quad + \frac{V_\mathrm{in}}{Z_\mathrm{o}}\sin\omega_\mathrm{r}(t - t_1) \end{aligned} \tag{4}$$

$$\begin{aligned} v_\mathrm{Cr1}(t) &= v_\mathrm{Cr4}(t) \\ &= \frac{V_\mathrm{in}}{2}\left(1 - \cos\omega_\mathrm{r}(t - t_1)\right) \\ &\quad - Z_\mathrm{o}\left(I_\mathrm{o} + i_\mathrm{Lr}(t_1)\right)\sin\omega_\mathrm{r}(t - t_1) \end{aligned} \tag{5}$$

$$\begin{aligned} v_\mathrm{Cr2}(t) &= v_\mathrm{Cr3}(t) \\ &= \frac{V_\mathrm{in}}{2}\left(1 + \cos\omega_\mathrm{r}(t - t_1)\right) \\ &\quad + Z_\mathrm{o}\left(I_\mathrm{o} + i_\mathrm{Lr}(t_1)\right)\sin\omega_\mathrm{r}(t - t_1) \end{aligned} \tag{6}$$

where

$$\omega_\mathrm{r} = 1/\sqrt{C_\mathrm{r}L_\mathrm{r}} \tag{7}$$

$$Z_\mathrm{o} = \sqrt{\frac{L_\mathrm{r}}{C_\mathrm{r}}}. \tag{8}$$

STAGE 3 [Fig. 2(c)— $t_2 < t < t_3$]: During this stage, because the resonant voltages $v_\mathrm{Cr2}(t)$ and $v_\mathrm{Cr3}(t)$ equal zero, this instant is the best time to turn on switches S_2 and S_3 at ZVS. The energy stored in resonant inductor L_r is delivered back to the dc source. The resonant current $i_\mathrm{Lr}(t)$ is decreased linearly. The input dc voltage source supplies the output stage by $-V_\mathrm{in}$. This stage ends when the resonant current $i_\mathrm{Lr}(t)$ drops to