Characterization of Substrate Noise Impact on RF CMOS Integrated Circuits in Lightly Doped Substrates

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Abstract – Analog and RF circuit performance in single-chip transceivers can severely suffer from coupling of digital switching noise to the silicon substrate. To predict this performance degradation, a deeper understanding of the impact of substrate noise is absolutely necessary. Using measurements, this impact is studied as the cascade of an attenuation through the substrate from the source of substrate noise to the RF circuit and the propagation through the RF circuit to its output. This approach has been validated with measurements on a 0.25 \( \mu \)m and a 0.18 \( \mu \)m CMOS low-noise amplifier (LNA) and reveals insight in the mechanisms of impact of substrate noise on RF circuits. In addition, impact of a real digital circuit is measured on a 0.18 \( \mu \)m differential CMOS LNA.

I. INTRODUCTION

A single-chip implementation of a transceiver would be a cost-effective solution for many wireless applications. However, it sets additional requirements on the architecture of the RF part. For example, to avoid the use of components that are difficult to integrate (e.g. RF bandpass filters) direct downconversion instead of superheterodyne is used. Another important requirement is that the transceiver analog and RF parts are not too much disturbed by the switching activity of its digital part: the digital switching noise (generated by the digital part) couples to the common substrate, propagates through it to the analog and RF circuits and can severely degrade their performance. With today’s ever-decreasing transistor sizes and supply voltages, latch-up becomes very hard to occur and highly doped (low-ohmic) substrates with an epitaxial layer are replaced by cheaper lightly doped (high-ohmic) substrates. For these lightly doped substrates less has been reported on substrate noise coupling \([2,3]\) than for the highly doped substrates \([1]\). Moreover, the few experimental studies published on the performance degradation of analog/RF circuits due to substrate noise concentrate mainly on highly doped substrates \([4]\). In order to help RF designers protect analog circuits against substrate noise (by using guard rings, physical separation, etc.), a good understanding of both noise propagation and impact on RF circuits in lightly doped substrates is mandatory. In this document, both propagation and impact are studied using measurements. The performance degradation due to substrate noise is studied as the cascade of an attenuation through the substrate from the source of noise to different sensitive parts of the RF circuit and the propagation through this RF circuit to its output. This approach gives insight in the mechanisms of substrate noise impact on RF circuits.

Section II describes our experimental approach for investigation of substrate noise impact on RF circuits. Section III and IV discuss measurement results on substrate noise propagation and substrate noise impact on two CMOS LNAs, respectively. Section V gives a brief overview of our future work. In section VI first conclusions are drawn.

II. EXPERIMENTAL APPROACH

In a lightly doped substrate, the impact of a substrate noise signal on an RF circuit depends mainly on four aspects: the propagation distance between the noise source and the circuit, the orientation of the circuit, the layout of the circuit, and the functionality of the circuit. To study these different aspects, a 0.25 \( \mu \)m and a 0.18 \( \mu \)m CMOS test chip with a 20 \( \Omega \)cm substrate have been designed and measured. The 0.25 \( \mu \)m test chip contains structures to measure the attenuation experienced by a noise signal propagating through the substrate over three different distances. To investigate the influence of layout, the 0.18 \( \mu \)m testchip contains structures to study propagation over two additional distances with and without a digital circuit in the transfer path.

The LNA is used as a test circuit to study the impact of substrate noise on an RF bandpass circuit. The 0.25 \( \mu \)m and 0.18 \( \mu \)m chips contain a single-ended and a differential LNA, respectively. The substrate underneath these LNAs can be excited via an external contact. The propagation of noise from a noise source to the LNA output is studied as the cascade of an attenuation through the substrate from the source of substrate noise to different parts of the LNA and the propagation through it to its output. A digital circuit is placed...
on the same chip as the differential LNA to measure the influence of real digital switching noise on its performance. The following paragraphs resume measurement results on noise propagation in a 20 Ωcm substrate (Section III) and substrate noise impact on two CMOS LNAs (Section IV).

III. STUDY OF SUBSTRATE NOISE PROPAGATION IN A LIGHTLY DOPED SUBSTRATE

Increasing the physical separation between a noise source and its victim, in a highly doped substrate, provides no additional attenuation of substrate noise after ca four times the lightly doped epi-layer thickness (= e.g. 30 µm) [1]. The substrate can be considered as one single node, which simplifies the study of substrate noise impact. Investigation of impact in a lightly doped substrate is far more complicated because of the large distance dependent attenuation experienced by substrate signals.

The propagation of signals through the substrate is studied by means of two sets of structures. A first set [Fig. 1(a)], designed in a 0.25 µm CMOS twin-well technology, consists of substrate contacts placed 250 µm, 500 µm and 750 µm from each other. Pads are foreseen to probe the structures with two ‘Ground-Signal-Ground’ (‘GSG’) probes. Large metal lines composed of all five metal layers available in the technology, connect the grounds of both probes. Signals propagating through the substrate may be very weak, even comparable to the crosstalk level between probes. Hence, the calibration prior to the actual measurement may require a compensation for this crosstalk. To allow for crosstalk compensation when necessary, calibration structures have been added on the chip for the three distances over which propagation through the substrate is measured.

The measured resistance as a function of distance for both sets of measurement structures is shown in figure 2. The resistance drops to values between 500 Ω and 1 kΩ due to the p-well present in this technology but is still high and clearly depending on distance. Hence the attenuation by the substrate cannot be neglected when studying substrate noise impact on a RF circuit.

The frequency dependence of the propagation of signals through the lightly doped substrate is studied using S-parameter measurements. Layout is observed to greatly influence transfer of signals through the substrate. Grounded metal regions, on top of the field oxide, drain noise signals to the ground via capacitive coupling. Because of the lightly doped nature of the substrate, the coupling to and propagation through grounded metal lines is no longer negligible compared to the transmission through the substrate. It is interesting to note that measurement of the influence of layout on propagation is complicated by the fact that the layout of the measurement structure itself influences the measurement.

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Figure 3 shows $S_{21}$ measured over 250 µm, 500 µm and 750 µm distances (using the structures of Fig. 1(a)). It can be observed that the metal lines connecting the ground pads on chip introduce an important capacitance to ground. The higher the frequency of the substrate signal the more it couples capacitively to the grounded metal lines, giving rise to a decrease of $S_{21}$. 

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A substrate noise signal can impact a RF circuit via its transistors (via their back gate, modeled by $g_{amb}$) and via capacitive coupling to inductors, resistors and capacitors in the circuit. The low noise amplifier (LNA) is used as a first test circuit to study the impact of substrate noise on a RF bandpass circuit. This impact problem is simplified to a linear phenomenon. It is studied as the cascade of the attenuation through the substrate from the source of substrate noise to different entry points (transistors, capacitances, inductors) in the LNA and the propagation from each entry point through the LNA to its output.

A. Substrate Noise Impact on a 0.25 µm Low Noise Amplifier

A first LNA was designed in a 0.25 µm CMOS twin-well technology. It has a gain of 14 dB at 6 GHz [Fig. 5(b)]. The most important entry point for noise coupling in the LNA is suspected to be situated close to its input. This was found out of the combination of the following three S-parameter measurements:

- the propagation from a substrate contact at approximately 250 µm from the LNA, to a bonding pad close to the input of the LNA [Fig. 5(a)]
- the transfer function from the LNA input to the output [Fig. 5(b)]
- the total transfer function, from the substrate excitation to the LNA output [Fig. 5(c)]

In terms of the peak gain and frequency at which this peak occurs, it can be seen that the addition (in dB) of the two first measurement results [Fig. 5(d)] agrees well with the third one [Fig. 5(c)]. This indicates that in this circuit the main entry point for substrate noise is close to the LNA input.
B. Substrate Noise Impact on a 0.18 µm Low Noise Amplifier

The second, differential LNA was designed in a 0.18 µm CMOS twin-well technology. It has a gain of 8 dB @ 5 GHz and a noise figure of 3.5 dB.

The dominant entry points in the 0.18 µm LNA are studied as was done for the 0.25 µm LNA. A sinusoidal signal, with frequency varying from 2 GHz to 8 GHz, is injected into the substrate at two different locations with respect to the LNA: close to the input of the LNA (Fig. 7(a), (1)) and close to the output of the LNA (Fig. 7(a), (2)). The resulting spectrum is measured at the LNA output both when the LNA is turned on and off. The ratio of the power at the LNA output to the power at the substrate input is plotted in function of frequency in figure 6.

It can be concluded that when a substrate noise source is located close to the input of the LNA, coupling to the circuit will dominantly occur via components situated in the input stage of the LNA. The coupled noise signal will then be amplified like regular input signals. This is confirmed by the fact that when the LNA is turned off the output power is reduced with up to 20 dB around 5 GHz. Very few substrate noise power will couple to components located at the output of the LNA because they are highly attenuated when traveling through the substrate to the LNA output region. Substrate noise injected close to the LNA output couples dominantly to components in the output stage. The power measured at the output remains unchanged whether the LNA is turned on or not. A noise signal close to the output will thus not be amplified by the LNA.

A digital circuit is placed on the same chip as the 0.18 µm LNA to measure the influence of switching noise on its performance [Fig. 7(a)]. The digital circuit is composed of a 20-bit Pseudo-Random-Binary-Sequencer (PRBS) followed by a cascade of two IQ modulators and demodulators [Fig. 7(b)]. The operation frequency can be chosen from DC to 130 MHz. The clock and reset signals have a rise / fall time of 0.8 nsec and toggle from 0 V to 1.8 V. The power consumption during operation at 130 MHz is 128 mW.

This paragraph presents results for a clock frequency of 130 MHz. The spectrum of the substrate noise produced by the digital circuit, measured at a substrate contact located close to the LNA, contains contributions at the clock frequency and its harmonics [Fig. 8]. The power of the harmonics in the LNA bandpass region is small compared to the power at the clock frequency and its low frequency harmonics, hence one can predict that direct coupling of these high frequency harmonics will have a small impact on the differential LNA.

The output spectrum of the 0.18 µm LNA was measured for a sinusoidal input signal of –50 dBm and –20 dBm at 5.1 GHz. This paragraph discusses measurement results for an input power of –50 dBm, with and without digital circuit operation, shown in figures 10 and 9 respectively. Only direct coupling
of substrate noise is seen above a noise floor of −100 dBm when the digital circuit is operated [Fig. 10]. No intermodulation is measured between the clock frequency or its harmonics and the LNA input signal. Substrate noise appears at the clock frequency and its harmonics. The highest harmonic seen in the LNA output spectrum is the 32nd located at 4.16 GHz. No harmonic reaches as high as the LNA operation band, and hence no degradation takes place. The power of the input signal has no influence whatsoever on the impact of the direct coupled noise on the LNA. Substrate noise impact on this 5 GHz LNA is avoided thanks to the use of a lightly doped substrate in combination with a differential topology and a metal groundplane under the circuit interconnect and pads. This was not the case for the differential 1.5 GHz LNA processed in a highly doped technology, reported by Min Xu et al. [4].

![Figure 8](Image)

**Fig. 8.** Frequency distribution of the substrate noise measured at a substrate contact next to the LNA.

![Figure 9](Image)

**Fig. 9.** Spectrum measured at the output of the LNA when the digital circuit is off.

This 1.5 GHz LNA was much more vulnerable to substrate noise impact for two main reasons. First, the direct-coupled noise power around 1.5 GHz (produced by a digital circuit with a clock frequency around 100MHz) is much higher than it is in the 5 GHz region. Secondly, the highly doped substrate hardly attenuates the noise. We can conclude that several factors have to be taken into account when predicting the impact of substrate noise on a RF band-limited circuit: the frequency distribution of the substrate noise, the attenuation by the substrate (including layout), and the circuit topology.

![Figure 10](Image)

**Fig. 10.** Spectrum measured at the output of the LNA when the digital circuit is on.

### V. PERSPECTIVES

An investigation of substrate noise impact will be performed on two other crucial RF transceiver circuits: a mixer and a voltage controlled oscillator.

### VI. CONCLUSIONS

In the design of single-chip wireless transceivers the substrate noise, caused by digital switching activity, can severely degrade the performance of RF circuits. To help RF designers protect analog and RF circuits against substrate noise both noise propagation and substrate noise induced RF performance degradation in lightly doped substrates are investigated using measurements. A study method has been developed that decomposes the signal seen at the output of an RF circuit into an attenuation part between the noise source and entry points in the circuit, and a propagation part from the different entry points to the circuit output. This approach, which is verified experimentally with a 0.25 µm and a 0.18 µm LNA, reveals insight in the mechanisms of substrate noise impact on RF circuits. Measurements of the impact of a real digital circuit on a 0.18 µm LNA show that the impact of substrate noise on RF band-limited circuits depends mainly on three aspects: the frequency distribution of the substrate noise, the attenuation by the substrate (including layout), and the circuit topology.

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