Large-Scale, High-Resolution Data Acquisition System for Extracellular Recording of Electrophysiological Activity

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Abstract—A platform for high spatial and temporal resolution electrophysiological recordings of in vitro extracellular activities concerning MEAs handling 4096 electrodes at a full frame rate of 8 kHz is presented and validated by means of cardiomyocyte cultures. Based on an active pixel sensor device implementing an array of metallic electrodes, the system provides acquisitions at spatial resolutions of 42 µm on an active area of 2.67 mm × 2.67 mm, and in the zooming mode, temporal resolutions down to 8 µs on 64 randomly selected electrodes. The low-noise performances of the integrated amplifier (11 µVrms) combined with a hardware implementation inspired by image/video processing concepts enable high-resolution acquisitions with real-time preprocessing capabilities adapted to the handling of the large amount of acquired data.

Index Terms—Active pixel sensor (APS), cardiomyocytes culture, electrophysiology, extracellular recording, high density, high spatiotemporal resolution, microelectrode array, real-time processing.

I. INTRODUCTION

LONG-TERM monitoring of electrogenic cells has become available with the emergence of microelectrode arrays (MEAs) in the 1970s [1] and early 1980s [2], [3]. Mapping capabilities of MEAs combined with imaging and cell manipulation are extensively exploited in order to develop new experimental models for the study of dynamics and propagation effects in cardiomyocyte cell assemblies [4] as well as for the unraveling of population coding [5], activity patterns [6], [7], plasticity [8]–[11], and for alternative pharmacological testing [12] on either dissociated neuronal cultures or brain slices [8], [13]–[15].

Commercially available MEA systems feature sampling rates up to 50 kHz, noise levels lower than 3–5 µVrms, and integrate typically 60–120 microelectrodes of 10–30 µm in diameter with pitches in the order of hundreds of micrometers. Assuming average cardiomyocyte cell lengths in the order of 60 µm, observations of subcellular propagation effects cannot be achieved with current electrode densities. Furthermore, with typical neuron soma dimension in vertebrates of a few micrometers and typical neuronal networks of 10 000–50 000 neurons, the limited number of electrodes and their rather large pitch results in a substantial spatial undersampling of the overall network activity. The development of MEA systems featuring a higher spatial resolution while preserving adequate noise and sampling performances is thus a prerequisite for improving both the subcellular resolution capabilities in cardiomyocyte cultures and the statistical activity representation of organized neuronal populations.

Among different strategies to upgrade the spatial resolution of MEAs, that based on CMOS devices presents several advantages for managing a large number of electrode channels interconnections, multiplexing, amplification, and filtering, and was initially investigated for in vivo neuroprobes [16] and later for in vitro devices [17]–[21]. Specifically addressing the high spatial resolution for in vitro devices, two main approaches of densely integrated electrode arrays [19] and field-effect transistor (FET) arrays [20] were reported. In the latter FET-based approach, spatial resolutions down to 7.8 µm were recently achieved on arrays of 128 × 128 elements. As yet, the temporal resolution of 2 kHz full frame rate and up to 8 kHz on smaller areas and a noise level of 250 µVrms do not measure up to that of conventional MEA systems [22]. The second aspect in developing high spatial resolution MEAs concerns the data acquisition system that, in its current standard format (channel by channel addressing), is inadequate. The implementation of the real-time signal processing thus becomes essential for handling of the large amount of data resulting from the thousands of parallel recording sites. A recently reported hybrid approach implementing an external application-specific integrated circuit (ASIC) amplification chip for 512 electrodes [23] is not, in our opinion, an effective solution for arrays of several thousands of electrodes.
In our study, we have implemented an active pixel sensor (APS) concept CMOS design to realize high-density APS–MEAs featuring a $64 \times 64$ array of $20 \mu m \times 20 \mu m$ electrodes separated by $40 \mu m$ [24]. Here, we report on the implementation and validation of a complete electrophysiological recording platform, consisting of an APS–MEA device and an acquisition system with real-time signal and data processing capabilities based on architectural ideas from the image/video acquisition field.

Section II describes the main concepts, requirements, and specifications for the high-density acquisition platform. In particular, a bimodal multilevel activity imaging feature for zooming the acquisitions from the macroscale to the microscale of the electronic cell network is introduced. This enables recordings with both high spatial and temporal resolutions on large active areas of several thousands of electrode channels and acquisitions at even higher sampling rates for zoomed regions. Section III addresses the implementation of the real-time acquisition platform. Finally, experimental results (Section IV) characterizing the system and validating the approach under culture conditions are presented and discussed.

II. SYSTEM SPECIFICATIONS

A. APS–MEA

The APS–MEA comprises $64 \times 64$ electrodes arranged as an array of pixel elements. The electrode size is $20 \mu m \times 20 \mu m$ since this dimension turned out to be a good tradeoff between the spatial resolution requirement and the microelectrode performances [25]. The distance between electrodes is $20 \mu m$, so that an area of $40 \mu m \times 40 \mu m$ is available underneath each electrode for basic in-pixel analog processing as enabled by commercial CMOS processes. The overall active area of the electrode array is $2.56 \times 2.56 \ mu m^2$, which results in an electrode density of $2500$ electrodes/mm$^2$. This is worth noting that typical cell densities in cortical cultures range from $500$ to $2500$ cells/mm$^2$, resulting in a good theoretical match between number of neurons and available electrodes [7].

B. Data Acquisition Platform—Real-Time Signal Processing

A two-order-of-magnitude increase of the number of recording sites with respect to the number of passive sites available in conventional MEAs entails severe constraints toward the mining and analysis of the recorded data. It is therefore imperative to integrate sufficient resources in the system in order to perform signal processing tasks. Nonidealities (i.e., drifts and offsets) of the APS–MEA compromise efficient signal analysis tasks at later stages. Hence, it is necessary to perform signal enhancement, such as filtering, prior to applying further analysis. Filtering of 4096 channels in real-time needs an outstanding speed performance in the involved processing blocks, and only hardware-implemented functions (i.e., field-programmable gate array (FPGA)) can meet these stringent requirements. More advanced analysis tasks such as spike detection and sorting and classification can be handled on dedicated processing units [reduced instruction set computers (RISC), digital signal processor (DSP)]; however, their implementations will not be addressed in detail in this paper.

In our approach, we manage data by implementing concepts originally developed for image/video processing. Briefly, instead of acquiring a parallel set of one-dimensional signals along the amplitude versus time quantities, the main idea behind the system organization, and that is reflected by the hardware implementation and signal handling, consists in representing the electrophysiological data as time sequences of images. This image acquisition concept stems from the optical sensing field related to widely known image sensing technologies based on APS [26]–[29].

In order to provide the capability of acquiring signals from different types of electrogenic cells characterized by different amplitudes, the dynamic range of the system needs to be very high. On one hand, typical signal amplitudes of dissociated cortical neurons from rats are in the order of $100 \mu V_{pp}$. On the other hand, signals up to several millivolts are obtained from cardiomyocytes cultures. Therefore, a programmable gain has to be implemented for adapting the acquisition system to this wide amplitude range. The sensitivity of our system will be given by the minimum noise floor that can be achieved. The noise performance of CMOS circuits is directly related to the available area and power consumption. Due to the high-resolution requirement, both area and power consumption are very limited. Preliminary circuit-level simulations of $0.35 \mu m$ CMOS-based amplifiers showed that an input-referred noise floor of $15 \mu V_{rms}$ can be achieved under the defined area constraints and with a maximum current consumption of about $5 \mu A$ per pixel element. Given the power supply at $3.3 \ mV$ and the minimum and maximum signal amplitudes, i.e., $100 \mu V_{pp}$ and $2 mV_{pp}$, respectively, the minimum and maximum gain of the system can be determined.

Another key feature of the proposed system is the bimodal imaging capability, i.e., full-frame and zoomed modes, for enhancing the correlation and the investigation of signal propagation at the macroscale and at the microscale of the cellular network circuitry. The sampling rates for these two modes have to target a sufficient temporal resolution for performing efficient spike detection at the full frame level and even provide higher frequencies for microscale propagation analysis. Upon evaluation of both aspects on custom-designed passive MEAs with high-density electrodes integrated in small areas [24], a 12-bit analog-to-digital (AD) conversion with a global sampling rate of $10 \ kSamples/s$ in the full-frame mode and a minimum sampling rate of $20 \ kSamples/s$ in the zooming mode were defined. A bandwidth requirement of $490 \ MHz$ results from the specifications of the analog-to-digital converters (ADCs) and the spatiotemporal resolution.

III. SYSTEM IMPLEMENTATION

A. Architecture

The front end of the system thus consists of the APS–MEA featuring an array of electrodes with corresponding amplification, addressing, and multiplexing functionalities. The location of each electrode is precisely defined in terms of row and column
indexes, and all the electrodes are subsequently multiplexed on one or several parallel output channels. It is this on-chip multiplexing that enables the readout of a large number of channels without being limited by the electrode interconnections and therefore, leads to the implementation of large-scale and dense electrode arrays for high spatial resolution.

The multiplexing of numerous electrodes on one single output entails stringent requirements with respect to the bandwidth along the critical paths of the integrated circuit. Therefore, in order to relax these requirements, the signals of 4096 electrodes are multiplexed on 16 parallel analog output channels (i.e., 256 electrodes per channel). The complete architecture of the acquisition system is shown in Fig. 1. The 16 analog output channels from the APS–MEA are externally sampled by a bank of ADCs. The different outputs are sent to an FPGA through a serial interface internally provided by the ADCs. The FPGA is both the control and timing device of the APS–MEA and of the bank of ADCs, since the addressing of the electrodes has to be synchronized with the AD conversion. The interface between computer and FPGA is bidirectional, so that control data can be sent from the user interface, which allows for a high flexibility in the configuration of the hardware and of the experimental settings.

Preprocessing such as filtering is performed on the same FPGA. The data are then multiplexed to a high-speed interface and sent to the peripheral component interconnect (PCI) frame grabber containing a dedicated image processor that can be used for spike detection. Thereafter, the processed data are buffered on the frame grabber and subsequently sent to a hard drive by a PCI bus. It is important to note that the general-purpose CPU of the host computer only controls the setup configuration and the visualization of data, and is not included in the real-time chain. This architecture, stemming from high-speed camera systems, enables efficient preprocessing (i.e., real-time filtering; see Section III-D) of the data at the hardware level (FPGA). The preprocessing will be, in future, followed by implementations of higher level functions, such as wavelet-based signal compression [30], spike detection [31], spike sorting [32], and classification on either the FPGA or the image processor (RISC) of the frame grabber.

B. APS–MEA

For high-sensitivity systems that have to reliably record signals in the range of 100 $\mu$V, it is imperative to maximally reduce the noise contributions. Preamplification of the signals at the very beginning of the acquisition chain is essential in order to be more robust to the noise contributions of subsequent stages and to on- and off-chip noise coupling over the interconnection paths. Therefore, the APS–MEA consists of an array of pixel elements that comprise each an electrode, a preamplifier, and a set of electronic components to bias and address the pixel (Fig. 2). The major contribution to the total noise power density function in the signal chain is given by the thermal and flicker noise of the preamplifier stage [33], [34]. Flicker noise power density of the transistors in the amplifier is inversely proportional to the product of their lengths and widths [35], and thus, directly related to the area of the pixel element. In-pixel low-pass filtering could limit the total noise power at the output of the system [21]; however, again the tight area constraints due to the high spatial resolution requirement do not allow for an efficient and well-controlled filter implementation for the required frequency bands. Nevertheless, some inherent low-pass filtering characteristic in the pixel can be obtained by connecting a capacitor between the outputs of the two input transistors of the first differential amplifier (see Fig. 2).

The multiplexing of 256 electrodes on one channel increases proportionally the bandwidth requirements of the channel signal path. The bandwidth of the multiplexed channels has to be at least the bandwidth of one individual pixel multiplied by the number of multiplexed electrodes. However, sampling of each channel will substantially alias high-frequency noise into the signal band, and therefore, considerably degrade the overall noise performance, since the sampling frequency is only a fraction of the channel bandwidth [20]. Consequently, the total effective noise increases. One way to reduce noise aliasing is to limit the maximum bandwidth per channel, or equivalently, the number of pixels multiplexed on one channel. This consists of dividing the entire array into a number of smaller zones, each one having its own output channel. The current circuit implementation with 16 output channels was found to be a good
tradeoff between bandwidth limitation and increasing external routing complexity.

The in-pixel circuitry implements an amplification stage with a gain of 40 dB within the electrode element in order to mask the noise of subsequent stages. Moreover, a calibration stage was included in the pixel to limit the effects of dc offsets arising from the dynamic electrochemical equilibrium at the electrode–electrolyte interface, which could saturate the following analog processing blocks. Due to limited pixel area a capacitive ac coupling in the signal path was not feasible. Therefore, to solve this offset problem, a dc-coupled architecture was chosen. Consequently, a dc offset compensation circuitry within the electrode element [36] is required and is implemented in our device by an auto-zeroing structure, based on a sampled feedback (SW \textsubscript{AZ1} in Fig. 2). During operation, a calibration sequence (SW \textsubscript{AZ1} and SW \textsubscript{AZ2} closed) lasting 4 \( \mu s \) is used for resetting the input to a defined potential that is equal to the electrolyte potential, and which sets the feedback to its appropriate dc value. At the end of the calibration sequence the feedback path is opened and the sampling capacitor \( C_{AZ} \) holds the corresponding value. However, due to leakage currents in the capacitor, ambient light, and temperature changes, the sampled potential drifts and the in-pixel circuit has to be regularly recalibrated. The lower cut-off frequency of the signal band can be set according to the frequency of calibration. Under standard operation, a typical calibration period of 1–2 s is sufficient.

Still at the pixel level, a global shutter is integrated for providing synchronous sampling of all the electrodes. The amplification of the signal chain is completed by a programmable column amplifier, which allows to set a total gain of 52, 64, 70, or 76 dB, respectively, and to adapt the gain to signals from different cell cultures. Besides the nominal bias currents and in order to have additional tuning capabilities, different programmable bias currents for the in-pixel amplifier, read-out amplifier, and output amplifier were implemented.

C. Acquisition Platform

The acquisition platform is implemented in two physically separated but linked parts, namely: 1) an FPGA-based (Cyclone, Altera) board and 2) an image frame grabber with on-board RISC processor.

The FPGA board acts as a controlling and processing device. The 16 output channels are each sampled by a 12 b ADC. Each output channel is conveying the signals from 256 multiplexed electrodes. In order to achieve a frame rate of 10 kHz, the ADCs are required to operate at 2.56 MSample/s per channel. We chose a 3-MSample/s ADC component from Analog Devices with integrated serializer to maximally reduce the number of interconnections to the FPGA. The basic tasks implemented on the FPGA are the control of the APS–MEA, such as configuration and calibration (Section III-B), as well as the control and timing of the addressing and the ADC sampling. Configuration data are sent from the user interface software running on the host computer to the FPGA board. The control tasks implemented on the FPGA (20 k Logic Elements, 290 kb RAM) take about 2 k logic elements. The remaining 90% of the resources allow the implementation of a set of real-time preprocessing tasks, such as filtering (Section III-D).

After the FPGA processing, the data are further multiplexed, sent to a high-speed serializer, and transferred to the host computer by a CameraLink interface, a protocol used in the high-speed imager field. This scaleable \textit{de facto} standard [37] allows downlink rates of up to 2 Gb/s on a set of four parallel low-voltage differential signaling (LVDS) data lines. Complementary to these data lines, the clock is also sent on a separate channel. Therefore, simple receivers/deserializer can be used at the back end of the transmission. The CameraLink protocol also provides a high-speed uplink and a bidirectional low-speed serial interface. The physical layers on the reception (RX) and transmission (TX) sides are connected through an MDR-26 (Mini D Ribbon) cable. This straightforward protocol is preferred to protocols like USB 2.0 or IEEE 1394 (Firewire) since it is well suited to the needs of efficient image-formatted data transmission. Buffers, ADCs, CameraLink serializer, and power supplies are mounted on an additional PCB plugged on the top of the FPGA board [Fig. 4(c)].

The receiver side of the CameraLink interface consists of a PCI-FrameGrabber [from Arvoo, Fig. 4(d)] connected to the host computer. This frame grabber implements a deserializer, a synchronous dynamic random access memory (SDRAM) (1 GB), and an on-board 600 MHz 64 b MIPS RISC image processor that can be used to enable another layer of computationally intensive processing tasks, such as spike detection and spike sorting.

D. Real-Time Processing Blocks

Our platform provides two blocks for real-time computation (see Fig. 1): the FPGA and the MIPS RISC image processor. Here, we present a hardware implementation of real-time filtering on the FPGA. We also emphasize the hardware solution of our application-specific preprocessing tasks that are more efficient than software-based solutions on dedicated microprocessors.

The FPGA is a Cyclone from Altera. It contains 20 060 logic elements (LE) and 64 dual-port RAM blocks (256 \( \times \) 18 b). The off-the-shelf FPGA kit used as a basis for the system also provides external static random access memory (SRAM) and SDRAM circuits. For real-time signal preprocessing of a high number of channels, the memory is one of the most critical resources. The external memory of the FPGA board does not provide adequate transfer rates (only one 32-bit write and one 32-bit read per sample), and therefore, computation is limited by the amount of on-chip RAM blocks. With the provided FPGA we can allocate 72 bits per channel.

This low number of bits can only be used to implement infinite impulse response (IIR) filters. We considered a bandpass filter in order to remove APS–MEA nonidealities and to reduce noise level. By using Matlab models, we explored ranges and dynamics required by these filters with respect to the specific needs of the signals we are dealing with. This study revealed an optimized bit usage with two separate filters for low- and high-frequency rejection. We also found that the most efficient
compromise is a first-order high-pass filter with 24-b fixed point registers, and a second-order low-pass filter with 20-b floating point registers (5 b for exponent). Here, we present the high-pass filter to remove APS–MEA nonidealities. The structure of this filter is given in Fig. 3(a). It only requires one multiplier $\alpha$. This coefficient $\alpha$ determines the ratio between cutoff frequency $F_c$ and sampling frequency $F_s$. For optimizing the FPGA resources, we decided to limit $\alpha$ to $\alpha = 1 - 2^n$ with $n = 7, 8, 9, 10, 11, \text{or } 12$. These values enable to use single bit shifters as multipliers. Possible values for $\alpha$ allow $F_c$ to lie between 1 and 10 Hz for sampling frequencies of 10 kHz (full array acquisition) and 20 kHz (zooming mode). We also added logic circuits to disconnect the filter during APS–MEA calibrations.

As the channels are electronically organized in a 256 $\times$ 16 channels matrix, registers are stored in a 256 $\times$ 320 b RAM. We then retrieve the samples and the related registers in the same clock cycle. Filtered data are then computed in a three-cycle pipelined unit. We implemented two units, so each of them computes eight channels per sampling time. Finally, data are sent and registers are updated before the next 16 channels are sampled. Fig. 3(c) shows the effect of this filter on raw acquired data with calibration steps [Fig. 3(b)]. Furthermore, the filter delays the data retrieval by 12 clock cycles (120 ns at 100 MHz).

The whole logic structure in the FPGA (including instruction decoding, signal sampling, high-pass filtering, and sending) requires 2579 LEs and 23 of the 64 internal block memory, leaving 17 480 LEs and 41 RAM blocks available for additional real-time preprocessing tasks (i.e., second-order low-pass filtering on 4096 channels). Current developments on the low-pass filter section shows that the final structure should not exceed 6000 LEs and that the most complex involved structures, i.e., pipelined 100 MHz multipliers, only require 400–500 LEs.

IV. RESULTS

A. Acquisition Platform

The APS–MEAs were fabricated in a standard 0.35 $\mu$m CMOS, four metal-layer process by Austriamicrosystems. The final circuit has a total of 88 pads, 32 out of them being dedicated to 16 signal channels provided in the form of differential analog outputs, and the remaining pads being assigned to power supply, bias, and digital control signals. The chip size is 5.3 mm $\times$ 5.5 mm. A picture of the circuit can be seen in Fig. 4(a).

The device packaging consists in mounting and wire-bonding the chips on a custom-designed printed circuit board (PCB) and affixing a glass reservoir of 16 mm in diameter and 8 mm in height, as shown in Fig. 4(b). In order to facilitate the mounting/dismounting of the device from the acquisition system and to manage the large number of connections, a custom-designed device socket was developed using Zebra strip connectors. As-fabricated and Au-postprocessed devices [38] were packaged...
and used for electrical testing and experiments under culture conditions.

B. Electrical Tests

To begin with, the acquisition system was tested without the APS–MEAs in order to: 1) check the ADC conversion and 2) verify the FPGA processing, serializing and grabbing on the host computer. For this purpose, a dummy PCB that connects a signal generator to the 16 differential channels of the acquisition system is plugged into the APS–MEA socket. By using a custom graphical user interface developed at the back end of the acquisition system, the signal is correctly acquired on the host computer as a sequence of frames and user-selected single channel amplitude–time signals can be extracted.

In the next step, the electrical evaluation of the acquisition system with the APS–MEAs was performed. The chip reservoir was filled by a 150 mM phosphate solution (pH adjusted to 7.3 with H₃PO₄) and a Pt electrode was immersed into the electrolyte for the application of external electrical signals. Different waveforms were applied and acquired with the APS–MEA system. The total gain of the signal chain was measured between 10 Hz and 100 kHz. A typical result from some selected channels is depicted in Fig. 5, showing a stable gain of about 55 dB over a bandwidth of about 5 kHz. For higher frequencies, the gain rolls off at $-20 \text{ dB/dec}$ due to the capacitor at the output of the first differential amplifier in the pixel. The low-frequency cutoff (not shown) of the autozeroing loop in the pixel directly depends on the frequency of the calibration sequence.

In order to evaluate the system sensitivity, a typical low-SNR waveform mimicking an ECG-like electrophysiological signal with an amplitude of $100 \mu V_{pp}$ was applied. The noise for an individual electrode (static operation) was measured and amounts to $11 \mu V_{rms}$. The noise level per electrode measured during full array read-out (dynamic operation) increased to $26 \mu V_{rms}$, and is mainly attributable to the aliasing of noise from higher frequency bands due to the large channel bandwidth required for the multiplexing. The implicit tradeoff between noise performance and spatial resolution was discussed in Section III-B.

A full-frame snapshot and a few extracted single channels of a typical recording captured at a frame rate of 8 kHz are shown in Fig. 6. The snapshot [Fig. 6(a)] shows an inhomogeneous pattern mainly due to varying offset levels between the pixels. In fact, component mismatch and tolerances give rise to different initial dc values and these inhomogeneities have to be corrected by the real-time data preprocessing [Fig. 6(b)], as discussed in Section III-D. The temporal resolutions were measured with a reduced number of addressed rows. A temporal resolution of $120 \mu s$ was achieved in the full array, whereas it increased up to $8 \mu s$ for a region of interest (ROI) comprising 64 electrodes.

Finally, temperature measurements of the media for the nominal bias conditions of the APS–MEA were performed as a function of time in order to verify the device suitability for biological recordings. Starting with an environment temperature of 25 °C we found that the culture media temperature stabilizes at about 29 °C after 3 min from device power-on. In parallel, a total nominal current consumption of 40 mA at 3.3 V is measured, resulting in a total power consumption of 132 mW. These low-temperature conditions and low-power performances of the device are compatible with cell culture conditions. However, for biological tests, a heating element was added to
stabilize the temperature of the culture media at 36 °C during recordings.

C. Biological Tests

Biological tests were performed with cardiomyocytes cell cultures. For this purpose, ventricular cardiomyocytes were obtained from Sprague Dawley rats at embryonic day 14–15 (E14-15) and processed as follows. Heart tissue fragments, once isolated and washed in Ca\(^{2+}\)- and Mg\(^{2+}\)-free Hank’s balanced salt solution, were incubated with 0.05% trypsin (E14-15) or 0.125% (E18) at 37 °C and exposed at two or three cycles of enzymatic digestion. The supernatant containing dispersed cardiac cells was removed after each cycle and placed into a conical centrifuge tube with a solution of nutrient medium (5% FCS, 1 mM L-Glutamine, 1% Pen-Strepto, DMEM-F12). After the last cycle of Trypsin, cells were mechanically separated in nutrient medium by repeated pipetting and centrifuged for 5–8 min at 1000 r/min. In order to separate cardiac fibroblasts from ventricular cardiomyocytes, the cells were preplated in a Petri dish, without any treatment of the adhesion factor, with nutrient medium and stored for 1 h at 37 °C in a humidified standard incubator. Finally, ventricular cardiomyocytes were collected, centrifuged, diluted in DMEM-F12 medium, 4% FBS, 2% HS, 1% Pen-Strepto, and plated onto the precoated (laminin solution at 0.01 mg/mL overnight) APS–MEAs. Three days later, the medium was replaced with a serum-free medium composed of DMEM-F12 supplemented with 1% N2.

Cardiomyocytes cultures grown on APS–MEAs showed good viability over the observed period of two weeks and their behavior was similar to reference cultures simultaneously plated on standard MEA devices. Even if the cells showed a spontaneously contractile behavior after about 48 h in vitro, we used cultures at 4, 5, and 7 DIV in the experiments in order to observe the propagation of large and clear electrophysiological signals. An example of acquired full-frame activity is illustrated
in Fig. 7 by 2-D and 3-D plots captured at three distinct acquisition times. Additionally, three electrode signals acquired at locations indicated on the 2-D plots of Fig. 7(c) are reported as amplitude–time graphs [Fig. 7(b)]. These results demonstrate how the high spatiotemporal resolution of our system enables detailed observation of the microscale propagation effects.

Of these experiments, we evaluated the propagation velocity on APS–MEAs of cardiomyocyte cultures. Because of the large number of electrodes featured by the APS–MEAs, we used a simple estimation; the velocity was evaluated considering the starting and ending points of the syncitium and the temporal gap between the two events. The calculated value of 0.14 m/s is in accordance with values measured on standard MEAs [39].

Finally, the functionality of the zoom mode is demonstrated by the results reported in Fig. 8, where an area of 384 electrodes was addressed. In this case, the temporal resolution is increased down to 18 µs.

V. CONCLUSION

In this study, we presented the specification and the design of a large-scale data acquisition platform for high spatiotemporal resolution electrophysiological activity recordings of networks of electrogenic cells. We implemented a CMOS circuit with 4096 electrodes at a pitch of 42 µm and a data acquisition system inspired by the concept of image/video acquisition and processing enabling to transmit and analyze large amounts of data. A summary of the system characteristics is provided in Table 1. Extensive hardware resources, such as FPGA and RISC units, underline the strong emphasis to enable real-time processing of the data. Real-time preprocessing has been demonstrated by a simple high-pass filter over the 4096 electrodes. Two acquisition modes operating in full array and in zoom capture modes allow monitoring cell cultures both at a high spatial resolution at the network level and a high spatiotemporal resolution at subnetwork levels. Validation of the platform on cardiomyocytes was carried out and demonstrated with the propagation of cardiac pulses across the network.

![Image](127x466 to 463x724)

![Image](318x177 to 535x379)

![Image](38x751)

Fig. 8. (a) Highlighted subset of the array selects 384 electrodes used for an increased temporal resolution acquisition. (b) Signal of one selected electrode of the recording [electrode is indicated in (a)] at a frame rate of 55 kHz. (c) Enhanced temporal resolution in the zoom mode can be achieved by reducing the number of addressed electrodes used for a fine analysis of the microscale propagation effects.

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Current study involves validating the system with neuronal cell cultures and further improving the data preprocessing and real-time visualization. The final aim is to use the system under a wide range of experimental conditions for investigating relations between local phenomena in electronic cells, such as propagation effects or synaptic changes and network characteristics, such as overall dynamics (e.g., firing rate, network bursting) and information processing mechanisms (i.e., population code) and network plasticity.

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