Charge Recycling Differential Logic (CRDL) for Low Power Application

Bai-Sun Kong, Joo-Sun Choi, Member, IEEE, Seog-Jun Lee, and Kwyro Lee, Senior Member, IEEE

Abstract—A novel logic family, called charge recycling differential logic (CRDL), has been proposed and analyzed. CRDL reduces power consumption by utilizing a charge recycling technique with the speed comparable to those of conventional dynamic logic circuits. It has an additional benefit of improved noise margin due to inherently static operation. The noise margin problem of true single-phase-clock latch (TSPC) is also eliminated when a CRDL logic circuit is connected to it. Two swing-suppressed-input latches (SSIL’s), which are introduced for use with CRDL, have better performance than the conventional transmission gate latch. Moreover, a pipeline configuration with CRDL in a true two-phase clocking scheme shows completely race-free operation with no constraints on logic composition. Eight-bit Manchester carry chains and full adders were fabricated using a 0.8 μm single-poly double-metal n-well CMOS technology to verify the relative performance of the proposed logic family. The measurement results indicate that about 16–48% improvements in power-delay product are obtained compared with differential cascode voltage switch (DCVS) logic.

I. INTRODUCTION

ENERGY efficiency has become one of the most important concerns in VLSI design. Especially in portable applications, the issue of managing power is a dominant consideration due to low energy capacity of current battery products [1], [2]. In a designer’s point of view, there are a variety of considerations that must be taken into account for low power design which include the architecture used, the style of logic employed, and the technology incorporated. Among these, choosing a proper logic style is one of the most important factors for low power since the power consumed in the arithmetic and logical units is greatly dependent on the way in which these blocks are implemented.

In many applications requiring high speed, precharged dynamic circuit techniques are preferred for timing-critical portions [3]. These circuits are usually operated by repeating the actions of precharging output nodes up to the power supply voltage (Vdd) in the precharge phase, and conditionally discharging some of them depending on the input in the evaluation phase [4]–[7]. Unfortunately, these techniques are inefficient as far as the power consumption is concerned since all the charge consumed in an evaluation phase must be resupplied during the next precharge phase. Moreover, some precharged nodes, which are not to be discharged in the evaluation phase, remain as dynamic nodes. These nodes are usually noise-sensitive sacrificing the noise margin of the circuit. If the logic state is to be preserved, additional devices are required resulting in slower speed and an increase in power. Finally, the current due to the simultaneous switching of the output nodes during precharge or evaluation phase gives rise to large di/dt noise, causing voltage bumps on the power supply and ground (Vss) rails. This noise is especially critical in the precharge phase, as all the discharged output nodes are precharged simultaneously during this phase. This creates spurious signals, and can lead to false switching if its magnitude exceeds the noise tolerance of the logic circuit.

We propose in this paper a new logic style, called charge recycling differential logic (CRDL) [8], which uses a novel precharge scheme to solve the problems in the conventional precharged dynamic circuits addressed above. Section II describes the basic circuit architecture for CRDL with some additional circuits to recover full signal swing at the output of this logic. Section III explains a timing constraint on the activation of the sense amplifier in a CRDL circuit for reliable operation. In Section IV, we show a distinct advantage when CRDL is connected together with a true single-phase-clock latch (TSPC) [9]. We further introduce novel latch structures that are best suited for CRDL. This section also includes an explanation for a race-free pipeline structure driven by a true two-phase clocking scheme. In Section V, we present simulation and experimental results for some benchmark circuits, and finally, we draw our conclusion in Section VI.

II. BASIC CIRCUIT ARCHITECTURE

The generic CRDL gate is shown in Fig. 1. It consists of two parts, a complementary output pass-transistor logic network [10], [11] with precharge circuitry and an acceleration buffer. The inputs to the pass-transistor logic network are of two types, control variables that are connected to the gates of the pass-transistors, and pass variables that are connected to the sources of the transistors [12]. The precharge circuitry consists of a cross-coupled pair of the pMOS transistors, MP1 and MP2, and the nMOS transistor MN1 which connects both the output nodes. The cross-coupled pair is used to pull one of the complementary outputs up to Vdd as the other goes down to Vss, while the nMOS transistor is used to equalize the voltages of the output nodes. The threshold voltages of the pMOS
transistors in the cross-coupled pair are made to be higher than other devices so that these transistors are nearly off when both nodes are precharged to around half the supply voltage. An acceleration buffer is attached to this circuit to increase the speed as shown inside the dashed line in Fig. 1. This is required as CRDL suffers from degraded speed performance when used in a long chain. The buffer is enabled through the input $E_i$, and the signal $E_o$ is the output to be used as $E_i$ in the next stage. Transistors MN2, MN3, and MN4 form the sense amplifier to accelerate pull-down transitions, and transistors MP3, MP4, and MN5 are used to make the enable signal for the amplifier at the next stage. Each enable signal is disabled in the precharge phase and enabled during the evaluation phase to accelerate pull-down transitions of output nodes.

As with other precharged dynamic circuits, CRDL has two phases of operation, namely, the precharge phase and the evaluation phase. In the precharge phase, the clock signal $CK$ goes high, connecting the output nodes $OUT$ and $OUT'$ to each other through the nMOS transistor MN1. Then, by the charge sharing effect, the voltage levels of both outputs become equal. Since the outputs are complementary, that is, one is always at Vdd and the other at Vss during last evaluation phase, the connection between these nodes makes the voltage level be in between the extremes. In usual cases, as the amounts of parasitic capacitance of each node are comparable, this value is close to half of the supply voltage. When this value becomes lower than the required one due to a mismatch in parasitic capacitance’s, the pMOS transistors in the cross-coupled pair turn on, and supply an additional charge to the precharge nodes making the voltage closer to one half the supply voltage. After reaching the required voltage level, these nodes experience no subsequent pull-up because the cross-coupled pMOS transistors, having higher threshold voltages, turn off immediately.

In the evaluation phase, the clock signal $CK$ goes low, separating the precharged nodes from each other. Then, depending on the applied input values, a low impedance path to ground is established at one of the two precharged nodes through the pass-transistor network, pulling down the node toward ground. As an example, let us assume that the inverting output, $OUT$, is to be evaluated low. In this case, lowering of the voltage at this node turns on the pMOS transistor MP2 in the cross-coupled pair, pulling up the node $OUT$. Then, when the enable input signal $E_i$ goes high, the transistor MN4 is turned on to activate the sense amplifier. Through the regenerative action of the sense amplifier, the node $OUT$ is pulled down quickly toward ground. As the voltage difference between the output nodes gets larger, the transistor MP4 in the acceleration buffer turns on to enable the output $E_o$ which is to be used for activating the sense amplifier at the following stage.

To interface a CRDL circuit with conventional full-swing techniques, simple circuit structures described in Fig. 2 can be used to generate a full-swing signal from the output of a CRDL circuit. The circuit in Fig. 2(a) is implemented with only two transistors driven by a pair of complementary signals, and the one in Fig. 2(c) requires an additional transistor driven by the enable signal generated in a CRDL logic block. This circuit has the same form as one stage of the TSPC latch. The outputs in both cases are precharged to Vdd when the input is around half-Vdd, and conditionally discharged when the input signal gets stable. By using duality, we can construct circuits having “zero-to-one” transition at the output nodes as shown in Figs. 2(b) and (d), respectively.

CRDL has several important advantages over conventional dynamic logic circuits. First, it uses a novel precharge scheme in which the charge used for logic evaluation in a cycle is recycled to establish a precharge value in the next cycle. Thus, CRDL consumes less power than conventional full-swing precharge circuits. In an ideal situation assuming that precise half-supply precharge level is achieved, the amount of power consumed is exactly 50% that with a full-swing technique. The charge recycling operation also reduces $di/dt$ noise on the supply lines, sometimes a critical problem in conventional circuits. CRDL uses internally stored charge to precharge its output nodes during the precharge phase, resulting in a reduction in the amount of the current from the supply, and thus, the slope of the current variation to cause this type of noise. Noise during the evaluation phase also decreases due to reduced voltage swing, resulting in smaller current to and from the supply lines. Another advantage of this logic style comes from the fact that there are no noise-sensitive dynamic nodes in the gates implemented with this logic technique. Although the operation of CRDL is based on

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**Fig. 1.** Schematic diagram of charge recycling differential logic (CRDL).

**Fig. 2.** Circuits to recover a full signal swing from the output of CRDL.
Fig. 3. Circuit model of sense amplifier for CRDL.

precharge and evaluation actions using a clock signal much like conventional precharge logic circuits, all of the evaluated nodes are connected to either supply or ground rails leading to a static operation. Therefore, it eliminates the problem which is related to dynamic node such as degraded noise margin. Finally, CRDL has the advantages of the pass-transistor logic network such as the implementation of any random Boolean functions. Moreover, some important logical functions can be implemented more efficiently using this logic circuit. For example, XOR’s can be implemented using only two pass-transistors. In CRDL, we can also eliminate devices needed only for pull-up functions in the pass-transistor network as the cross-coupled transistors in the precharge circuit perform the function instead. This type of efficient implementation is particularly important since it is a key to reducing power dissipation and increasing speed by creating logic circuits with a minimal number of devices.

III. SENSITIVITY ANALYSIS

The acceleration buffer has been used to increase the speed of a CRDL circuit. In designing the buffer, we have to consider a certain constraint on the activation time of the sense amplifier to confirm reliable operations. As far as the speed is only concerned, earlier $E_{lb}$ signal is a better choice as it gives higher performance. But, if the sense amplifier is enabled too early, it may not sense the logic states correctly leading to false output values. Thus, it must be enabled at least after a sufficient voltage difference is established at the output nodes. The earliest possible enable signal without false operation is determined by the sensitivity of the sense amplifier, which means the minimum signal difference the sense amplifier can detect correctly. The sensitivity of the sense amplifier used for a CRDL circuit depends on several factors such as the difference in load capacitance values, the mismatches in the threshold voltages, the amount of current flowing through the logic network during sensing operation. The relationship between the sensitivity and the above-mentioned factors is represented as (1) with a simplified model shown in Fig. 3

\[ S = \sqrt{K} \frac{C_0}{\beta_0} \left( A \left( \frac{\beta_1 - \beta_2}{\beta_0} - \frac{C_1 - C_2}{C_0} \right) \right)^\alpha - B \left( 1 + \frac{\beta_2 (V_H - V_{T0})^2}{\beta_0 (V_T - V_{T0})^2} - 1 \right) + |V_{T1} - V_{T2}| \]  

\( (1) \)

where

\[ C_0 = \frac{1}{2} (C_1 + C_2); \]
\[ \beta_0 = \frac{1}{2} (\beta_1 + \beta_2); \]
\[ V_T = \frac{V_{T0} + \gamma \sqrt{V_S}}{2}; \]
\[ C_{1,2} \] capacitance value at nodes N1 and N2;
\[ \beta_{1,2} \] channel conductance of devices M1 and M2;
\[ V_{T0} \] threshold voltage at 0 V source potential;
\[ K \] effective channel conductance of logic network;
\[ K \] voltage decrease speed coefficient at node Ns (V/s);
\[ A \] and \( B \) proportional constants;
\[ \alpha \] constant (between 1.1–1.2);
\[ V_p \] precharge potential at nodes N1 and N2;
\[ V_H \] logic “high” potential.

In this model, a current source is attached to the pull-down node to represent the current flowing through the logic tree to evaluate logic value of the circuit. The cross-coupled $p$MOS transistors are ignored in the model as they, which are off at the starting point of sensing operation, have no effect on sensitivity. The first term in the parenthesis and the last one in the equation are associated with mismatches in the gain factor, the load capacitance, and the threshold voltage, respectively, and are similar to the analysis in [13] except for the value of $\alpha$. The second term in the parenthesis represents the effect of the current source on the sensitivity. The current source helps improve sensitivity as it steadily draws current from the node which is to go low during sensing operation. Fig. 4 shows the computed and the simulated relationship between the sensitivity and the factors such as load capacitance and the amount of current flowing through the logic block. As shown in the figure, the minimum allowable signal difference of the sense amplifier in a CRDL circuit tends to be smaller than that used for DRAM, and can even be a negative value.

In determining the activation time of the sense amplifier, we must also consider the effect of possible delay variations of the enable signal due to process skew. Fabrication variations on driver strength of devices due to channel length/width variations and on capacitance of interconnects due to variations
in oxide thickness or interconnect width can produce variations in nominal delay of the logic gates which could cause a timing violation on the enable signal. Thus, the timing variation reflecting the worst-case process condition must be included as a margin in determining the timing of the enable signal. This is especially important for the enable signal driving more than the next stage since a long interconnect across several stages tends to have larger process variation.

With these considerations, we can choose or generate a proper enable signal from the enable output signals of the previous several stages. The aim here is to fully exploit the speed advantage of the acceleration buffer by activating the sense amplifier as early as possible without violating the timing condition stated above. In the majority of cases, the output of the previous stage can be used as the enable signal for the current stage without any timing violation. And, as far as the condition is met, the enable signal can be taken from the second or third previous stages instead of the first previous stage to get the highest possible speed. In some cases in which even the $E_o$ signal from the previous stage cannot meet the constraint, the propagation delay can be adjusted by changing the size of the transistors of the amplifier, or by inserting a proper delay element to this signal path.

IV. Latch Structure AND Clocking Strategy

A. Novel Latch Structures

The true single-phase-clock latch (TSPC) can be used as a storage element for storing output data as shown in Fig. 5. The output signal of the acceleration buffer, $E_o$, is used as the control signal instead of the clock signal. With this combination, we have an additional advantage as shown below. The TSPC has severe noise margin problem when it is used with conventional circuits. For example, the node $A$ may be tristated “high” with $OUT$ being tristated “low” by driving a logic “one” signal to the input when the latch is opaque. This maps into the case of a dynamic node driving a dynamic gate that is very sensitive to noise. Thus, a noise incurred can reduce the voltage on $A$ enough to cause a substantial leakage current through $P_2$, and change the logic state of $OUT$. This problem is well addressed in recent publication and solved by adding an additional device [14]. But, when the TSPC is driven by the output of a CRDL circuit, the node $A$ does not show the noise-sensitive behavior as above. Let us explain it briefly now. When the latch goes into the opaque state by deasserting the enable signal $E_o$, the CRDL is also in the precharge phase. Then, the input voltage for the latch is low enough to turn on the transistor $P_1$, making $OUT$ be held at $V_{dd}$ instead of being tristated. This means the transistor $P_2$ is in cutoff state preserving its output state during this period. Therefore, no such noise margin problem occurs when a TSPC latch is used with CRDL.

When a static latch is required, the traditional latch based on the transmission gate [15] can be used with the clock being replaced by the buffer output signal $E_o$ as shown in Fig. 6. With this configuration, however, the transition of the input signal during the evaluation phase is disturbed by the internal logic state at node $B$ resulting in slower speed, if the input logic state is opposite from the internal one. The internal logic value is also disturbed by the input signal level at the front stage of the precharge phase during which the enable signal is still changing. These signal disturbances are shown in upper waveforms in Fig. 8, and originated from the fact that the current for charging and discharging the internal storage node is supplied and extracted through the input node $D$ via a transmission gate. In addition, a skew inevitably occurring between the inverting and noninverting control signals can cause a signal fighting between the old and the new values at the internal storage node during the overlap period resulting in a substantial short-circuit current.

We propose, therefore, novel static latches to reduce these effects and speed up the operation with smaller power con-
sumption, and they are shown in Fig. 7. The latch in Fig. 7(a), which is a single-rail version of swing-suppressed-input latch (SSIL), is in opaque state while the enable signal $Eo$ is low, turning off the transistor MN2. During this phase, the nodes $A$ and $B$ are in "high" and "low" states, respectively, as half-Vdd precharged voltage asserted at the input nodes makes both the transistors MP1 and MN1 on. Then the transistors MP2 and MN3 are fully off, tristating the node $OUT$. Meanwhile, with the transistors MP3 and MN4 being turned on by the inverted input signal which is also precharged to half-Vdd, both the inverting and noninverting outputs are connected to each other through a cross-connected inverter preserving their states. When the inputs $D$ and $D$ get stable and go high and low to turn on and off the transistors they are driving, a new value can be evaluated without any signal fighting against the old value in the latch. As an example, let us assume $OUT$ was in logic state "zero" and $OUT$ in "one" state, turning on and off the transistors MN5 and MP4, respectively. When a new input value "one" is driven with $Eo$ being enabled, $A$ goes down and the transistor MP2 becomes active. Then, $OUT$ starts to
evaluate its new value. At this point, the transistor MN4 is off since the inverting input \( \overline{D} \) is “zero,” preventing the current to preserve the old value from flowing. The operation principle for storing the “zero” state into the latch is similar to the above one. But, in this case, it must be noted that the logic “high” level at node \( B \) is one threshold voltage less than the supply level because the logic “high” signal cannot be fully transmitted through an \( n \)-type device, MN2. This imbalances the rise and the fall times of output node. Hence, the width of the transistor MN3 must be increased up to the level of MP2 to get balanced transition times. A dual-rail version of SSIL, shown in Fig. 7(b), has similar operation and improves speed further by evaluating both the complementary outputs simultaneously. These latches have no inverted control signal as in the conventional transmission gate latch. Hence, no skew problem occurs during transitions. In addition, they have no signal disturbances because the current for charging and discharging the internal node does not come from the input node but from the supply rails. These latches require complementary inputs, but they are obtained simultaneously at no cost as CRDL naturally generates complementary signals as its outputs.

Table I summarizes the comparison results of the conventional transmission gate latch, and single- and dual-rail SSIL latches. Simulated waveforms for them are also shown in Fig. 8. The maximum operating frequencies are measured with 100 fF load at each output node, and the powers are those consumed by latches without including output loads when the circuits are operated at the frequency of 100 MHz. We note that the proposed latches show no signal disturbances at all, as is verified by the waveforms in the figure. Table I indicates that single-rail SSIL has 25% higher operating frequency with 38% less power, and the operation speed of dual-rail SSIL is almost two times faster with slightly less power as compared with the conventional latch shown in Fig. 6.

The speed advantage of SSIL can be easily understood by a close investigation into the transition operations while new data are being transferred into the latch. As explained before, when the enable signal is low the internal nodes \( A \) and \( B \) in
Fig. 12. Schematic diagram of Manchester carry-chain circuit with CRDL (Note that the threshold voltage of the cross-coupled PMOS pair is adjusted by Vbb).

Fig. 13. Schematic diagram of full adder with CRDL (Note that the threshold voltage of the cross-coupled PMOS pair is adjusted by Vbb). (a) Sum circuit. (b) Carry circuit.

B. Race-Free Two-Phase Clocking Scheme for CRDL

The pipeline connection of CRDL and the corresponding clock timing are depicted in Fig. 9. It contains two stages, the \( \Psi \) stage and the \( \bar{\Psi} \) stage. The circuit structure of the \( \Psi \) stage is the same as the schematic shown in Fig. 1 except for the first function block. The structure of the first function block will be explained later in this section. The schematic diagram of the \( \bar{\Psi} \) stage is the same as the \( \Psi \) stage with clock signal \( CK \) being replaced by \( \bar{CK} \). Each stage is precharging when the clock signal is high and evaluates its input values when the clock is low. Latch structures introduced previously in this section are used as storage elements between stages.

Another reason for higher speed is that the new latch has fewer number of transistors in series from the internal storage node to the supply or the ground rails. In conventional latch, the internal node is connected to the ground through three or more transistors in series including the pass gate in the latch, and the sense amplifier or the logic tree of the proceeding stage. In SSIL, however, the internal node is connected to appropriate rails only through MP2 or MN3, leading to an improved speed due to reduced conductive distance. The additional speed gain of the dual-rail version comes from simultaneous evaluation of logic values at both the inverting and noninverting output nodes, as previously stated. When the power consumption is concerned, the fact that the clock loads of both SSIL’s are far smaller than that of conventional latch, as listed in Table I, leads to a reduction in power because the clock signal is the busiest signal consuming the largest power. Lack of short-circuit current through MP2 and MN3 is another reason for power efficient operation of SSIL.

The output \( EO \) of each stage instead of the clock signal is used to define the time when latch inputs are to be considered valid. With this pipeline connection, when the \( \Psi \) stage is in the precharge phase, the \( \bar{\Psi} \) stage is operated in the evaluation phase, and vice versa. Fig. 10 depicts the schematic diagram of the first function block in each stage. The logic tree in the schematic is implemented using the cascode logic network with a bottom device instead of using pass-transistor logic tree. This modification results from the fact that the inputs to the first function block, which are the outputs of the latches of the previous stage, become stable when the function block is in the precharge phase not in the evaluation phase. Thus, if the pass-transistor circuit is used for the logic composition, some devices in the logic network become active and try to evaluate logic values before the evaluation phase actually starts. This results in a substantial short-circuit current through the cross-coupled pMOS pair and active devices in the logic tree, as they are simultaneously on. Meanwhile, when the circuit structure in Fig. 10 is used, any current path through the logic block established during the precharge phase is eliminated as the bottom device is off. Then, as soon as the pipeline stage goes into the evaluation phase, the bottom device becomes active and logic tree starts evaluating input logic values.

One of the major advantages of the pipeline configuration with CRDL is that it imposes no restriction to the amount of clock skew as NORA [5] does. In conventional case with transmission gate latches, these storage elements are controlled simultaneously by the clock phases, \( CK \) and \( \bar{CK} \). Thus, any overlap between these phases makes the latch stay on, resulting in an illegal flow of information. In a pipeline structure with CRDL, however, the alteration of the latch output information...
Fig. 14. CRDL implementation of 8-b carry chain. (a) Simple version. (b) Optimized version.

Fig. 15. Photomicrograph of the test chip.

is controlled by only one of the two clock phases. Although
the latch control signal is not the clock signal itself, it is
locally generated by one clock phase and the inputs which have
no relationship with the other clock phase. Therefore, CRDL
circuit technique is fully race-free regardless of any overlap
between clock phases. Even though CRDL circuit is immune
to the overlap of the clock phases, the cycle time must be
increased by the amount of clock skew as other logic circuits
do. The advantage of CRDL pipeline structure over NORA is
that it has no constraints on logic composition, increasing the
logic flexibility of the circuit. In a NORA pipeline structure,
on the other hand, there must be an even number of inversion
blocks between any two clocked CMOS(CMOS) latches [5].

V. COMPARISON AND EXPERIMENTAL VERIFICATION

To verify the performance of CRDL, current drawn from
the supply rail during transition operation is compared with
those of the conventional logic types such as DCVS [6] and
LCDL [7]. All the simulations are done at power supply
of 5 V using HSPICE for several fan-in numbers and load
capacitance values. Fig. 11(a) plots the current consumption of
the XOR/XNOR and the AND/NAND gates implemented in
each logic circuit with the fan-in number being changed from
two to eight with the load capacitance of 100 fF. Fig. 11(b)
shows the same data with changing load capacitance over
the range of 0.2–1 pF when the fanin number is two. The
propagation delays of all the logic styles for each Boolean
function are made to be the same by device sizing for each
fan-in number and load capacitance value, and are also shown
in the respective figure. From these figures, it is seen that the
current drawn by CRDL is the smallest among all the logic
circuits compared, indicating that this logic type consumes the
lowest power.

Eight-bit Manchester carry chains and full adders con-
structed of CRDL and of DCVS are designed as benchmark
circuits to verify the performance of the proposed logic circuit.
Figs. 12 and 13 show the schematic diagrams of bit-sliced
cell of the carry chain, and the full adder implemented using
CRDL, respectively. The 8-b carry chain is constructed by
cascading the carry chain cell in series as shown in Fig. 14.
The simple version is shown in Fig. 14(a) in which the
output signal $E_0$ is used at the very next stage as the
buffer enable signal $E_i$. In this case, the power is saved
approximately by 23% with almost the same speed as the
conventional one. Fig. 14(b) shows an improved version where
the interconnection of $E_0$ is modified. That is, $E_0$ of each
stage is connected up to the next fourth stage to optimize the
activation timing of the sense amplifier. With this connection,
the speed improves approximately by 35% over the simple
version without any additional power. In the conventional
DCVS Manchester carry chain, carry look-ahead technique is
used to speed up the operation. All the precharged dynamic
nodes in conventional circuits are made static using a weak
PMOS transistor [15] to supply enough current to compensate
for the leakage as well as to strengthen these nodes against
the external noise. The experimental chip for these benchmark circuits was fabricated using the 0.8 μm single-poly double-metal n-well CMOS process. Because the threshold voltage adjustment was not feasible in this process, those of the cross-coupled pMOS transistors for the CRDL were adjusted by applying back-bias voltage so the precharged value was about 3.5 V. Fig. 15 shows the chip photomicrograph of the test circuit, and Fig. 16(a) and (b) are the measured waveforms of the optimized Manchester carry chain and the full adder implemented using CRDL, respectively. Table II(a) and (b) list the number of transistors, the average power, the worst-case propagation delay, and the calculated power-delay product of each of the logic circuits. The simple and the optimized carry chain with CRDL achieve about 21 and 48% improvements in power-delay product over the circuit with DCVS, as shown in Table II(a). The measurement result of full adder, which is shown in Table II(b), indicates that the new circuit improves power-delay product 16% over the conventional circuit.

To compare the performance with static CMOS logic circuits, we list the simulation results of static full adders together with that using DCVS and CRDL in Table III. These simulations are performed at 10 MHz operating frequency including parasitic components extracted from the layout (The switching activities of static adders are around 50%). The result in the table shows that the static logic style has slightly better performance in terms of power delay product. But, it should be noted that static logic circuits have slower speed, and as a result, precharged circuit techniques are popularly used in high-speed applications due to their speed advantage although they consume larger power than the static logic [3]. Moreover, since almost all of today’s challenging low-power systems such as portable cellular telephone and notebook computers are simultaneously high-speed systems requiring many of these techniques, it is very important to reduce as much power as possible in precharge logic circuits. In this sense, CRDL circuit technique is a suitable solution for use in low-power and high-speed applications.

### VI. CONCLUSION

A new logic style called CRDL has been proposed to address the demands of current low-power high-speed VLSI systems. It improves power efficiency by utilizing a charge recycling technique with the speed comparable to conventional precharged circuit techniques. Due to inherently static operation, it improves noise margin and eliminates problems related to dynamic nodes. It also causes less ground bouncing noise as it recycles the internal charge and has smaller voltage swing as compared with the conventional precharge logic circuits. When a TSPC latch is connected to the output of a CRDL circuit, an inherent noise margin problem in the latch is eliminated without additional devices. SSIL latches, introduced in this paper, improve speed and power consumption when it is compared with the conventional latch using the transmission

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**TABLE II**

**measurement Results for 8-b Manchester Carry-Chains and Full Adders Implemented Using CRDL and DCVS: (a) Measured Carry Chain and (b) Full Adder**

<table>
<thead>
<tr>
<th>Device Count</th>
<th>Delay (nSec)</th>
<th>Power (μW@10MHz)</th>
<th>Power*Delay Product (fJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCVS</td>
<td>140</td>
<td>3.08</td>
<td>142</td>
</tr>
<tr>
<td>CRDL</td>
<td>128</td>
<td>3.17</td>
<td>109</td>
</tr>
<tr>
<td>CRDL(opt.)</td>
<td>128</td>
<td>2.08</td>
<td>109</td>
</tr>
</tbody>
</table>

**TABLE III**

**Simulation Comparison Between Static and Dynamic Full Adders**

<table>
<thead>
<tr>
<th>Device Style</th>
<th>Delay (nSec)</th>
<th>Power (μW@10MHz)</th>
<th>Power*Delay Product (fJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static CMOS</td>
<td>40</td>
<td>1.65</td>
<td>11.0</td>
</tr>
<tr>
<td>Pass-Tr.</td>
<td>48</td>
<td>1.34</td>
<td>16.0</td>
</tr>
<tr>
<td>DCVS</td>
<td>38</td>
<td>0.75</td>
<td>32.4</td>
</tr>
<tr>
<td>CRDL</td>
<td>33</td>
<td>0.90</td>
<td>22.2</td>
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</table>
gate. Moreover, a pipeline configuration implemented using CRDL and SSIL is shown to have fully race-free operation in a true two-phase clocking scheme. The performance of the proposed CRDL circuit has been verified through SPICE simulation and an experimental chip. From these results, CRDL has been shown to have a strong advantage in power consumption over the conventional circuit techniques.

REFERENCES


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