Design Platform and Tools For 3D-IC Integration

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CMP
Outline

• Introduction

• Which Design Methodology to address?

• For Which Applications?

• Design Platform features for 3D-IC

• 3D-IC automatic Place & Route

• Conclusion
Two Worlds with Different Integration Approaches

“Monolithic”
Distributing a whole system across several tiers

- 3D-IC TSV Stacked Memory
- 3D-IC face to face
- 3D-IC TSV integrated
- Multi-Chip Module
- Substrate based Module (PCB)

“Discrete”
Assembly of “Known Good Dies”

- Heterogeneous Multi layer 3D-IC TSV integrated
- Die to Die Integrated package
- Silicon Interposer to high Integrated MCM

Which Design Methodology?

- **Discrete**: 3D packaging, stacked dies, ...
  1. Design a whole system.
  2. Split it in subsystems.
  3. Place the subsystems as predefined “Known Good Dies” (IPs).
  4. Determine and place the interfaces in between.
  5. The system is done

- **Monolithic**: 3D-IC Integration
  1. Design a whole system.
  2. Split it in subsystems.
  3. Determine and place the interfaces in between.
  4. Generate and Place the subsystems in between the interfaces.
  5. The system is done

Here comes the difference: The “key” for a true 3D-IC Integration
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Industrial Applications

- There are two 3D areas that are receiving a lot of attention.
  - Stacked memory chips and memory on CPU
    - IBM expected to provide samples later this year
    - Both IBM and Samsung could be in production next year (2008)
  - Imaging arrays (pixelated devices)
    - Working devices have been demonstrated by MIT LL, RTI, and Ziptronix
    - Much work is supported by DARPA
- Pixel arrays offer the most promise for HEP projects.

LHC-ILC Workshop on 3D Integration Techniques
Large Systems Benefits from 3D-IC Integration

"Implementing a 2-Gbs 1024-bit \( \frac{1}{2} \)-rate Low-Density Parity-Check Code Decoder in Three-Dimensional Integrated Circuits"

Lili Zhou, Cherry Wakayama, Robin Panda, Nuttorn Jangkrajarng, Bo Hu, and C.-J. Richard Shi

University of Washington


Comparison between 3D and 2D designs

<table>
<thead>
<tr>
<th></th>
<th>2D design</th>
<th>3D design</th>
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<tbody>
<tr>
<td>Area (mm*mm)</td>
<td>18.238*15.92</td>
<td>(6.4*6.227)*3</td>
</tr>
<tr>
<td></td>
<td>=290.35</td>
<td>= 119.56</td>
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<tr>
<td>Total wire length (m)</td>
<td>182.42</td>
<td>22.39+22.57+22.46</td>
</tr>
<tr>
<td></td>
<td></td>
<td>=67.42</td>
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<tr>
<td>Max WL before buffer insertion (mm)</td>
<td>13.82</td>
<td>8.68</td>
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<tr>
<td>Max WL after buffer insertion (mm)</td>
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<td>4</td>
</tr>
<tr>
<td>Buffer used</td>
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<td>24636</td>
</tr>
<tr>
<td>Clock skew (ns)</td>
<td>2.33</td>
<td>1</td>
</tr>
<tr>
<td>Power dissipation (mw)</td>
<td>646.2</td>
<td>260.2</td>
</tr>
</tbody>
</table>

Performance Factor (Area * Timing * Power) = 14
Some 3D-IC Applications

- Pixel array for Particle detection (HEP community)
  (Pixel sensor + Analog + Digital + Memory + high speed I/Os)

- CMOS Image Sensor (Sensor + Processor + Memory)

- 3D stacked Memories (Flash, DRAM, etc...)

- Multi-cores Processor + Cache Memory

- NoC (Network on Chip)

- Processor + DRAM + RF + MEMS + Optical communication + ...
The more design automation is performed on the 3rd dimension, the more is the 3D-IC Integration.
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A common root installation for the different parts of the Design Platform

- PDK
- Libraries
- Memory compilers
- Utilities
- Tutorials

- Defining a unique variable for the root installation. All the modules inside refer to this unique variable.

Making the Design Platform portable to any site.
Collaborative Work and Contributions to the Design Platform

HEP labs contributing with Programs, Libraries, and Utilities. All included in the Design Platform

- DBI (direct bonding interface) cells library. (FermiLab)
- 3D Pad template compatible with the ARM IO lib. (IPHC)
- Preprocessor for 3D LVS / Calibre (NCSU)
- Skill program to generate an array of labels (IPHC)
- Calibre 3D DRC (Univ. of Bonn)
- Dummies filling generator under Assura (CMP)
- Basic logic cells and IO pads (FermiLab)
- Floor-planning / automatic Place & Route using DBIs, and TSVs (CMP)
- Skill program generating automatically sealrings and scribes (FermiLab)
- MicroMagic PDK (Tezzaron/NCSU)
Virtuoso Layout Editor with 3D layers and verification

- TSV
- Back Metal
- Back Pad
- DBI
- Calibre
- Assura
True 3D Mask Layout Editor

Technology Files fully supported by Tezzaron

MicroMagic MAX-3D
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3D-IC Automatic P&R using DBI and TSV

- System Level Partitioning
- 3D Floor-Planning
  - DBI, TSV, IO placement
- Automatic Place & Route
- Extraction, Timing Analysis
- Physical verification
  - 3D DRC, 3D LVS
- Dummies Filling
- Final 3D DRC

Design exploration at system level
Design exploration at the physical level
DBI, TSV, and IO placement & optimization
Cells and blocks place & route can be done tier by tier
To be done for each tier, then combined for back-annotation to the 3D top level system
Similar to the full-custom design flow
Using Cadence / Encounter for automatic P&R with Direct Bond Interface

- Encounter natively refuses to make the routing for pins on DBIs.
- Custom scripts solved the problem. It’s a workaround.
- The resulting layout is compliant to the Tezzaron DRC, LVS etc ...

DBI array generation + P&R

DBI completely routed down to the lower metal layers
Saving the floor plan for the bottom tier, and apply it for top tier so the automatic Place & Route run the placement and routing taking into account the DBI locations.

The place & route for both tiers is optimal for timing, buffer sizing and power performance.

This should result in a “correct by construction” design.
Using Cadence / Encounter for automatic P&R with TSV

3 ways investigated and solved for P&R using TSV:

1) Using a combined TSV / DBI cell allowing a straight vertical routing across the tiers. Scripting allowing the automatic placement, then P&R is done automatically. Access is available on M5. The router decides how to make the wiring to the pin.

2) Using a separated TSV, allowing the router to connect to any of the metal layers (except M6).

3) Using a combined TSV / DBI cell with pins for routing on all metal layers (except M6)
Create Bump Array

Floorplan > Flip Chip > Create bump Array...

Specify the array Name, number of bumps, pitch, …
Then click OK.

To save an IO file with this bump array choose the following menu:
Design > Save > I/O File…
Floorplan > Flip Chip > Assign Signal…

1. Select the IO signal in the list
2. Select the bump to be assigned
3. Click “Assign”. The selected bump become blue.
Custom Scripts Enabling Routing on DBIs

Create pins under bumps:

```
exec ../ScriptsBDI/makePhysical_Pins.sed Design_pins_bumps.io makePhyPins.do
```

Before

![Before image](image1)

After

![After image](image2)

Placing logical pins on bumps (DBIs), and extract their location.

Generating physical pins under bumps:

```
source makePhyPins.do
setBumpFixed -allBumps
```

Before

![Before image](image3)

After

![After image](image4)

Generating Physical pins from these locations. They can now be used as terminals for routing.
Automatic P & R Design Flow (From Floor-Plan to Routed Design)

- DBIs Placement
- TSVs Placement
- Obstructions on TSVs

- Std cells Placement
- Clock Tree Synthesis

Filler Cells Placement

- Clock routing
- Final routing
The M6 layer must not be used during routing. This layer is reserved for DBI.

- Routing Clock Nets

Route > NanoRoute > Route...

Switch Selected Nets Only in the Routing Control panel.

In the Attribute Menu, select:
Net Type: Clock Nets
Avoid Detour: True
(this allows to route the clock nets as straight as possible)

Use the “Mode setup” panel to switch the different options (for example, define the bottom/top routing layer).
Click OK to run Nanoroute.
Conclusion

- Design Methodologies strongly depend on:
  - The type of the 3D-IC process.
  - The nature of the application.

- A very collaborative work has been achieved and still ongoing between the parties CMC, CMP, MOSIS, FermiLab, Tezzaron, HEP Labs, NCSU.

A **Unique and Unprecedented** Design Platform resulted from the collaboration.

(Industrial CAD vendors just starting addressing the features)

- The community is eagerly awaiting for new CAD tools dedicated to 3D-IC Integration:
  - 3D-IC Partitioning: both at the system level and the floor-planning level.
  - Sign-off verification tools for 3D-IC Integration: (3D-DRC, 3D-LVS, 3D-Extraction)