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Level-Shifted PWM Techniques Applied to Flying Capacitor Multilevel Inverter

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Abstract: **This paper presents the level-shift PWM technique applied to the flying capacitor three-phase five-level inverter. The advantages of the proposed inverter compared to other MLIs, single DC source required, not required more number clamping diodes like diode clamped MLI, less THD value, low power loss, suitable high power applications. The main disadvantage of proposed topology more number of capaciotrs. The proposed topology 22 capacitors are used, each phase 6 capacitors connected across the switches. This paper simulation results verified phase voltage, line voltage, output voltage THD.**

Keywords: Multilevel Inverter, PD PWM, POD PWM, APOD PWM, Voltage, Current

I INTRODUCTION

Inverters are classified into single-phase and three-phase inverters. Again single-phase inverters are classified into the two-level inverter and multilevel inverters, however, three-phase inverters are classified into the three-phase two-level inverter and three-phase multilevel inverter. The merits of the two-level inverter, in the two-level inverter, used only a few switches, a single DC source, and low switching loss. Demerits are poor power factor, low efficiency, not quality output voltage, and current waveforms. The merits of a multilevel inverter it generates a nearly pure sine wave.

Authors in [1] reviewed unique symmetrical, asymmetrical, single-segment, and three-segment inverter topologies. However, as compared to unique topologies. In [2] extensive overview of various modulation strategies for a multilevel inverter. A changed PSPWM Technique is applied to this paper for a 5stage hybrid clamped inverter [3]. By imposing the PSPWM approach the excessive voltage capacitor charging time and discharging time may be reduced. Authors proposed [4] on this paper modulation and manipulation of 5stage voltage supply inverter for excessive strength applications. The voltage supply inverter became linked in again to again with the not unusual place DC link. To manipulate the output voltage of the inverter a brand new PD-PWM approach is applied. The proposed approachapplied5stages inverter comprises flying capacitor H- Bridge [5].

The PWM method, with the fantastic and terrible carriers. To lessen the overlapping of 5-degree layers, the road to line voltage waveform is proposed. In [6] Flying capacitor clamped 5-degree inverter was applied with a switched capacitor. The switched capacitor circuit with DC-DC boosting conversion is proposed. The first-class of output waveforms may be improved. in presents [7] a brand new six-transfer 5 phase improve impartial factor clamped inverter. The dc hyperlink voltage is decreased by 50%. Authors proposed [8] an extended operation of a flying capacitor multilevel inverter. To enhance the capacitor voltage applied a step with the segment redundancy method. This paper focussed [9] multilevel hysteresis present-day law and capacitor voltage flying capacitor. The modulation strategies were implemented to the 5-phase capacitor for the higher development of line-to-line voltages.

In this paper [10], a 5-level inverter with one DC power is implemented. The proposed topology reduces the number of switching states to generate different voltages. This improves the reliability of the circuit and also provides various modulations. In [11], a 5-level voltage source inverter with pulse width modulation was implemented. The inverter operates in a wide voltage range without a series connection of power semiconductors. This article [12] proposes a five-stage hybrid inverter control scheme for medium voltage applications. Diode rectifiers are used to supply voltage to the DC bus and are inefficient for higher applications. Multi-level inverters with flying capacitors [13] are implemented for series and parallel compensation in ISMS systems. A proposed method for controlling the charging and discharging of capacitors. In [14]-[16] multilevel inverter is used for power quality improvement in the distribution

system. Authors in [17]-[20] discuss advanced control techniques for the inverter.

This paper presents level-shift PWM techniques applied to a five-level flying capacitor inverter. Section II discussed the five-level flying capacitor inverter. Section III discussed the level shift PWM technique. Section IV discussed simulation results.

II FIVE-LEVEL FLYING CAPACITOR INVERTER

Multilevel – inverters are classified into diode-clamped MLI, Flying-capacitor MLI, and Cascade MLI. fig.1 shows a three-phase flying capacitor multilevel-inverter. A B and C are three phases.

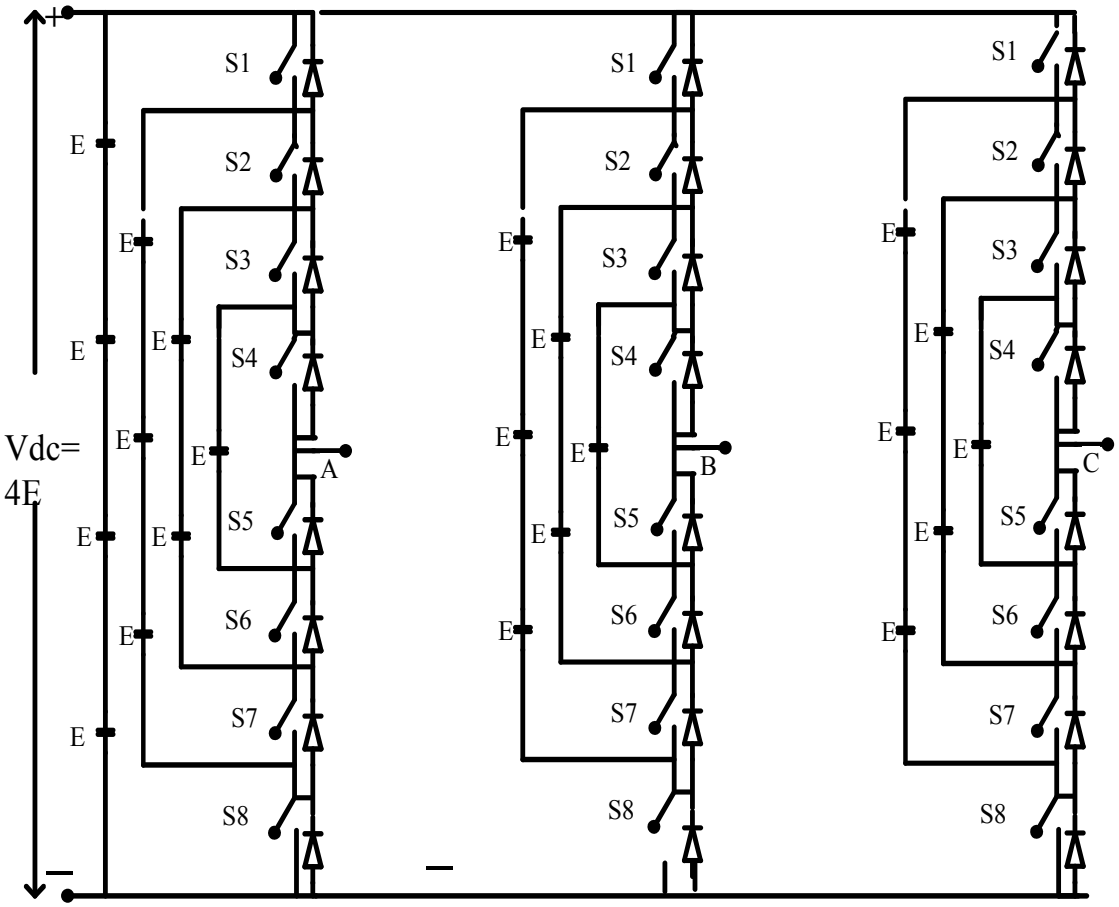

Fig.1. Single-phase flying-capacitor multilevel inverter

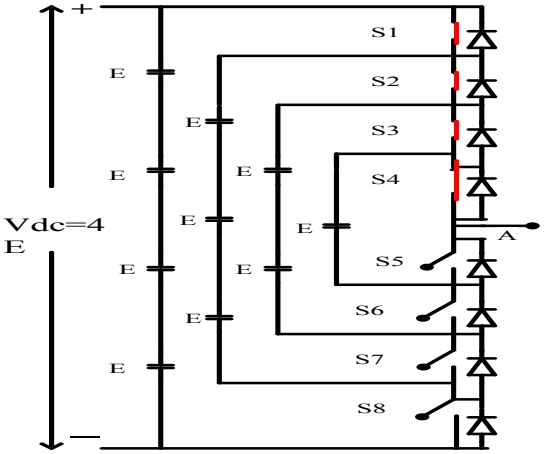

Fig 2. Mode 1 Operation

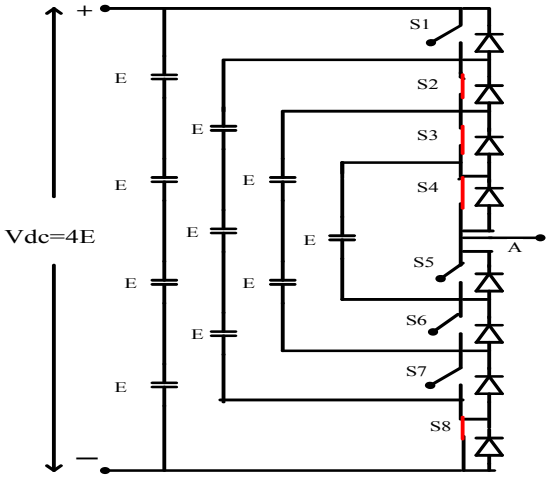

Fig 3. Mode 2 Operation

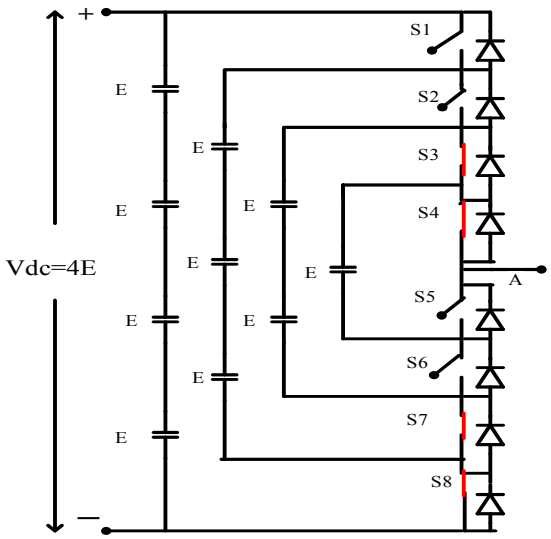

Fig 4. Mode 4 Operation

Fig 2. Represents the mode 1 operation of Single phase flying capacitor multilevel inverter. In this mode switches S1, S2, S3, S4 turn ON, and remaining switches S5, S6, S7, S8 turn OFF. It produces an output voltage of 4E.

Fig 3. Shows the mode 2 operations of single-phase flying capacitor multilevel inverter. In this mode switches S2, S3, S4, S8 turn ON, and remaining switches S1, S5, S6, S7 turn OFF. It produces an output voltage of 3E.

Fig 4. Represents the mode 3 operations of a single-phase flying capacitor multilevel inverter. In this mode switches S3, S4, S7, S8 turn ON, and remaining Switches S1, S2, S5, and S6 turn OFF. It produces an output voltage of 2E. The proposed topology used all capacitors are pre-charged capacitors. The proposed topology has a high number of voltage levels compared to the conventional topology.

Numerous capacitors. The inverter calls for a massive quantity of garage capacitors. Assuming that the nominal voltage of every capacitor corresponds to the nominal voltage of the switching device, the M-stage converter has a total (m1) * (m2) / 2 auxiliary capacitors for every segment department similarly to the (m1) primary DC bus capacitor. Is required. The voltage of the compensation capacitor. In contrast to diode clamp inverters, flying capacitor multi-level inverters have redundancy in internal voltage levels. Voltage redundancy is available so that individual capacitor voltages can be controlled. This elasticity makes it easy to manipulate the capacitor voltage and keep it at an appropriate level. The switching frequency must be higher than the fundamental frequency. The inverter can contain different combinations of 0f capacitors if they produce the same output voltage. This gives priority to charging or discharging individual capacitors [10].

A large number of storage capacitors can ensure operability in case of power failure. This inverter provides a redundant switch combination to balance the different voltage levels. Low harmonic content, such as high-level diode-limited inverters, eliminates the need for filters. The flow of both active and reactive power can be controlled. Using a large number of levels will require an excessive number of storage capacitors. High-end inverters are more difficult and more expensive to fit into bulky power capacitors. Inverter manipulation may be very complicated and the switching frequency and switching losses are excessive to supply actual energy.

TABLE 1: SWITCHING SEQUENCE

S.No	S1	S2	S3	S4	S5	S6	S7	S8	Output Voltage
1	1	1	1	1	0	0	0	0	4E
2	0	1	1	1	0	0	0	1	3E
3	0	0	1	1	0	0	1	1	2E
4	0	0	0	1	0	1	1	1	E
5	1	1	1	0	1	0	0	0	-E
6	1	1	0	0	1	1	0	0	-2E
7	1	1	1	0	1	1	1	1	-3E
8	0	0	0	0	1	1	1	1	-4E

The multilevel inverter switching sequence is explained in the table.1, conventional switching sequence generated only five-level voltage, the proposed sequence generated nine-level output voltage.

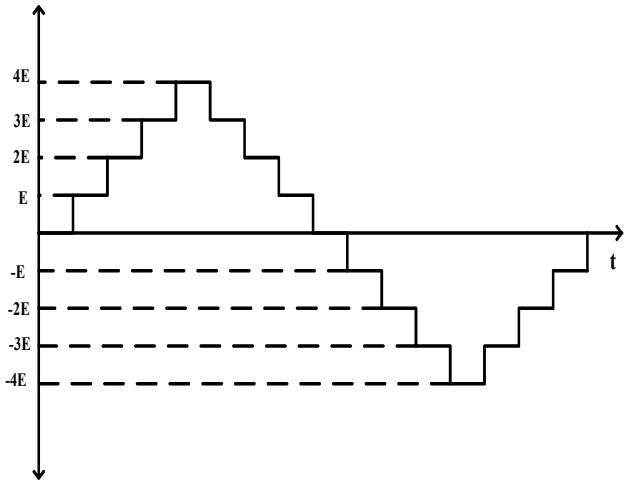

Fig.5. Output waveforms of MLI

Figure.5 shows the output voltage of the proposed topology output voltage, total of nine levels.

III LEVEL SHIFT PWM TECHNIQUE

Level offset PWM uses a different carrier signal (usually a triangle wave). They all have the same frequency, amplitude, and different DC offset. The phase angles may or may not coincide. The DC bias of each signal ensures that the horizontal line (DC voltage line) does not intersect multiple carrier signals in the waveform representation. The sum of

the peaks of all carrier signals is less than the peaks of the reference signal. It can also be divided into:

PD PWM: All carrier signals are in phase (have the same phase angle).

POD PWM: All carrier signals above zero (0 V) are in phase, but 180 ° out of phase with all carrier signals below zero.

APOD PWM: All other carrier signals are in phase, but 180 ° out of phase with the previous/next carrier signal.

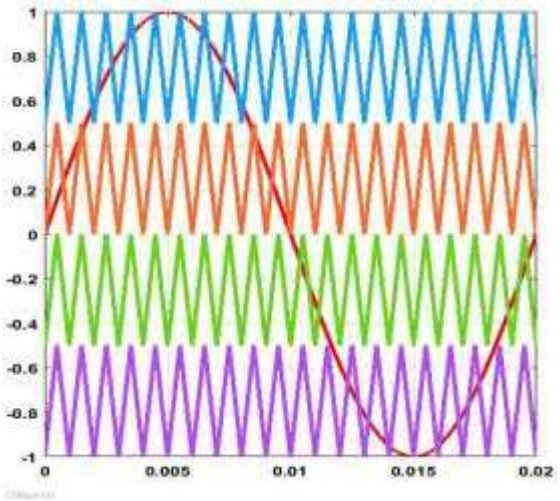

Fig.6.PD-PWM

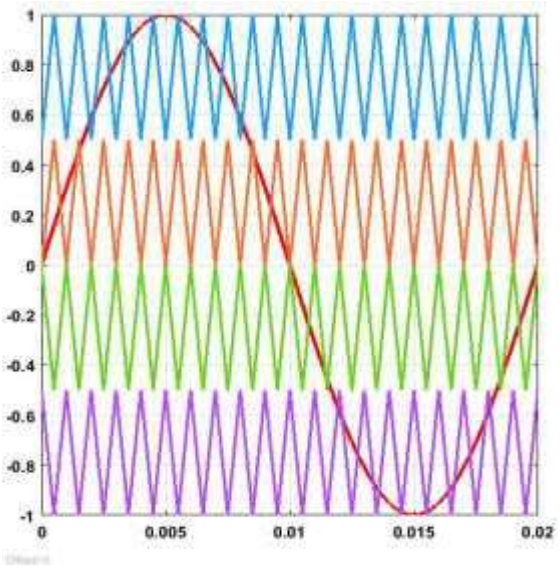

Fig.7.POD-PWM

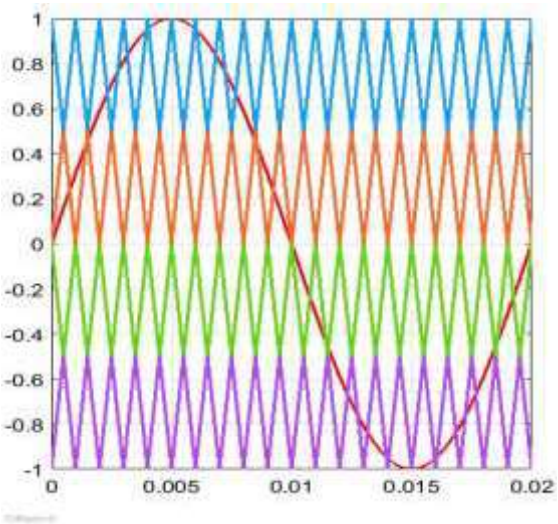

Fig.8.APOD-PWM

IV SIMULATION RESULTS

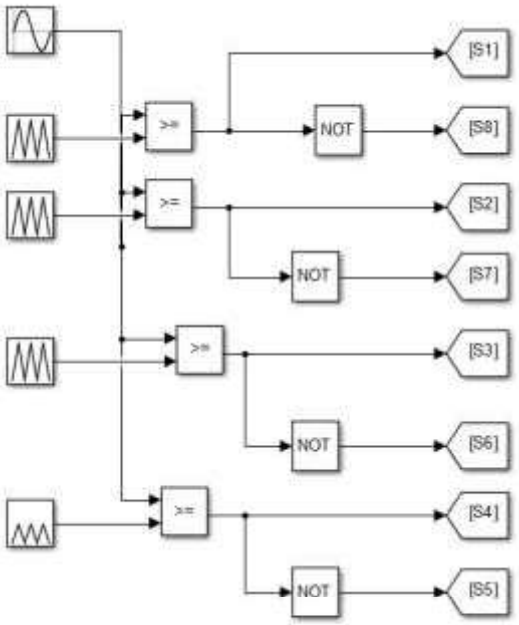

Fig.9.Carrier PWM Techniques

Fig.9 represents a switching pulse generating circuit. The convention switching sequence S1, S5 complementary, S2, S6 are complementary, S3, S7 are complementary, and S, S8 are complementary. The proposed sequence S1, S8 switches are complementary, as well as S2, S7 and S3, S6 and S4, S5 are complementary manners.

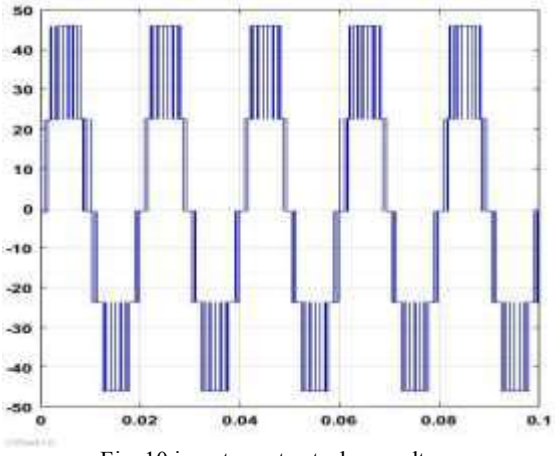

Fig. 10 inverter output phase voltage

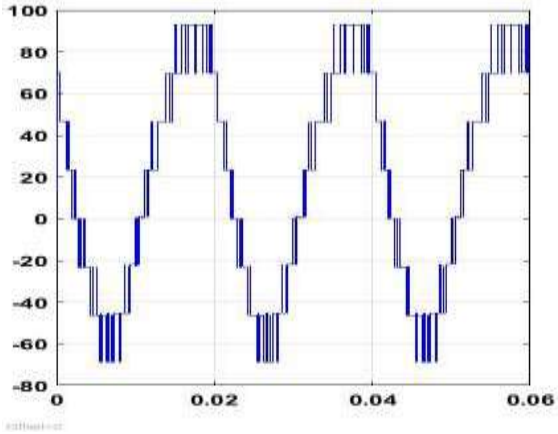

Fig.11 inverter output line-line voltage

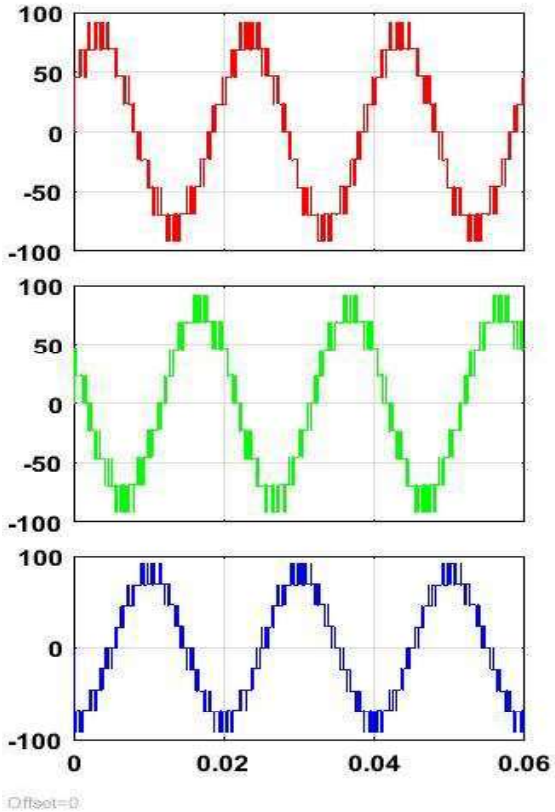

Fig.12 three-phase inverter output voltages

This section explains multilevel inverter output waveforms. Fig.10 shows inverter phase voltage, the output voltage shows five levels +44V, +22V, 0, -44V and -22V. Fig.11 shows inverter line-line voltage, fig.12 represents three-phase multilevel inverter output voltage. Each phase generated an eight-level output voltage. The proposed inverter output voltage THD value is 17.32%. fig.13 shows inverter output volatge with THD.

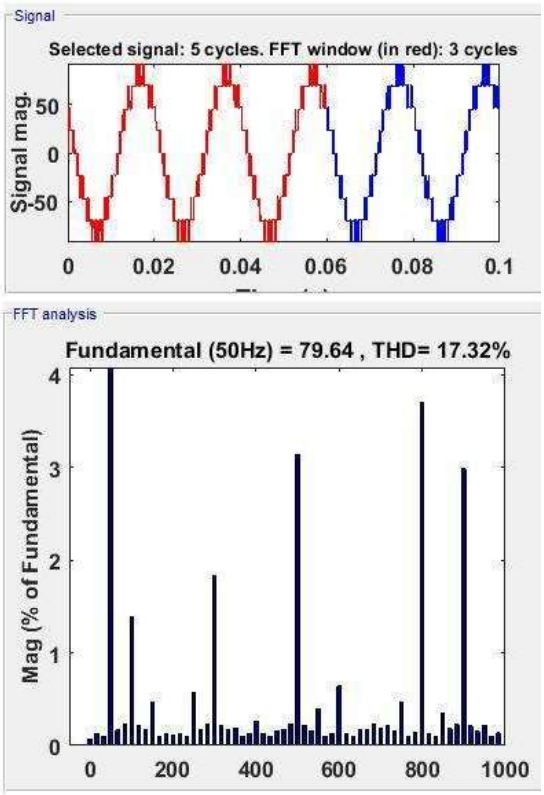

Fig.13 the output voltage THD waveforms

V CONCLUSION

This paper presented a three-phase flying capacitor multilevel inverter. The proposed topology advantages, single DC source, more number of output voltage levels, not required clamping diodes. The disadvantage of the presented topology required more number diodes. The proposed results simulation results were verified using Matlab/Simulink software, the output results are phase voltage, line voltage, three-phase line voltages, and output line voltage THD. The value of THD is 17.32%.

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