A Low Phase Noise CMOS Ring Oscillator Using Phase Modulation and Pulse Injection Techniques

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Abstract This paper presents a novel design of a ring oscillator (RO) producing eight phases output with accurate signal phase adjustment. By using the pulse injection technique, the RO phase noise has been strongly suppressed. In addition, a novel phase control technique is proposed for the implementation of the phase modulation. The proposed RO achieves a phase noise of -131.5 dBc/Hz @1MHz offset and FoM of -19.25 dBc/Hz. This RO consumes a 3.4 mW of power from a 1.8V power supply while having an oscillation frequency of 4.5 GHz and a locking range of 540 MHz in CMOS 0.18 um technology.

Key words Ring Oscillator (RO), Pulse Injection (PI), Phase Modulation, Figure of Merit (FoM), Phase Noise

I. Introduction

CMOS has become a prevailing technology for RFICs design and implementation because it is suitable for integrity with silicon-based system on chip. Moreover, it is mainly a convenient technology for ICs design due to its reduced cost [1]. The presence of highly scaled advanced CMOS processes leads to more and more lessening of RFICs digital building blocks area. On the other hand, the existence of non-scalable passive components such as inductors used for the implementation of RF analog blocks makes its area relatively un-scalable. This clarifies the interest of RF designers in inductorless RF blocks [2].

Oscillators are representing an essential building block in most very large integration level (VLSI) systems. An oscillator can be considered a key component of digital data recovery systems, clock recovery systems, clock generators and frequency synthesizers. CMOS inverter based ring oscillators design has gained the interest of RF researchers and designers as it can achieve a wide tuning range while having controllable tuning, low consumed power, small die area and low cost [3].

Oscillator phase noise which is used to express the amount of randomly going fluctuations caused by the timing jitter in frequency domain is representing an important measure of the oscillator performance [4]. Due to ring oscillators (RO) phase noise poorness, low phase noise ring oscillator design still represents an interesting idea. Phase noise suppression techniques such as pulse injection (PI) are being investigated for ring oscillators phase noise enhancement [5]. When pulse injection is used, the oscillation frequency is shifted from the free-running frequency to the injection locked oscillation frequency as shown in Fig. 1. The oscillation frequency is locked to one of the n-th harmonics of the injected signal frequency. The injection locked oscillator (ILO) phase noise is suppressed due to the periodic reset of the oscillator output phase error [5]. Figure 1 shows the ILO phase noise enhancement using PI technique where fosc is the RO oscillation frequency and 2f2 is the ILRO locking range.

A closed loop circuit of an odd single-ended delay stages forms the single-ended ring oscillator. A simple single-ended RO block diagram is given in Fig. 2.

Fig. 1. Phase noise enhancement of injection locked oscillator

Fig. 2. A block diagram of a simple three stage single-ended RO

Through this paper a multi-phase low power RO with an enhanced phase noise will be presented. This paper is organized as follows. Section II gives the proposed RO circuit with a brief description. Section III shows the obtained simulation results followed by a brief discussion. Conclusion is finally driven in Section IV.
II. Circuit Description

The schematic circuit of the suggested ILO is shown in Fig. 3. The proposed RO circuit consists mainly of three identical output split inverters (OSIs) with a feedback connection around the RO to allow oscillation start up. OSI is selected for the implementation of this RO due to its precise controllable tuned time delay. OSI also seems to have an improved matching properties in comparison to recently implemented inverter stages. Besides, it can verified that the OSI circuit has an enhanced performance and accurate controlled delay in the presence of fabrication mismatch [6]. The implementation of OSI circuit simplifies the control circuit of the proposed ILO to produce its different output signal phases.

![Schematic circuit of the proposed injection locked RO](image)

To have oscillation of the ring oscillator, it must have a phase shift of \(2\pi\) while having a voltage gain of one. A phase shift of \(\pi\) is provided through the inversion of the odd number inverters employed to form the RO circuit. Another \(2\pi/n\) phase shift should be provided by each delay inverter of the ring oscillator where \(n\) is the number of delay stages or inverters the RO has [7]. The frequency of oscillation is given by \(f_{osc} = \frac{1}{2nT_d}\) where \(T_d\) is the stage time delay assuming all of the delay stages are identical. Gate time delay is mainly pre-described through the selection of the delay stage dimensions (width, length and number of fingers). These dimensions are defining the charging and discharging time of the inverter which imply the definition of the inverter delay of time \(T_d\) [7].

Voltage controlled phase is produced through this ILO using a voltage pull-down circuit. This pull-down circuit depends mainly on the voltage transfer concept. This circuit aims to transfer an adjusted voltage value from the source to the drain of the \(M_{phase}\) transistor while operating in the deep-triode region of operation. This voltage transfer forces the oscillator output terminal to change its initial phase to the desired signal phase. As shown in Fig. 3, the trigger is representing the main control signal of the proposed RO circuit. When trigger signal is low, \(M_{trigser1}\) becomes off, oscillation stops and the output phase control circuit is enabled connecting the \(V_{di}\) voltage value to the output node. This changes the output node voltage from \((V_{ds})\) to \((V_{ds})\) adjusting its initial signal phase value. In contrary when the trigger signal goes from low to high, \(M_{trigger1}\) becomes on, oscillation conditions become verified, oscillation starts and the voltage transfer circuit switches off. Four different signal phases are produced when the drain of the \(M_{phase}\) transistor is connected to the RO output node. The other four phases are produced when the drain of the \(M_{phase}\) transistor is connected to the first inverter output. A simple representation of the RO output stage while trigger signal is high and low is shown in Fig. 4. Assuming that \(M_{phase}\) transistor dimensions have been selected to represent a semi-ideal switch, the time needed for the signal phase adjustment can be given by :-

\[
    t_i = \frac{RC}{V_{dd}} \ln\left(\frac{V_{ds}}{V_{dd} - V_{ds}}\right) 
\]

Where \(t_i\) is the time period needed for the circuit to have an output signal phase corresponding to the applied \(V_{ds}\) voltage value. \(R\) and \(C\) represent the output stage pMOS on-resistance and nMOS off-capacitance respectively.

The time period \(t_i\) is defining the period in which the oscillation is disabled. The output waveform is becoming more distorted as this time increases. Due to this distortion of output waveform, the spurious power gets larger. In general, the existence of spurious signal represent an annoying issue for oscillators designers. For spurious signal minimization, a mandatory reduction of output waveform distortion is needed. This spurious power reduction can be achieved by reducing the period of time in which the oscillator is off \(t_i\) [8]. On the other hand, that period of time \(t_i\) is required to be long enough to minimize the signal phase error of this RO.

Equation 1 is stating that the optimization of this time period \(t_i\) can be done through proper selection of transistors size (width, length and number of fingers) which imply the determination of the oscillation frequency and the dissipated power.

III. Simulation Results and Discussion

The proposed injection locked ring oscillator (ILRO) with phase modulation is designed and simulated using Agilent Advanced Design System (ADS) in CMOS 0.18 µm technology. Electromagnetic simulation is verified using Cadence design environment.

A. Oscillation Frequency and Tuning Range

The proposed ILRO has an oscillation frequency of 4.5 GHz while have a tuning range extends from 4.23 GHz to 4.77 GHz using the injected pulse frequency. Forming the ILRO using identical delay
stages helps in widening its locking range of frequency using a 500 MHz injected pulse. The duty cycle of the signal used for the implementation of the pulse injection technique would define the spurious power of this oscillator. The proposed ILRO injected pulse has a 90% duty cycle. The output spectrum is shown in Fig. 5.

A further reduction of the spurious signals could be achievable with the increase of the injected signal duty cycle which would increase the signal phase error. In addition, this duty cycle increase would increase the RO phase noise due to the shortening of time allocated for RO phase error reset.

B. Time Domain Signal Phases

The use of the voltage pull-down circuit of this ILRO achieve an accurate implementation of an eight output signal phases. These signal phases fit in the 8-PSK signal constellation. The output signal phases are 0, π/4, π/2, 3π/4, π, 5π/4, 3π/2 and 7π/4. The periodic steady state time domain simulation results illustrating the implementation of the eight different signal phases are shown in Fig. 6.

Figure 6 shows the time domain signal representation of the obtained oscillation signals. It illustrates also the signals phase shift of π/4 which emphasizes the ability of this RO to be used in phase modulation technique.

As in [2] and [3], multi-phase signal generation requires the RO to have multi-delay stages and produces the different signal phases from different output nodes. The ability of this single-ended ILRO to produce these different signal phases from the same output node would have a great impact on communication systems complexity reduction. In addition, the proposed ILRO represents a suitable RO to be used in M-PSK systems if \( V_{\Phi} \) control voltage values are precisely adjusted.

C. Phase Noise

The ILRO phase noise in comparison to the free running RO phase noise is shown in Fig. 7.

<table>
<thead>
<tr>
<th>Design Phase (°)</th>
<th>0</th>
<th>45</th>
<th>90</th>
<th>135</th>
<th>180</th>
<th>225</th>
<th>270</th>
<th>315</th>
</tr>
</thead>
<tbody>
<tr>
<td>Obtained Phase (°)</td>
<td>-1.01</td>
<td>45.05</td>
<td>89.14</td>
<td>134.96</td>
<td>179.05</td>
<td>224.71</td>
<td>269.91</td>
<td>314.61</td>
</tr>
<tr>
<td>Absolute Error (°)</td>
<td>1.01</td>
<td>0.05</td>
<td>0.86</td>
<td>0.04</td>
<td>0.95</td>
<td>0.29</td>
<td>0.09</td>
<td>0.39</td>
</tr>
</tbody>
</table>

Table 1 gives the values of the design signal phases in comparison to obtained signal phases values. The absolute phase error value is the absolute difference between the design and obtained signal phase values.
Single-ended inverter based ring oscillator structures are having good phase noise performance specially when a phase noise suppression is used [5]-[9]. The suppression of this RO phase noise is accomplished through the use of pulse injection technique. This ILRO has a phase noise less than -131.5 dBC/Hz @ 1MHz frequency offset while consuming only 3.4 mW of power.

A phase noise enhancement of -44.1 dBC/Hz @ 1MHz offset is achieved due to the employment of pulse injection technique. The pulse injection technique prevents the accumulation of the RO output phase error. The injected pulse is forcing the RO output signal to shift back to its right position resetting the ILRO phase error every 1/f_{inj} period of time, where f_{inj} is injected pulse frequency.

According to the figure of merit (FoM) formula given by Equation (2), this proposed low power, low phase noise multi-phase ILRO has a FoM of -199.25 dBC/Hz.

\[ \text{FoM} = L(\Delta f) - 20 \log(f_0/\Delta f) + 10\log(P_{dc}/1 \text{ mW}) \] \hspace{2cm} (2)

Where \( L(\Delta f) \) is the RO phase noise @\( \Delta f \) offset. \( f_0 \) is the RO oscillation frequency and \( P_{dc} \) is the DC dissipated power.

Table II summaries this ILRO performance and gives a comparison between its performance and other recently proposed ROs. It also indicates that the suggested structure of ILRO has achieved the highest FoM among these recently published designs.

**TABLE II. COMPARISON OF THE PROPOSED ILRO WITH PREVIOUSLY PUBLISHED WORK**

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Technology</th>
<th>Phase Noise (dBC/Hz)</th>
<th>Available Output Phases</th>
<th>DC Power (mW)</th>
<th>FoM (dBC/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work*</td>
<td>CMOS</td>
<td>-131.5 @ 1MHz</td>
<td>0, ( \pi/4, \pi/2, 3\pi/4, \pi, 5\pi/4, 3\pi/2, 7\pi/4 )</td>
<td>3.4</td>
<td>-199.25</td>
</tr>
<tr>
<td>4.23 ~ 4.77</td>
<td>CMOS</td>
<td>-119.9 @ 1MHz</td>
<td>( \pi/2, \pi, 3\pi/2, 2\pi )</td>
<td>112</td>
<td>-169.9</td>
</tr>
<tr>
<td>0.52 ~ 3.4</td>
<td>CMOS</td>
<td>-96.11@1MHz</td>
<td>0°, 120°, 240°</td>
<td>37 ~ 257</td>
<td>-161.8</td>
</tr>
<tr>
<td>13 ~ 25</td>
<td>CMOS</td>
<td>-99.5 @ 1MHz</td>
<td>single</td>
<td>27</td>
<td>-161.2</td>
</tr>
<tr>
<td>5.16 ~ 5.93</td>
<td>0.18 µm</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

*Simulation Results **Single Output Node

**IV. Conclusion**

An eight signal phases generation is accomplished through the implementation of inverter based single-ended injection locked ring oscillator with simple output phase control circuit. This phase control is constructed as a simple voltage pull-down circuit. The produced RO represents an enhanced and simplified structure for the generation of 8-PSK constellation signals with an average absolute signal phase error of 0.45°. The proposed ILRO has a minimized phase noise while consuming a low DC power. The proposed RO excellent performance is implied with its FoM. The next step is to implement this multi-phase RO so that a comparison between simulation and measured results can be held.

**REFERENCES**


