3D chip stacking
with C4
technology

Three-dimensional (3D) integration technology promises to continue enhancing integrated-circuit system performance with high bandwidth, low latency, low power, and a small form factor for a variety of applications. In this work, conventional C4 (controlled-collapse chip connection) technology is studied for robust interconnection between stacked thin chips. Various solder hierarchies to enable 3D chip stacking and packaging are investigated. Examples are presented to compare stacking schemes with sequential and parallel reflow. Chips as thin as 90 μm are stacked using conventional chip-placement and reflow processes, and the associated process challenges are investigated and discussed. Warpage of the thin chips is measured on various substrates. Rework of the chip stack has also been demonstrated through a temporary chip attachment operation, and the scalability of reworkable C4 is investigated.

Introduction

Integrated circuit (IC) technology has evolved from a transistor-centric era into an interconnect-centric era as the interconnect delay in critical paths now far exceeds the gate delay [1]. As feature sizes are further reduced to integrate more devices, the monolithic chip performance may degrade in contrast to the trend observed in the semiconductor industry predicted by Moore’s Law [2]. Meanwhile, the form factor of computing systems continues to be reduced for most applications, from servers to handheld devices. Two-dimensional integration can no longer offer the necessary packing density for devices and components. In addition, the ever-increasing demand for functionality requires that RF, analog, and mixed-signal circuits be integrated with the logic devices. There is a significant challenge to implement all these devices and circuits on the same layer of a monolithic substrate due to the incompatibility of manufacturing processes. Therefore, revolutionary interconnection schemes are needed for IC systems. By stacking multiple device and circuit layers, three-dimensional (3D) integration can enable much higher packing density, allow much shorter chip-to-chip interconnection paths, and make possible the heterogeneous integration of different types of chips in the same area. Thus, it is a promising solution to solve the above problems and has become an area of focus in advancing IC technology [3, 4].

Stacking monolithically produced semiconductor chips can be accomplished using the following approaches: chip to chip, chip to wafer, and wafer to wafer. Among these options, wafer-to-wafer stacking allows all chips on the wafers to be bonded simultaneously and provides the highest manufacturing throughput. A number of wafer-to-wafer bonding methods have been recently reported. Cu-Cu thermal compression bonding can be performed at temperatures of less than 300°C with high bond strength [5]. Polymeric dielectric glue bonding allows relatively compliant bonding at a low temperature [6]. Also, a room-temperature direct oxide bonding technology, Ziptronix ZiBond, has been developed [7]. In spite of this progress, wafer-to-wafer stacking has some intrinsic limitations. First, high coplanarity is necessary to ensure intimate contact across the entire wafer area. Second, wafer-to-wafer stacking requires very high yield for the individual wafers to avoid yield loss for the bonded assembly. In addition, matching the wafer size and the chips is required, which can significantly constrain chip design.

In contrast, chip-to-chip and chip-to-wafer stacking have advantages of flexibility in chip dimensions, the option of selectively bonding known good die, and a short time-to-market implementation. In addition, chip-to-chip and chip-to-wafer stacking can easily adapt to existing interconnection methods, such as wire-bonding...
and solder technology, and are easier to implement. Today, chip stacking with wire bonding has already been widely used to reduce the overall form factor and thickness of products in memory and handheld applications [8]. As the demand for higher performance and higher bandwidth continues to increase, chip stacking with through-silicon vias (TSVs) for interconnection is being developed and receiving more attention [9–12]. However, several issues need to be investigated for the manufacturing of TSV chip stacks. First, chip stacking involves handling of ultrathin Si substrates with a large number of TSVs. The thinned Si chips or wafers are very fragile and require special attention during processing and assembly. Tools and processes need to be developed to handle very thin chips and thin wafers at high throughput and low cost. Second, an assembly process needs to be investigated for robust interconnection between the multiple layers of thin chips and wafers at low cost. The C4 (controlled-collapse chip connection) technology that was developed by IBM in the 1960s has been widely used for high-I/O-count applications [13]. Thus, chip-stack assembly with C4 technology needs to be studied. Third, the reworkability of chip stacks and the encapsulation of multiple gaps between stacked thin chips should be investigated. Moreover, interconnection scaling needs to be explored to meet the increasing demand on I/O counts.

In this work, chip-stack assembly with C4 technology is investigated. Various wafer-handler (or carrier) release methods are first reviewed, as this is critical to enable the handling and processing of thin chips and wafers. Chip-to-chip stack assembly results with a discussion on sequential or parallel bonding approaches are then presented. The results for chip-stack rework and multilayer chip stacking are demonstrated. Finally, the scalability of C4 technology is described for ultrahigh-density interconnection between stacked chips.

Handling of thinned chips and wafers

Si wafers become fragile as they are thinned, making the handling of them a significant challenge for the application of automated equipment. The force to bend a Si wafer $F_{\text{max}}$ to breaking is proportional to the square of thickness $t$ [14], as indicated in $F_{\text{max}} = Ct^2$.

In addition, the highest stress is experienced at the surface of the wafer, where defects are introduced by TSV processing and wafer dicing. Therefore, the mechanical strength of a thinned wafer or chip with TSV interconnects may be further reduced. While a full-thickness wafer ($>700 \ \mu m$) may require several hundred newtons to bend to breaking, a wafer thinned to 70 $\mu m$ can be broken by a few newtons. To facilitate handling and processing, a handler wafer is usually attached to enhance the mechanical integrity of a Si wafer to be thinned. The most common approach is to laminate a device wafer with a handler wafer using a temporary adhesive [15, 16]. In general, a handler wafer should have a coefficient of thermal expansion (CTE) closely matched to the device wafer to be processed. A handler wafer also serves as a stiffener to keep a thinned wafer flat, allowing it to be handled as a regular wafer. Upon completion of wafer processing and dicing, the handler wafer then needs to be released from the processed Si wafer to allow TSV interconnection between the two sides of wafers or chips. Thus, debonding of the handler wafer is another important step for 3D integration.

In recent years, several debonding approaches such as thermal release [15, 16] and laser ablation [17, 18] have been studied and reported. In order to select a proper release process for handling thinned wafers, the chemical stability of the adhesive and the wafer processing temperature should be considered. In addition, the handler wafer requirements are different for the various release methods [15–18]. For instance, the thermal release method involves the use of an adhesive that melts at elevated temperatures. The handler can be either a Si or a glass wafer, and a hot-sliding tool must be used to separate the processed wafer from the handler wafer [15, 16]. Laser ablation release has a long history in microelectromechanical system device fabrication and transfer [17, 18]. It requires the use of a transparent glass handler wafer and an adhesive that strongly absorbs the working laser for the selected wavelength. An advantage of the laser ablation approach is that it does not involve high temperature or wet chemical processing. However, stress may be induced because shock waves occur when the adhesive material is ablated by pulsed laser. Moreover, with any release method, it is desirable to be able to re-use the handler wafers to reduce the manufacturing cost.

Thin chip stacking with C4 assembly

Regardless of the release method, chip stacking can be performed between individual chips or between chips and wafers. In this work, we consider chip-to-chip assembly because of its flexibility. C4 technology has been widely used in high-I/O-count flip chips for various applications because of proven manufacturability and reliability. Therefore, it is evaluated as an important interconnection solution for chip-to-chip stacking. Compared with regular full-thickness ($>700 \ \mu m$) chips, TSV chips are usually thinned significantly ($<150 \ \mu m$) to implement TSV interconnects. The tungsten-based TSV interconnects are fabricated with a CMOS-compatible TSV technology that is described in Reference [10]. The main assembly challenge concerns the bowing of the thinned TSV chips. In this work, the bowing is usually caused by inherent nonbalanced forces introduced by residual stress in the thin film layers, nonuniformity of the TSVs, and the
Figure 1
Chip bowing: (a) topography measurement of a thinned through-silicon via (TSV) chip with positive bowing and (b) the side view of the corners of the chip stack after assembly of a top chip; (c) topography measurement of a thinned TSV chip with negative bowing and (d) the side view of the corners of the chip stack after assembly of a top chip.
different wiring layers on the two sides of the thinned chip. The direction of the bowing may vary for TSV chips depending on the different processing conditions. In addition, the bowing may be temperature dependent. Therefore, the behavior of the C4 interconnects during the chip-stack assembly process needs to be studied. Ceramic substrates were first used to evaluate the chip-stack assembly because they usually have a relatively low CTE, very low warpage, and high mechanical integrity at elevated temperatures. During assembly, C4 solder melts at reflow temperature and then solidifies when the temperature decreases. Since the warpage of the ceramic substrate is negligible, the post-assembly chip warpage can be used as an indicator for the approximate warpage of the thin chip close to the solidification temperature.

**Figure 1(a)** is an example of a thinned TSV chip (~75 μm thick) that is bowed upward at its center due to nonbalanced stress. In this example, warpage of as much as ~50 μm can be observed across the chip area at room temperature after the chip assembly. After a full-thickness chip is joined on such a thinned TSV chip, warpage across the chip area cannot be observed from the top of the stack. However, in a side view of the corners of the assembled stack structure, different deformation can be observed for the two levels of C4 joints, as shown in **Figure 1(b)**. Obviously, the lower-level C4s are significantly compressed, while the upper-level C4s are significantly elongated after the reflow, which is consistent with the intrinsic bowing from the thinned TSV chip.

**Figures 1(c) and 1(d)** illustrate the opposite case in which the thinned TSV chip (~75 μm thick) bows upward by ~20 μm at the corners. As a result, the side view of the chip corners reveals that the lower-level C4s are elongated, while the upper-level C4s are significantly compressed. Since the same solder is used for both levels of C4s, both levels of C4s are melted simultaneously during reflow.

Through process improvement, TSV chips with relatively little warpage were obtained and assembly of
the chip-stack structure has been successfully achieved on ceramic substrates. With C4 technology, various solder alloys can be selected for the interconnection between the stack levels to create a solder hierarchy that allows a chip with high-melt C4s to be joined onto a chip with low-melt C4s or vice versa. Figure 2 shows examples of two-layer stacking of a regular full-thickness chip on top of a thinned TSV chip that is joined on a ceramic substrate. Figure 2(a) shows the same solder for the two levels of C4s, while Figure 2(b) shows different solder alloys used for the two levels of C4s. The use of a solder hierarchy can potentially enable selective chip removal or rework of the chip stacks. Furthermore, with low-melt solder for the upper-level C4s and high-melt solder for the lower-level C4s, a top chip may be selectively removed and reworked at a lower temperature without affecting the lower-level high-melt C4s.

Upon assembly, underfilling is necessary to mechanically couple a chip with a substrate and protect C4s from moisture and corrosion. During the capillary underfilling process, underfill is dispensed at an edge of a chip to allow the capillary force to fill the gap between the chip and the substrate. In the case of a stack of two chips, two gaps need to be filled. Thus, the amount of underfill material needs to be at least doubled. Experiments indicate that the capillary effect allows filling of the two levels of gaps simultaneously. Acoustic scan inspection verified that void-free gap filling can be achieved. The underfilled two-layer chip stacks were then subjected to deep thermal cycling (DTC) (from −55°C to −125°C) and the samples passed 1,000 cycles without dc failure on all the tested C4 and TSV paths. In addition, test C4 and TSV chains have survived more than 1,000 hours at a constant 0.7 A during current stress tests. While more comprehensive reliability tests need to be performed, these preliminary results indicate the robust reliability of the C4 and TSV interconnects.

Chip-stack rework and multilayer stack assembly

Known good dies are desired for high assembly yield, but it is difficult to perform thorough testing at the wafer level to verify perfect chips. As a result, rework is often performed, particularly for high-performance multichip modules (MCMs) because the overall package, as a system, costs much more than individual chips. In the past, temporary chip attachment (TCA) technology has been developed to prescreen chips to improve overall yield for high-performance MCM products [19]. With TCA technology, the number of reflows required for an MCM substrate is reduced during final assembly and test [19], which is beneficial to product reliability. To enable 3D chip stacks in these high-performance applications, a TCA process also needs to be developed for chip stacks.

A scanning electron microscope (SEM) image of a reworked chip stack on a TCA substrate upon completion of testing is shown in Figure 3.
have been successfully detached from the TCA without damage to the C4 bumps. The overall chip-stack structure was well maintained and the thinned interposer chip (<90 μm) remained intact. Since the hot-shear process temperature does not exceed the solder reflow temperature, the volume of C4 bumps is also well maintained. After the rework, the C4 bumps are usually reshaped through the reflow process. A reworked chip stack can then be treated as a thicker chip and joined onto a module substrate.

As shown in Figure 4, a reworked stack of a full-thickness CMOS chip on a thinned TSV chip has been successfully joined onto an organic laminate. The two levels of C4 interconnects are visible in the side view. The two gaps of the joined chip stack have been successfully underfilled simultaneously through a capillary underfilling process. In general, the strain on a C4 between a chip and a substrate can be reduced if the standoff is increased for a given distance to neutral point. In the case of the two-layer chip stack, the overall standoff height for the top CMOS chip is increased as a result of the added level of C4s, which is beneficial to stress reduction for its fragile low-k dielectrics.

In addition to stacking a full-thickness chip onto a thinned chip, stacking of multiple thinned TSV chips has also been demonstrated with C4 assembly. As shown in Figure 5(a), chips can be joined on a substrate with a sequential reflow process. In sequential reflow, first the bottom chip is joined onto the substrate followed by subsequent chips. A sequential process allows control of relative displacement between chips as each subsequent chip is joined onto the stack. Figure 5(b) shows examples of two-layer and three-layer stacks of thinned TSV chips (as large as 21 mm × 20 mm) utilizing sequential reflow of C4 interconnections.

An alternative approach, the parallel reflow process, has also been successfully demonstrated. By means of a conventional chip placement tool, multiple chips with C4 bumps are placed together and held in place with a tacky flux before the reflow process. The simultaneous joining of multiple chips can then be achieved within a single reflow step, which is desired for increased manufacturing throughput. However, a displacement may be incurred during the placement of multiple chips since the C4 bumps are not joined until the reflow. Therefore, the placement process must be well controlled to allow the self-centering effect of the C4 bumps to accommodate the potential displacement between chips.

**Scalability of reworkable C4 technology for 3D chip stacking**

To meet the demand for high I/O counts in high-performance and high-bandwidth applications, flip-chip I/O pitch needs to continue to be reduced over time. According to the International Technology Roadmap for Semiconductors, the area-array flip-chip I/O C4 pitch will be less than 85 μm for high-performance applications by 2020 [20]. In addition, fine-pitch wire-bonding...
interconnection in low-cost and memory applications needs to be replaced by fine-pitch area-array interconnection due to the performance limitation of wire-bond technology in a high-frequency regime and I/O-count limitation. Thus, fine-pitch C4 technology needs to be studied.

In this work, micro-C4 bumps as small as 25 \textmu m have been fabricated and joined onto Si-based test vehicles with bond pads that have various geometries and dimensions. With an optimal bonding profile, 100\% bonding yield is demonstrated for a die with up to \( \sim 11,800 \) Pb-free SnCu micro-C4s joined on a Si substrate with contact pads as small as 10 \textmu m. The average contact resistance of the micro-C4s on the various-size pads was measured using a four-terminal daisy-chain test structure. The measured dc resistance of the micro-C4s is plotted as a function of the bond pad area, as shown in Figure 6(a). As expected, the measured contact resistance increases as the bond pad size decreases. However, the measured contact resistance does not scale as a linear function of the contact area. As the contact area is reduced from \( \sim 415 \text{ \textmu m}^2 \) to \( \sim 78 \text{ \textmu m}^2 \), the contact resistance increases from \( \sim 43 \text{ m}\Omega \) to only \( \sim 60 \text{ m}\Omega \). This translates to an increase of \( \sim 40\% \) in contact resistance when the contact pad area is decreased by a factor of \( \sim 5 \). This can be explained by the current-crowding effect, which creates an uneven distribution of current density across the C4 contact area [21, 22].

Figure 6(b) shows an example of the simulated current density distribution across a C4 interconnect structure. Since the on-chip and handler wiring thickness in the vertical direction is much smaller (\( \sim 1.2 \text{ \textmu m} \)) compared to the contact dimensions in the lateral direction, the current density is the greatest near the edges of the contact via. Thus, the effective contact resistance does not scale linearly with the contact area as the contact size decreases. The implication of this result is that the electrical penalty is relatively small as C4 dimensions decrease to provide more I/O interconnections.

As C4 dimension scales, the reworkability is still of interest, particularly for high-performance applications. Thus, rework of chips with micro-C4s has been investigated through mechanical removal. Shear experiments are performed using an Instron tester with a special fixture to ensure precise shear movement. The shear force is characterized for contact pad area as well as the shearing temperature. As expected, the shear force decreases as the contact area is reduced. The shear force at room temperature of the Pb-free micro-C4s joined onto 23-\textmu m-diameter pads is as high as 4.6 gram-force and is reduced to \( \sim 1.5 \) gram-force when joined onto 5-\textmu m \( \times 15-\text{\textmu m} \) bond pads. To understand the fracture mechanisms occurring during the mechanical shear, the samples were inspected using a SEM. Figure 7 shows a comparison of two micro-C4s after the room-temperature shear experiments. The observed shear mechanism changes significantly as the dimension of the bond pads is reduced. The micro-C4 joined on the \( \sim 25-\text{\textmu m} \) pads is completely damaged, while the micro-C4 joined on the 10-\textmu m pad is only slightly scratched at the top. Apparently, the bond strength at the smaller contact interface is not enough to damage the bulk portion of the micro-C4s, thus allowing rework. To further reduce the removal force, shear experiments were also performed at elevated temperatures. As the temperature increased to 185\^\circ C (\( \sim 40\^\circ \text{C below melting point} \)), the shear force for chip removal was reduced to less than 0.5 gram-force per microbump. This reduction in shear strength is expected due to the creep effect of the solder at elevated temperatures, which further reduces the possibility of damage during the chip rework. With proper cleaning, the reworked dies with 11,800 micro-C4s have been successfully rejoined.
Conclusion
Stacking of thinned TSV chips has been demonstrated with C4 assembly for various schemes. Handling and release methods have been reviewed and compared for thin chips and thin wafers to enable chip stacking. The influence of thin-chip warpage on the assembly results was investigated. With warpage control, assembly yield of 100% has been demonstrated for stacking a full-thickness chip onto a thinned TSV chip with several thousands of TSV and C4 interconnects. The two-layer chip stacks on ceramic substrates have survived 1,000 DTCs and 1,000 hours of current stressing test conditions, which indicates the robustness of the TSV and C4 interconnections. Various solder hierarchies have been demonstrated and discussed. A two-layer stack on TCA has been reworked through hot shear without damage, followed by successful joining of the reworked chip stack onto organic laminates. In addition, multiple layers of thinned TSV chips have been stacked through both sequential and parallel reflow. Finally, the scalability of reworkable C4s has been demonstrated to enable future chip stacking with ultrahigh interconnection density. Electrical and mechanical characteristics of the micro-C4s were studied for reduced-size bond pads on Si-based substrates to enable the TCA process. Dies with more than 11,800 micro-C4s at 50-μm pitch have been successfully reworked without damage.

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