# Impedance Based Analysis and Design of Harmonic Resonant Controller for a Wide Range of Grid Impedance

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***Abstract – This paper investigates the effect of grid impedance variation on harmonic resonant current controllers for grid-connected voltage source converters by means of impedance-based analysis. It reveals that the negative harmonic resistances tend to be derived from harmonic resonant controllers in the closed-loop output admittance of converter. Such negative resistances may interact with the grid impedance resulting in steady state error or unstable harmonic compensation. To deal with this problem, a design guideline for harmonic resonant controllers under a wide range of grid impedance is proposed, where the controller gain boundary region is derived based on the short circuit ratio. The nonlinear time domain simulations are presented to verify the theoretical analysis in the frequency domain, and the experimental results based on the analysis results are included.***

***Keywords – P+Resonant current controller, Power quality, Grid-connected inverters, Harmonic compensation, Grid impedance***

## I. Introduction

The energy conversion technology and development process to improve the reliability and efficiency are important issue in these days as the grid is becoming much more power electronics interfaced. Particularly, demands for large power plants generating MW range electricity are drastically increasing. Hence, the grid network and impedance based design methods are normally required to stabilize the power converters with large capacities, such as HVDC (High Voltage Direct Current), FACTS (Flexible AC Transmission), and SVC (Static VAR Compensator) which are designed based on the grid information given from each grid company.

In grid-connected converters, harmonic compensation and their effect on the stability of the current control loop are important. To mitigate the grid side current harmonics according to the standards like IEEE 519, VDEW [1-3], various harmonic compensation solutions have been studied over the last years. Especially, proportional resonant controllers are widely used to increase the gain at fundamental frequency or to reduce the current harmonics generated from grid voltage disturbance and dead-time effect [4-10]. To implement resonant controllers in a computationally efficient way, the two-integrator-based resonant controller has been reported [9]. To further enhance the accuracy of harmonic compensation for high-order harmonics, the poles corrections and delay compensation have also been documented [9]. System stability problems owing to the *LCL* resonance and grid impedance variation are also well researched, such as harmonic impedance specification and their series-parallel resonance effects [11], and the system stability related to *LCL* resonance in weak grids [12]. In [13-15], the impedance-based analysis is used to reveal the interaction between the converter current control and grid impedance. The impedance regions have been developed to reduce the sensitivity of the converter and to obtain good gain margin and phase margin [13-15]. However, most of these works focused on the stability of current controller caused by the *LCL* resonance, while the dynamic stability and steady-state performance of harmonic resonant controllers under the different grid impedances are often overlooked.

This paper presents a comprehensive analysis on the effect of grid impedance variation on the harmonic resonant controllers by means of impedance-based analysis. It is found that the negative harmonic resistance may be brought by the harmonic resonant controllers even for harmonic frequencies below the gain crossover frequency. The negative harmonic resistances may interact with the grid impedance resulting in unstable harmonic compensation or steady state errors. To address this problem, a design procedure for the harmonic resonant controllers is proposed, where the boundary region for the controller gains is specified based on the Short-Circuit Ratio (SCR) of grid. Further, the sensitivity analysis of the resonant controllers to the output filter parameters shift is also performed. Lastly, time domain simulations are presented to verify the theoretical analysis and experimental results are included in last section.

## II. Impedance Based Analysis of Resonant Controller

### *A. System description*

The well-known 3-phase grid connected converter topology with *LCL*-filter is used to do a generalized analysis. Also p.u (Per Unit) value methods are adopted to define the output filter and controller gain to compare the system according to the power rating in the harmonic compensations. The grid impedance values are regarded as the % Z (percent Impedance), which can be calculated from the grid SCR derived from system p.u value. Block diagram and system parameter information are described in Fig. 1 and Table I, where the inverter side filter inductor $L_f$, inductor parasitic -

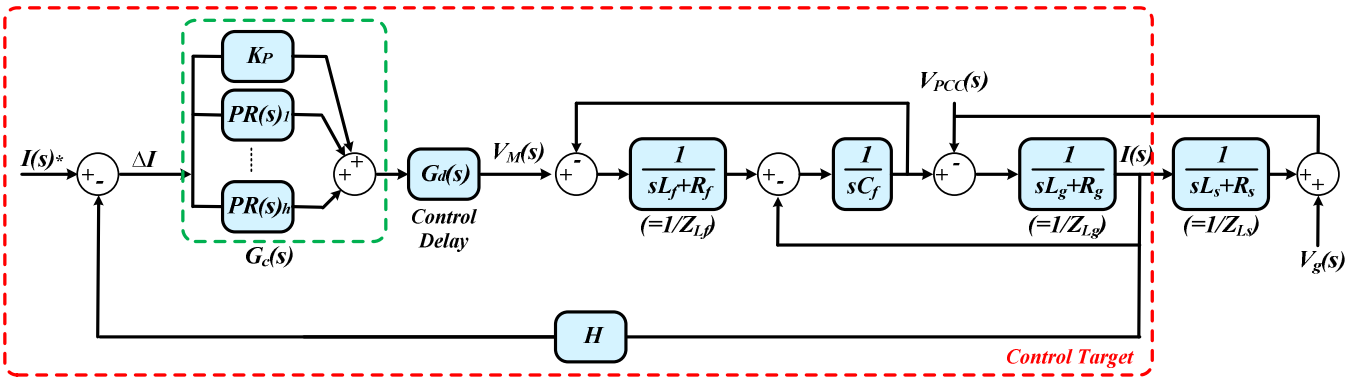


Fig. 1. Basic control block diagram of three-phase grid connected converter with grid impedance and grid connection.

resistance $R_f$, grid side filter inductor $L_g$, grid side inductor parasitic resistance $R_g$, filter capacitor $C_f$, current sensor gain H, gain cross over frequency $\omega_c$, and $Z_s(=L_s + R_s)$ are describing the grid impedance.

The proportional resonant controller is $G_c$, the delay term including computation delay and pwm delay considering sampling frequency $G_d$, *LCL*-filter output admittance $Y_{Mf}$ is the converter loop gain term, and the minor loop gain $Y_{Of}$ is describing the admittance obtained between the grid current and the PCC (Point of Common Coupling) of the grid side voltage [16]. The open loop gain of the control loop $T_{cf}$, the closed loop input admittance $Y_{ocf}$, the closed loop gain $G_{clf}$, and the current sensing feedback gain H which is assumed as constant gain of '1' [17].

Each component of the block diagram can be expressed in the s-domain like given in (1)~(8).

$$Y_{Mf} = \left.\frac{I}{V_M}\right|_{V_{PCC}=0} = \frac{Z_{Cf}}{Z_{Cf}Z_{Lf}+Z_{Lg}Z_{Lf}+Z_{Cf}Z_{Lg}} \tag{1}$$

$$Y_{of} = \left.\frac{-I}{V_{PCC}}\right|_{V_M=0} = \frac{Z_{Lf}+Z_{Cf}}{Z_{Cf}Z_{Lf}+Z_{Lg}Z_{Lf}+Z_{Cf}Z_{Lg}} \tag{2}$$

$$G_c = K_p + \frac{K_{i(f)}\cdot s}{s^2+\omega_f^2} + \sum_{h=3,5,7,11,13} \frac{K_{i(h)}\cdot s}{s^2+(h\cdot\omega_f)^2} \tag{3}$$

$$G_d = e^{-1.5\cdot s\cdot T_s} \tag{4}$$

$$T_{cf} = G_c \cdot G_d \cdot Y_{Mf} \tag{5}$$

$$Y_{ocf} = \frac{Y_{of}}{1+T_{cf}} \tag{6}$$

$$G_{clf} = \frac{T_{cf}}{1+T_{cf}} \tag{7}$$

$$I = G_{clf}\cdot I^* - Y_{ocf}\cdot V_{PCC} \tag{8}$$

The system parameters derived from the p.u based design method are described in Table I. The parasitic resistance of the filter inductance and resistance in the grid impedance are regarded as 10% of the base inductance value. Also a 10 kHz switching frequency is used as the nominal value for a 10 kW power rated converters.

Table I. P.U based system parameter example for single grid connected inverter (a) Inverter and passive filter parameter and, (b) Grid impedance calculations according to the Short Circuit Ratio(SCR)

(a)

| Power Rating (kW) | Vrms (V) | freq (Hz) | $L_f$ (mH) | $R_f$ (Ohm) | $L_g$ (mH) | $R_g$ (Ohm) | $\omega_{c(max)}$ (Hz) | $C_f$ (uF) |
|---|---|---|---|---|---|---|---|---|
| 10.0 | 380.0 | 50.0 | 3.7 | 0.115 | 1.8 | 0.058 | 1000 | 5.5 |

(b)

| Z (%) | SCR (1/(%Z)) | Ls (mH) | Rs (Ohm) |
|---|---|---|---|
| 1 | 100 | 0.46 | 0.014 |
| 5 | 20 | 2.3 | 0.07 |
| 33 | 3 | 15.33 | 0.48 |

*B. Grid impedance disturbance in PR controller operation*

Two cases are studied to see the grid impedance disturbance effect in PR controller performance and PR controller gain performance according to the grid variation.

First, to focus on the PR harmonic compensator which is located near a gain cross over frequency, the 11th harmonic is only considered as the analysis target. The loop gain of the converter is changed with the proportional gain $K_p$ and integral gain $K_r$ of each PR harmonic compensator and it is shown in Fig. 2, where the converter loop gain $T_c$, resonant controller fundamental integrator gain $K_{r1}$, 11th harmonic resonant controller integrator gain $K_{r11}$ is depicted to analyze the steady-state stability. The steady-state error is dependent on the line length $|1+T_c(jw)|$ from (-1,0) to the specified frequency response which is varying according to the $K_{r11}$ value in the system. On the contrary, the principal system stability is determined by the $K_P$ value. Even if the loop gain is over the unit circle in the certain range, the system can be in a stable condition following the $K_P$ value.

The time domain step response overshoot and steady state error result are matched with Fig. 2-(a). In #1 case and #3 case the results have not a large difference in the overall performance as like shown in Fig. 2-(a), (b). However, the #2 case has a steady state error value but more stable operation can be seen as like shown in Fig. 2-(a),(b).

Second, the grid impedance effect on the harmonic comp-

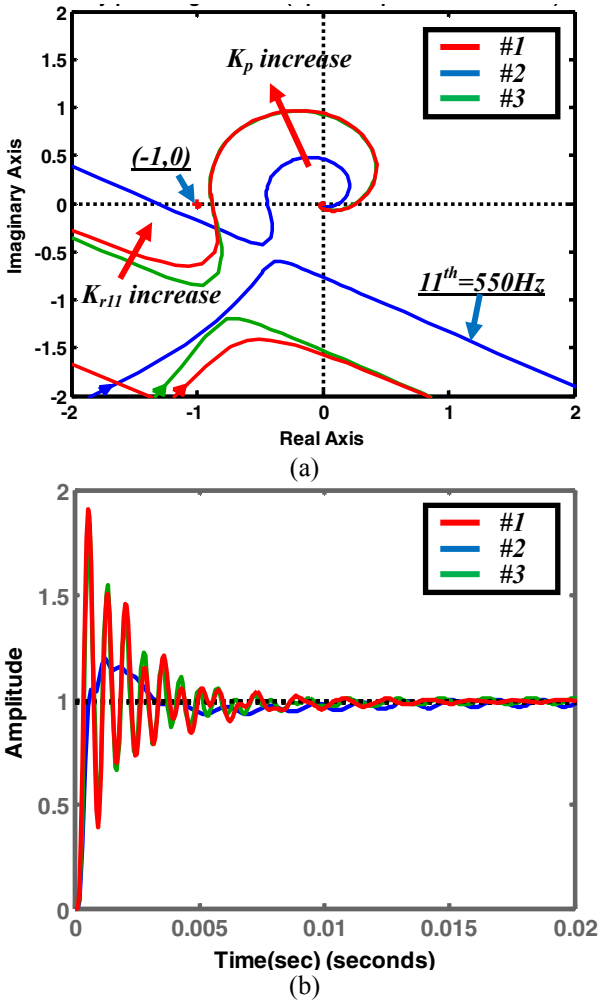


Fig. 2. PR controller proportional gain and integral gain effect analysis (a) Nyquist diagram of $T_c$ (open loop transfer function) in frequency domain, (b) Step response of $G_{cl}=T_c/(1+T_c)$ in time domain – (#1 : Kp=2 p.u Kr11=0.5 p.u, #2 : Kp=1 p.u Kr11=0.5 p.u, #3 : Kp=2 p.u Kr11=1 p.u)

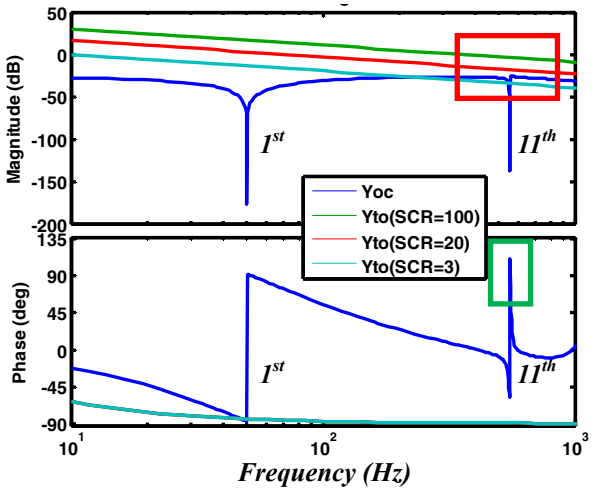


Fig. 3. Grid impedance disturbance analysis of 11th harmonic compensation according to $Y_{to}$ (=1/$Z_S$) variation (SCR =3~100), Red Box = grid disturbance point near gain cross over frequency, Green Box = negative resistance

ensator can be analyzed by means of (9)~(11) which is re-written from (8), where the admittance seen by grid connected inverter at the PCC point $Y_{to}$, the minor feedback loop gain $T_m$. The grid impedance is assumed as an inductor and resistance components and decided according to the SCR value of the main grid $Z_s$. $Y_{ocf}$ is describing the admittance obtained between the grid current and the PCC side grid voltage.

$$Y_{to} = \frac{1}{Z_s} \tag{9}$$

$$T_m = \frac{Y_{ocf}}{Y_{to}} \tag{10}$$

$$I = \frac{1}{1+T_m} \cdot G_{clf} \cdot I^* - \frac{T_m}{1+T_m} \cdot \frac{V_{PCC}}{Z_s} \tag{11}$$

The converter output impedance disturbed by varying grid impedance values are represented in the Fig. 3 where the converter closed loop input admittance is $Y_{OC}$, the varying grid admittance based on the SCR(%Z) $Y_{to}$ are minor loop gain term. In the status of low SCR, the inverter admittance is higher than the grid admittance, especially near the gain cross over frequency. In the condition of the same controller gain, the steady state error at a specific frequency region can be generated according to (10), (11) when $Y_{to}$ is lower than $Y_{ocf}$. If the SCR is low to be matched with weak grid condition, the system resonant frequency can be lower than the grid side.

This makes a resonant frequency to appear with uncompensated harmonic components in the vicinity of the gain cross over frequency by shaping the negative resistance between the current controller bandwidth and resonant frequency as like shown in Fig. 3. Hence, the gain controller design considering the grid impedance disturbance in the gain cross over frequency region should be studied in order to operate the converter properly in a wide range of grid impedance.

## III. Design of Resonant Controller in the Boundary Region

To implement the PR controller in the practical non-linear system, various kinds of design methods are studied. In [4], design guide for $K_p$ and $K_i$ values was proposed considering the gain cross over frequency $\omega_c$, filter inductance $L_f$ and the disturbance tracking error in the *S*-domain. Additionally, PR controller which has a delay compensation function $\square_h^*$ is studied in [8, 9], where the sampling frequency $T_s$, and harmonic order number h, the fundamental frequency $\omega_f$ are used. A proportional gain $K_P$ design guide is also studied in [8] according to the minimization method of sensitivity error in *Z*-domain. However, these studied methods are overlooking the grid impedance effect on their performance of harmonic compensation, which can make steady state error.

From a stability and sensitivity analysis result of converter input admittance and grid admittance, the available minor loop gain region can be depicted as like shown in Fig. 4-(a),(b), where the minor loop gain $|Z_{Mf}(=1/Y_{Mf})|/|G_{C*}G_d|$ is for the impedance of the output filter and impedance of the controller including control delay, minor loop gain

$|1+T_m*T_c+T_m|/|T_c|$ is for the function considering the feedback minor loop gain and converter loop gain. Besides, gain cross over frequency ($\omega_c$), another frequency point which is crossover the unity gain ($\omega_m$), gain margin ($1/A_m$) and phase margin ($\phi_m$) are used to define the relationship between the resonant controller gain and the stability and sensitivity according to the SCR.

In Fig. 2-(a),(b), to avoid the unstable status in dynamic performance of the two conditions, each minor loop gain $|Z_{Mf}|/|G_C*G_d|$, $|1+T_m*T_c+T_m|/|T_c|$ should have gain less than 1(=0dB). This means they have to be in the inner circle. However, these two minor loop gains can pass the unit gain if the proportional resonant (PR) gain at specific frequency is over the unit gain. This can be generated due to the -20dB or -40dB attenuation characteristics of output filter. In this case, amplitude of PR is dependent to steady state error. But phase difference which is driven from PR controller can make negative impedance by combining with phase characteristics from *LCL*-filter. This can make system to unstable conditions.

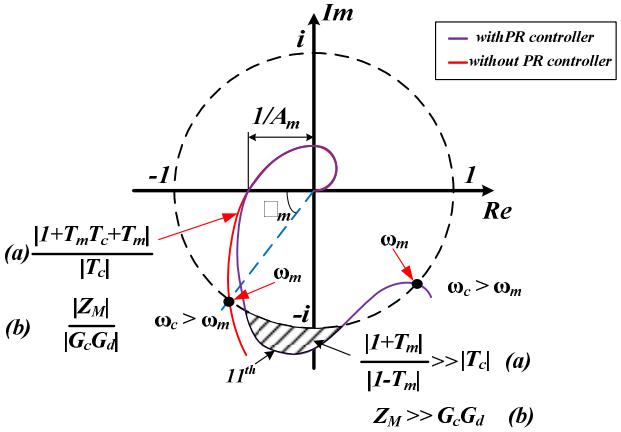


Fig. 4. Nyquist diagram of minor loop gain for stability and sensitivity (a) without grid impedance, (b) with grid impedance

The *LCL*-filter can also be modeled as an *L*-filter in the frequency range below the *LCL*-resonance [8, 12]. Hence, a harmonic compensator gain design based on the *L*-filter topology is adaptable in the low frequency harmonic analysis.

The overall system can be regarded as digital system if the grid impedance is modeled together not only the *L*-filter output admittance $Y_{Mf}$ but also the admittance obtained between the grid current and the grid PCC (Point of Common Coupling) side voltage $Y_{of}$. Besides, the grid admittance $1/Z_s$ can also be transformed to z-domain with considering the computational delay as like (12) by means of Zero-Order-Hold (ZOH) method [8], where $Y_X$ is the z-transformed admittance, $R_X$ is the parasitic resistance, $L_X$ is inductance respectively.

$$Y_X(z) = \frac{z^{-2}}{R_X}\frac{1-\rho^{-1}}{1-z^{-1}\rho^{-1}} \quad (where,\ \rho = e^{R_X T_S / L_X},\ T_S = 1/f_S) \qquad (12)$$

From (11), the overall open loop transfer function can be expressed as like shown in (13), when the grid is assumed having passive elements like inductor and resistor. In (13), the proportional gain is only considered to derive the controller gain because the proportional gain is a main factor in the stability and steady state problems as like shown in Fig. 2.

$$G_{all} = (T_m + T_c \cdot T_m + 1) - T_c \qquad (13)$$

$G_{all}$ should satisfy the stability criterion within the condition of cross over frequency ($\omega_c$), which is described in Fig. 4-(b) in order to stabilize the overall system (0 dB at $\omega_c$). Hence, the proposed proportional gain for grid connected inverter can be calculated like in (14), which is derived from (12) and (13), when the converter satisfies the specific cross over frequency to increase the DC-gain in the frequency below the cross-over frequency.

$$K_{p\_new} = \frac{R_S C - R_S C^2 - R_S CA + R_S C^2 A}{(A-1)\cdot(B-1)} - \frac{R_f D + R_S C^2 - R_f D^2 A + R_S C^2 A}{(A-1)} \qquad (14)$$

$$(where,\ A = e^{R_f T_s / L_f},\ B = e^{R_s T_s / L_s},\ C = e^{\frac{i\omega_f}{10 T_s}},\ D = e^{\frac{i\omega_f}{10 T_s}})$$

where $L_f$ is the filter inductance, $R_f$ is the filter parasitic resistance, $T_s$ is sampling frequency and $\omega_f$ is the cross over frequency. Further, the grid impedance values are $L_s$, $R_s$ respectively.

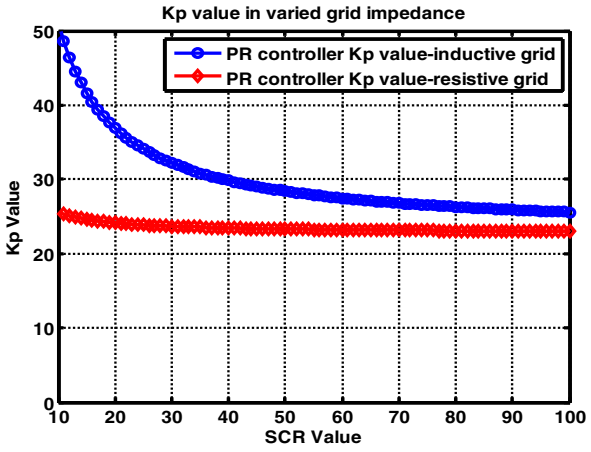


Fig. 5. Proposed $K_p$ value from (14) considering the grid impedance (inductive/resistive) value (10kW system example) to make stable system and improved harmonic compensation near gain crossover frequency.

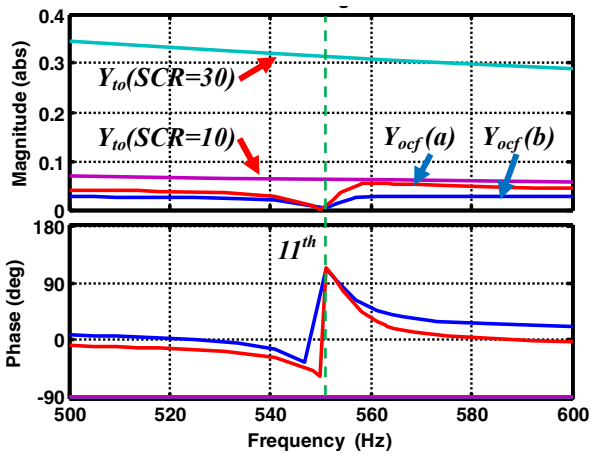


Fig. 6. Grid impedance disturbance analysis of 11th harmonic compensation according to $Y_{to}$ ($=1/Z_S$) variation, (a)-with conventional gain design method, (b)-with proposed gain design method (10 kW system example).

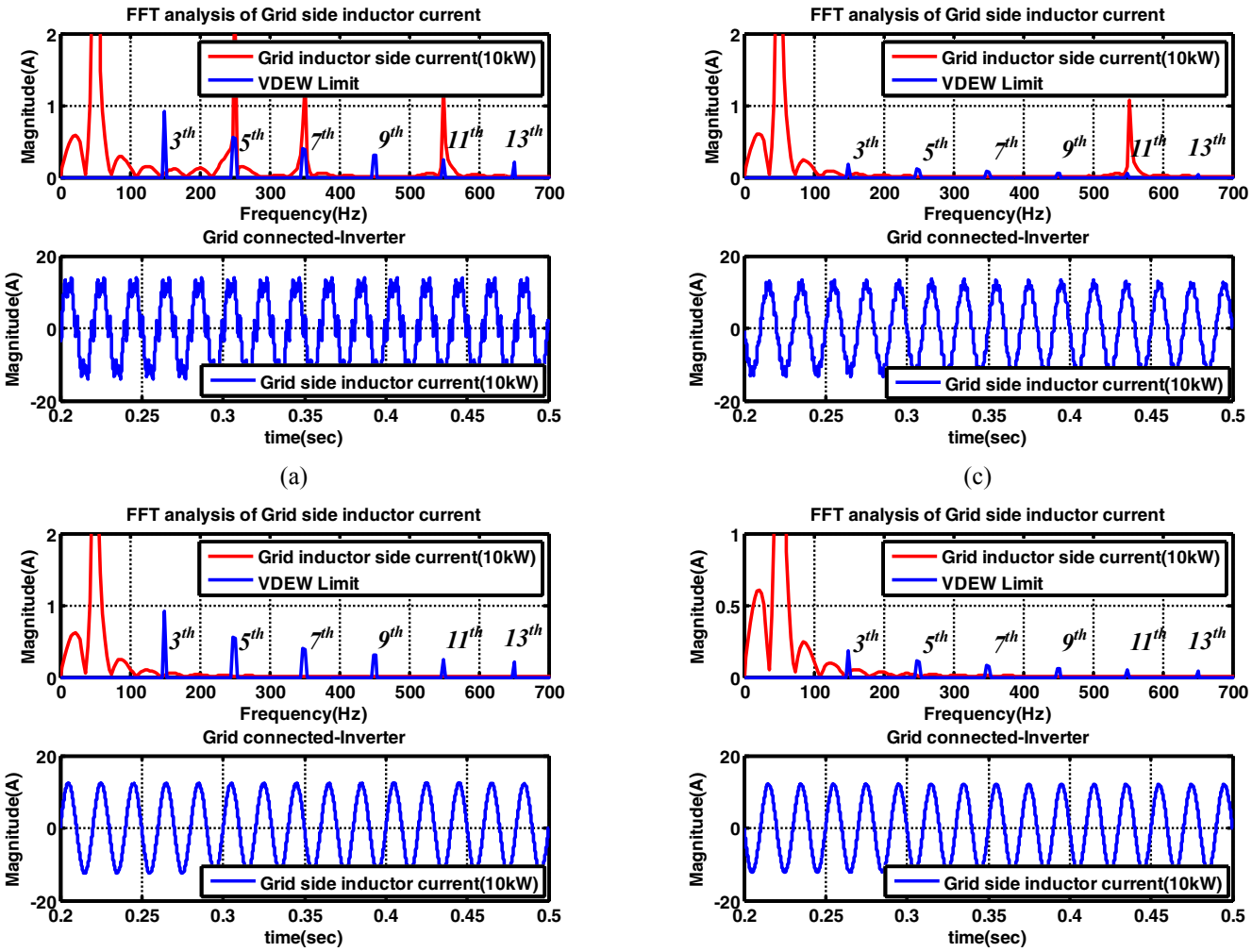


Fig. 7. FFT and time domain simulation analysis results of Grid side inductor current (10kW) with grid impedance variation condition, VDEW limits (Ki = 1 p.u (h=1, 3, 5), Ki = 0.5 p.u (h=7,11))
(a) without harmonic compensation (SCR=100), (b) with harmonic compensation (SCR=100),
(c) with harmonic compensation (SCR=20), (d) with harmonic compensation (SCR=20, $K_p$ = Proposed gain)

The relationship between proposed gain and the SCR value is shown in Fig. 5. If the resistive component is higher than the inductive components, $Y_{to}$ is hard to lower than $Y_{ocf}$ according to (1)~(11). Hence, the proportional gain in the harmonic compensation does not change in the overall design sequence. However, in the case of inductive grid impedance, $Y_{to}$ can be lower than $Y_{ocf}$ following the impedance relationship. The proposed gain should be reflected to meet the requirement of the impedance relationship and the system design requirement in a wide range of grid impedance.

Fig. 6 depicts re-analyzed Bode diagram. In the view of the 11th harmonic frequency range (550Hz), $Y_{ocf}$-(b) do not receive any disturbance from the changed $Y_{to}$ (SCR =30 to 10) as like shown in Fig. 6, when proposed gain design method is used in harmonic compensator. Besides, a gain, which is designed in a low SCR range, can also be used in a higher SCR range. Additionally, the integral gain for the proportional resonant controller should also be considered in terms of stability. Even though the integral gain has been looked not to have an effect in the gain or phase margin [8], those can also be affected in terms of the stability margin, when each resonant controller is used as in the case of 11th or above the frequency near the cross-over frequency [18]. In this case, the integral gain should be adjusted according to the stability conditions by considering the phase margin at each frequency.

## IV. Simulation Results

The simulink PLECS Block-set is used to simulate the analyzed results in the time domain. Grid impedance is regarded as an inductor and resistor, which are calculated from SCR ratio of the grid. Proportional resonant controller is implemented with two integrator methods [9]. The *LCL*-filter parameter is also designed from p.u based design method as like shown in Table I. To compare the compensated current with the standards recommendation, German Electricity

Association standard for generators connected to a medium-voltage network, VDEW is used. These standards use the SCR (Short Circuit Ratio) component in the calculation of the harmonic current limitation because the harmonic limitation value is changed according to the grid status [19]. For medium-low voltage grids, the maximum values must not be exceeded as shown in Table II, where $I_{hlim}$ is the relative maximum current for 10 kV and 20 kV line voltages.

Table II.
VDEW Harmonic Current Limit (h≤25$^{th}$) for medium voltage level[1] as a limitation of the Short Circuit Ratio (SCR)

| Ordinal number [v] | $I_{hlim}/SCR$ [A/MVA] | |
|---|---|---|
| - | 10kV | 20kV |
| 3, 5 | 0.115 | 0.058 |
| 7 | 0.082 | 0.041 |
| 9, 11 | 0.052 | 0.026 |
| 13 | 0.038 | 0.019 |
| 15, 17 | 0.022 | 0.011 |
| 19 | 0.018 | 0.009 |
| 21, 23 | 0.012 | 0.006 |
| 25 | 0.01 | 0.005 |
| >25 or even | 0.06/v | 0.03/v |

Simulation results are depicted in Fig. 7. The simulation conditions and the control are the same as given in Fig. 1 and Table I. In stiff grid conditions (SCR =100), grid side inductor is distorted due to a distorted grid PCC side voltage as like shown in Fig. 7-(a), when the harmonic compensator is not used in the current controller. However, if the PR controller is used, the harmonic components in the current are well compensated as like the analysis results and Fig. 7-(b). It can be found in Fig. 7-(c) that there are steady-state errors in the harmonic compensation near the 11$^{th}$ harmonics, if the grid impedance information of a weak grid is not included in the design process. These simulation results are for a weak grid (SCR =20). Hence, the harmonic limitation is also changed according to Table II. The 11$^{th}$ harmonic components are above the standards limitation due to the grid impedance as like shown in Fig. 7-(c). However, if the proposed gain design method is used for the harmonic compensator, the grid side inductor current is well compensated without steady state error in a weak grid range. Besides, these measured results are under the standard limits even if the grid impedance is increased, as like shown in Fig. 7-(d).

## V. Experimental Results

To verify the analyzed results, laboratory tests are performed in a scaled experimental set-up.

Fig. 8 depicts the laboratory test setup, where three phase Danfoss frequency converters are used as the PWM rectifiers. The control algorithms for the converters are implemented in a DS1006 dSPACE system. An 1.8 mH filter inductor is used as converter side filter inductor ($L_f$) and a 4.7 uF filter capacitor is installed as a filter capacitor ($C_f$) of the *LCL*-filter. Besides, a 0.9 mH filter inductor is used as the grid side filter inductor ($L_g$). To evaluate the same operation performance, 0~0.9 mH filter inductor is used as the grid impedance ($L_s$), which is calculated from the SCR (=%Z) value of PWM converter power rating. A programmable ac source is also used to make a distorted gird voltage condition. The harmonic limitations, which are included in the distorted grid voltage, are in Table III.

Table III.
Voltage Harmonic Limits [2, 3, 11]

| Odd harmonics | | | | Even harmonics | |
|---|---|---|---|---|---|
| Not multiple of 3 | | Multiple of 3 | | | |
| Order h | Relative Volt(%) | Order h | Relative Volt(%) | Order h | Relative Volt(%) |
| 5 | 6 | 3 | 5 | 2 | 2 |
| 7 | 5 | 9 | 1.5 | 4 | 1 |
| 11 | 3.5 | 15 | 0.5 | 6-24 | 0.5 |
| 13 | 3 | 21 | 0.5 | | |
| 17 | 2 | | | | |
| 19-25 | 1.5 | | | | |

The PLL algorithm used in this harmonic compensation strategy is based on a SOGI frequency Locked loop algorithm [20]. Space Vector PWM (SVPWM) with 10 kHz switching frequency is used as PWM methods in laboratory tests. Other control algorithm including PR harmonic compensator and PI controller are implemented in the dSPACE control desk and Matlab Simulink.

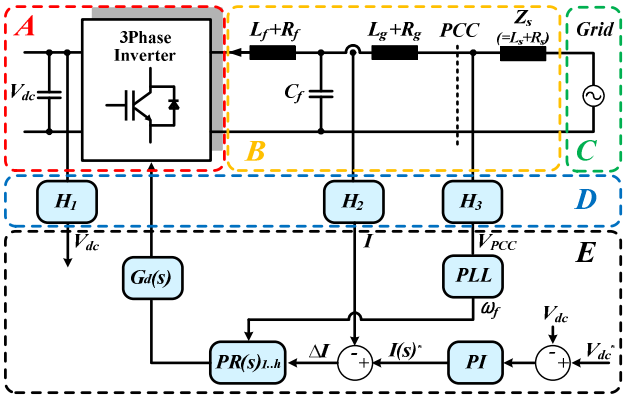


Fig. 8 Experimental set-up block diagram (A = Danfoss frequency Converter (Power ratings10 kW), B = Passive filter (*LCL*-filter and Grid impedance), C = Chroma Programmable 3-phase AC source, D = Sensor Box (*LEM* Voltage and Current Transducer), E = dSPACE DS1006 Control Block diagram and Control Desk)

Fig. 9 shows the measured grid side inductor current, distorted grid PCC side voltage and Fast Fourier Transform (FFT) results of grid side inductor current, when using and not using the proposed methods. If a fundamental frequency component of the grid side inductor current is only controlled in PWM converter, other distorted current components, which is driven from distorted grid voltage, can be shown with harmonic components as like shown in Fig. 9-(a). However, it can be found in Fig. 9-(b) that the distorted current can also be compensated well in the grid current control by using PR controller with the conventional gain design method. Harmonic components are diminished well behind the international standards [1-3] when the FFT results between

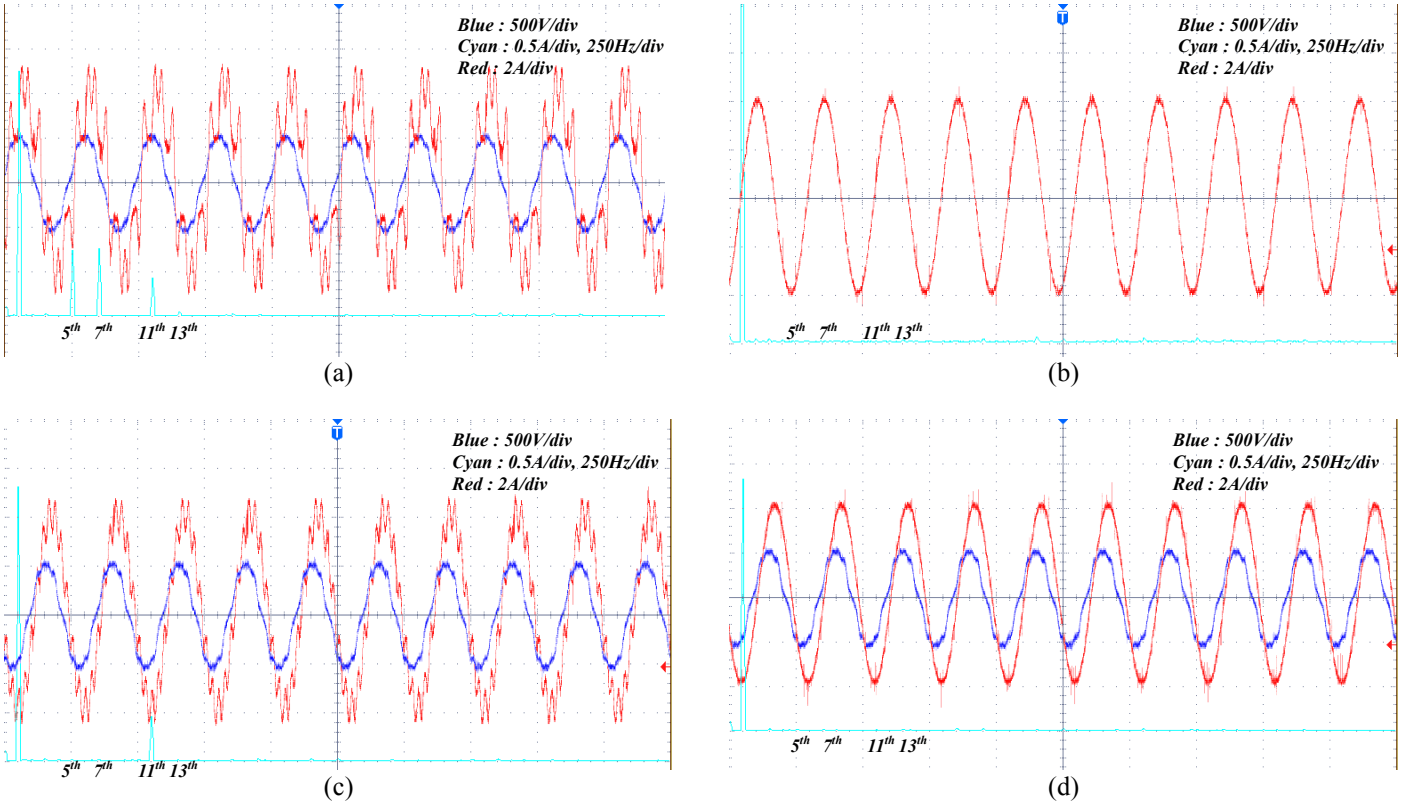


Fig. 9. Experimental results (red = grid side current, blue = distorted grid voltage from programmable ac source, cyan = FFT waveform of grid side current) (a) grid side inductor current waveform without PR harmonic compensation (SCR=100) (b) grid side inductor current waveform with PR harmonic compensation ($5^{th}$, $7^{th}$, $11^{th}$, $13^{th}$)/ (SCR=100) (c) grid side inductor current waveform with PR harmonic compensation ($5^{th}$, $7^{th}$, $11^{th}$, $13^{th}$)/ (SCR=30 with conventional PR controller gain) (d) grid side inductor current waveform with PR harmonic compensation ($5^{th}$, $7^{th}$, $11^{th}$, $13^{th}$)/ (SCR=30 with the proposed PR controller gain)

Fig. 9-(a) and (b) are compared with each other.

But these test results are from the stiff grid conditions (SCR = 100 ($L_s$< 10uH)) with conventional PR controller gain without considering the grid impedance information in the controller design.

On the other hand, it can be found that grid side inductor current can still have harmonic components ($11^{th}$ ~) especially those which are located near the system gain cross over frequency, if the grid condition is in a weak grid condition range like shown in Fig. 9-(c). Even though the grid current controller has a function to compensate harmonic components, there are still steady-state errors in the $11^{th}$ and $13^{th}$ due to a PR controller gain which is not considering the grid status. If the field data like the grid information is not considered, the PR controller gain sometimes should be adjusted again according to the circumstances in the fields even if the controller gain is designed well in the design process. It can not only make steady-state error of the reference but also unstable performance like the *LCL*-resonance, when the gain cross over frequency is near the negative resistance region or *LCL*-resonance frequency. Hence, the PR controller considering the grid information in a specific area is needed to operate in wide grid impedance region. In the weak grid condition (SCR = 30 ($L_s$ ≈ 1mH)), the grid side inductor current is well compensated in the same distorted voltage conditions like shown in Fig. 9-(d) without steady state error above the $11^{th}$ harmonics. This proposed PR controller gain can also be adopted in a stiff grid condition with same values are used. Besides, this proposed gain design method does not require trial and error adjustment in the field installation and operation if the grid impedance region is given from a grid company. It can be found that all harmonic components compensated with the proposed method are under the standards limitation like shown in Fig. 9-(d) by the FFT analysis.

## IV. CONCLUSIONS

This paper defines two possible regions and boundary conditions to derive the criteria near the cross over frequency. The first one is between the compensated converter harmonic controller impedance and the filter impedance to maintain the stability in the steady-state operation. Second one is between inverter output impedance and grid impedance which is varied according to the grid conditions to keep the stability in the steady-state operations. Besides, to verify inductive and resistive grid impedance conditions referring to practical cases, simulation and experiments are performed according to p.u based design method. And the proposed PR controller gain design method considering grid impedance is used. If the grid impedance is not considered in the PR controller design, the

current controller with harmonic compensator can have steady state error operation in a weak grid condition due to the disturbance of grid side admittance. However, it is verified that grid side inductor current can be compensated better without steady state error not only in the weak grid condition but also in the stiff grid condition, if the proposed gain design method is used.

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