HIGH-PERFORMANCE THREE-DIMENSIONAL ON-CHIP INDUCTORS FABRICATED BY NOVEL MICROMACHINING TECHNOLOGY FOR RF MMIC

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Abstract — Using novel micromachining technology, various three-dimensional (3D) on-chip inductors have been fabricated to achieve high performance and small area occupation for GHz applications. We have obtained 14nH, a peak Q of 38 at 1.8GHz with area occupation of 500μm by 500μm excluding pads (56nH/mm²) from a stacked spiral inductor on a glass substrate. Also, 1.75nH and a peak Q of 57 at 10GHz have been obtained from a levitated spiral inductor.

II. FABRICATION

Recently, we have reported a general 3D microfabrication method using a novel sacrificial metallic mold (SMM) [10]. Using this method, we can fabricate various 3D metallic microstructures including 3D on-chip inductors of common air-bridged spiral, stacked spiral, levitated spiral, and solenoid types.

Figure 1 shows the fabrication process of the proposed structure. At first, a previously IC-processed wafer is passivated with a dielectric material, electrical contacts are formed, and then the single seed metal for the next electroplating step is deposited on the entire surface. The thick copper bottom electrode is formed by conventional thick photoresist patterning and electroplating (Fig. 1a). Next, the conventional photoresist mold is patterned, UV-exposed, and the nickel SMM is formed by electroplating (Fig. 1b). The photoresist mold for the upper electrode is pattern-exposed (Fig. 1c), and developed together with the previously-exposed photoresist mold underneath (Fig. 1d). Then, the upper electrode and post are simultaneously formed by single-step copper electroplating (Fig. 1e). Finally, we complete the 3D on-chip inductor (made of copper) by selectively etching the SMM (Fig. 1f). A commercial Cu-compatible Ni etchant is used for the selective etching.

The process steps shown in Fig. 1b through 1e can be simply repeated for higher-level 3D inductors since at the stage in Fig. 1e, we can easily continue higher-level processes using the advantage that the surface is already planarized by the SMM and entirely covered with metal. Therefore, it does not require another seed-layer deposition and makes easy for next level lithography. In this way, various 3D on-chip inductors can be monolithically integrated without limitation on the number of levels.
Figure 1. The fabrication process for 3D on-chip inductors using the sacrificial metallic mold (SMM) [10]. (a) electroplating bottom electrode (b) patterning photoresist (PR) mold and electroplating the Ni SMM (c) pattern-exposure of the PR mold for upper electrode (d) development of both PR molds (e) single-step Cu electroplating for both upper electrode and post (f) final selective etching of the Ni SMM.

III. RESULTS

Figure 2a through 2c show SEM photographs of the fabricated 3D on-chip inductors made of 15µm-thick copper. In Fig. 2a, a 300µm-wide, 2.5-turn spiral inductor is levitated from the substrate by 50µm. In Fig. 2b, a stacked spiral structure is shown where the lower spiral has 2.5 turns and the upper spiral has 3 turns, respectively. Fig. 2c shows a 300µm-wide levitated and stacked spiral inductor, which has the lower 2.5 turns with 50µm-gap from the substrate and the upper 3 turns with 45µm-gap from the lower turns.

These 3D on-chip inductors have been measured in RF band (0.5 ~ 10 GHz). The one-port S-parameter is obtained from the measured two-port S-parameters of the 3D on-chip inductors fabricated on the corning #7740 glass wafer. The two-port S-parameters are measured by...
Wiltron 360B vector network analyzer and Cascade Microtech on-wafer probes. For reliable and accurate calibration’s sake, we have divided the frequency band into two parts, 0.5 ~ 3GHz and 3GHz ~ 10GHz, and performed both two-port calibration and two-port measurement separately in these two bands. In most cases, the inductance and Q-factors at two frequency bands show continuity at 3GHz except a few cases. The de-embedding procedure is not carried out since the substrate was glass. The equivalent lumped-circuit parameters are extracted by EEsof Libra with the equivalent circuit of the inductor as shown in Fig. 3, where the skin-depth effect of resistance is considered.

The measured inductance (imaginary part of the input impedance (Zin) divided by ω), resistance R (real part of the Zin) and Q-factor of the fabricated inductors are compared with their simulated values in Fig. 4a through 4c. The lumped-circuit parameters used for this simulation are listed in Table I. Fig. 5 is the Smith chart showing both measured and simulated S11 parameters of the levitated and stacked spiral inductor shown in Fig. 2c. In Fig. 6, we have compared the inductor performance of our 3D on-chip inductors with that of those reported earlier. As shown in Fig. 6, the performance of our 3D on-chip inductors is entirely superior to those reported earlier and elsewhere [11].

The data in Fig. 4 and Fig. 6 have been obtained from up to three-level fabrication process. However, it is easy to add a few more levels in fabrication process for higher-stacked structures since the SMM method does not limit the number of levels. Therefore, triple or fourth-folded 3D spiral inductors, which have the same area occupation as a single-level inductor, can be fabricated using this method. Furthermore, the levitated structure can be desirably integrated with conventional Si substrate to reduce the substrate loss and capacitive coupling.

Figure 3. Equivalent lumped-circuit for modeling the fabricated 3D on-chip inductors on a glass substrate.

Table I. Equivalent lumped-circuit parameters of the fabricated 3D on-chip inductors.

<table>
<thead>
<tr>
<th>Device</th>
<th>a</th>
<th>L (nH)</th>
<th>Cf (fF)</th>
<th>Rp (kΩ)</th>
<th>Cp (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 2a</td>
<td>0.50</td>
<td>1.75</td>
<td>5.9</td>
<td>41.9</td>
<td>3.4</td>
</tr>
<tr>
<td>Fig. 2b</td>
<td>2.34</td>
<td>13.8</td>
<td>4.5</td>
<td>29.7</td>
<td>63</td>
</tr>
<tr>
<td>Fig. 2c</td>
<td>1.34</td>
<td>4.84</td>
<td>7.0</td>
<td>25.7</td>
<td>14</td>
</tr>
</tbody>
</table>

Figure 4. Measured and simulated R, L, Q values of the fabricated 3D on-chip inductors. The equivalent lumped-circuit models and parameters used for this simulation are shown in Fig. 3 and Table I, respectively. (a) the levitated spiral inductor shown in Fig. 2a (b) the stacked spiral inductor shown in Fig. 2b (c) the levitated and stacked spiral inductor shown in Fig. 2c.
Figure 5. The Smith chart showing both measured and simulated $S_{11}$ parameters of the device shown in Fig. 2c.

Figure 6. Comparison of inductor performances.

B. Kim: 10µm-thick polyimide on silicon (Ref. 3)
Burghartz: Cu-damascene process on sapphire (Ref. 6)
GEC-Marconi: 9µm-thick polyimide on GaAs (Ref. 4)
Nam: 25µm-thick oxidized porous silicon (Ref. 4)
Y. Kim: 30µm-thick polyimide on alumina, solenoid (Ref. 8)
Young: 10µm-thick LTO, mechanically attached alumina core without adhesive, solenoid (Ref. 7)
Yoon: Corning #7740 glass, solenoid (Ref. 9)

IV. CONCLUSIONS

The monolithic fabrication method for the 3D on-chip inductors has been proposed. It utilizes only conventional lithography and electroplating techniques at low process temperature (<120°C), making the method IC-compatible. We can achieve thick metallization at low cost by electroplating and hence obtain on-chip inductors with low resistance and high Q-factors.

This technology is generic and is widely applicable to various RF MMICs such as high-current inductor loads for RF power amplifiers, from the excellent characteristics in RF performance of high Q factors and small area occupation in the fabricated 3D on-chip inductors.

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REFERENCES