Fabrication of a MEMS based high precision solar sensor for satellite applications using CMOS technology

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1. Abstract

This paper shows the design and fabrication of a miniaturized two-axis sun sensor for satellite attitude control, using a CMOS standard technology. The high precision will be obtained by the subdivision of field of view (FOV). A sun FOV of ±60 º and a resolution of 0.1º will be expected.

2. Introduction

A solar sensor is a device commonly used in attitude control of satellites [1]. The accurate relative position in the space is obtained from the incidence angle measurement of the sun light beam [2]. The starting point of the work shown is this paper was the design, fabrication and characterization of Vectorsol, a miniaturized sun sensor for satellite applications by the Universidad de Sevilla (US) and the Universidad Politécnica de Cataluña (UPC) [3], which combines MEMS and microelectronics technologies with a baseline crystalline silicon solar cell fabrication process, leading to a small area device (less than 1 cm^2), low weight, cost and power consumption. Electrical, mechanical, and thermal performance of the sensor device were been tested. The sensor device has been mounted in the Spanish nano satellite NANOSAT-1B, which has been launched in July 2009. Fig. 1 shows the structure of the MEMS for each axis.

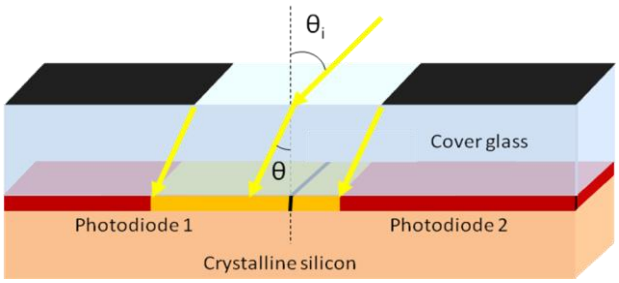


Fig.1. One axis sun sensor structure.

Two photodiodes have been manufactured in a silicon p-doped bulk. The sun rays reach the photodiodes trough a cover glass with an upper window, and generate a current in each one [4]. From the currents ratio we can obtain the incidence angle of the incoming ray. Fig. 2 shows the encapsulated final device. The aluminum shell is very important in order to protect silicon against dangerous radiations.

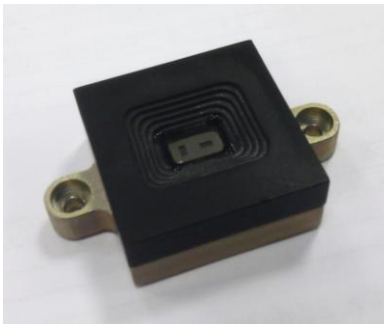


Fig.2. Sun sensor device for satellite application.

Since the launch of the NANOSAT-1B, this sensor has been working at expected performance.

3. Sensor description

The objective of this work is the improvement and miniaturization of the Vectorsol sensor. In order to increase the accuracy of measurement is necessary to maintain high gain factor without harming FOV and to reduce quantification error in AD converters. These two assumptions can be solved by using the subdivision of the FOV en N sub regions, as shown in Fig. 3, using in this case five sub regions of Θ grades. In each sub region, the angle for one axis is obtained using two photodiodes, being necessary a total of N+1 photodiodes in order to cover all the field of view (see Fig. 4) [5].

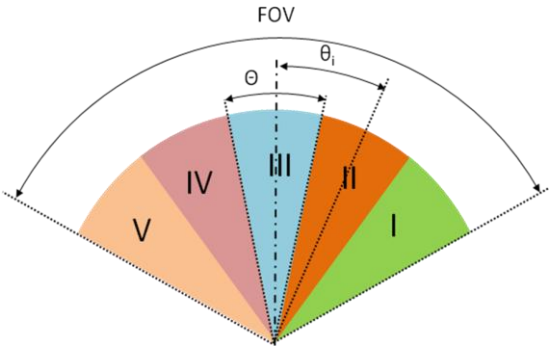


Fig.3. Subdivision of the FOV.

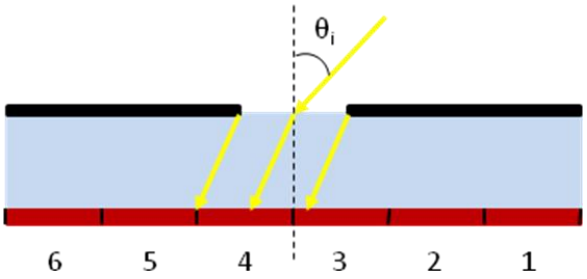


Fig.4. Multicell solution.

Given the illuminated areas of the actives photodiodes in one sub region (Fig. 5) it is possible to determine the angle of incidence using (1).

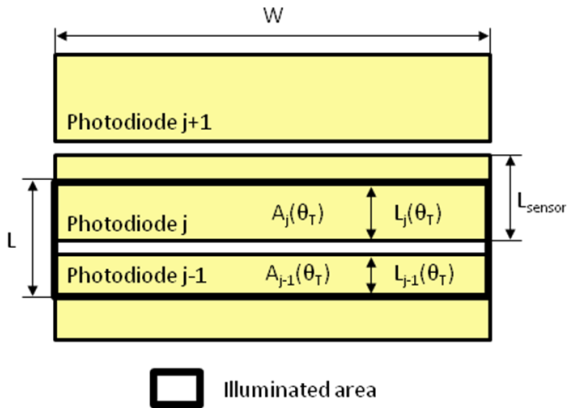


Fig.5. Active area in photodiodes.

$$R_j(\theta_T) = \frac{I_{ph_j} - I_{ph_{j-1}}}{I_{ph_j} + I_{ph_{j-1}}} = \frac{A_j(\theta_T) - A_{j-1}(\theta_T)}{A_j(\theta_T) + A_{j-1}(\theta_T)} = \frac{L_j(\theta_T) - L_{j-1}(\theta_T)}{L_j(\theta_T) + L_{j-1}(\theta_T)} \quad (1)$$

Three layouts have been designed, according to three different division of the FOV. Layouts for 5 subdivisions (6 photodiodes), 3 subdivisions (4 photodiodes) and FOV complete design (2 photodiodes, as the original Vectorsol) have been obtained. Using the nomenclature shown in Fig. 6, the parameters of the three designs for each axis can be found in Table 1.

The lateral photodiodes in the array are bigger than the others, due to a security margin that has been added to the design in order to obtain photocurrent even outside the limits of the FOV. Therefore, if there are any alignment errors between cover glass and silicon, there is always an illuminated photodiode.

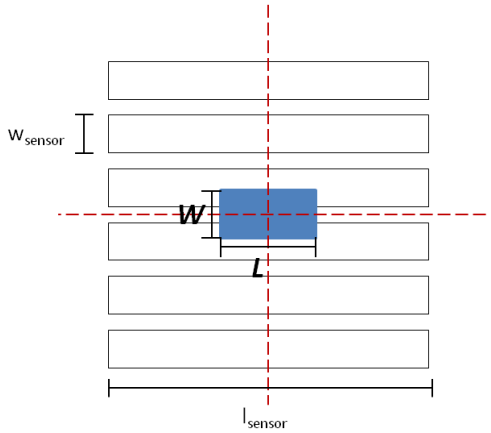


Fig.6. Nomenclature used in the design.

Subdivisions	5	3	1
Photodiodes	6	4	2
Size of the window (WxL)	200µm x 500µm	320µm x 500µm	900µm x 500µm
l_{sensor}	1500µm	1500µm	1500µm
w_{sensor} (central photodiodes)	160µm	280µm	890µm
w_{sensor} (lateral photodiodes)	180µm	290µm	-
Gap	20µm	20µm	20µm

Table 1. Parameters of the design.

The layout of a 6-photodiode sensor, designed using CADENCE software, can be seen in Fig. 7. It consists of two orthogonal arrays, one for each axis.

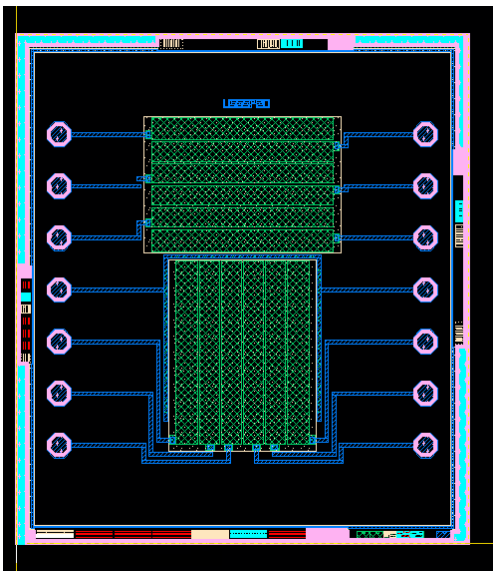


Fig.7. Layout of the sensor.

Besides the changes in the number of photodiodes, other structural variations were proposed to test their influence in sensor performance, such as the size of the gap between photodiodes (10 µm, 20 µm and 30 µm) and the presence of a passivation layer. As results, a layout with a matrix of 12 different designs has been obtained.

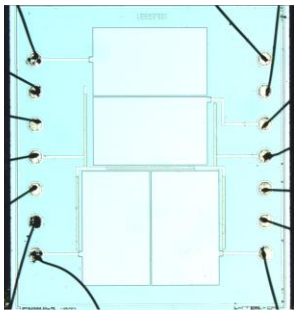
4. Sensor fabrication

The choice of using a CMOS process for the fabrication of these sensors is intended to integrate, in a future work, all the auxiliary electronics on the same silicon dice. To achieve this, it is necessary to test if it is possible the manufacture of photodiodes using CMOS technology at least with the same performance that those obtained as a results of a specific process.

The layout obtained in the design stage has been repeated all over the wafer, in order to study the repeatability. In addition, variations in the fabrication process have been included. 8 different wafers have been obtained, including the 12 designs in each of them.

The chip has been manufactured at the facilities of the Centro Nacional de Microelectrónica (CNM), located in Barcelona, at the beginning of 2010. A dice of 16 mm^2 for each sensor has been obtained, representing a quarter the size of the actual chip. In Fig. 8 it can be seen the fabricated silicon dice of the three main designs: 6-photodiodes (Fig. 8a), 4-photodiodes (Fig. 8b) and 2-photodiodes sensor (Fig. 8c).

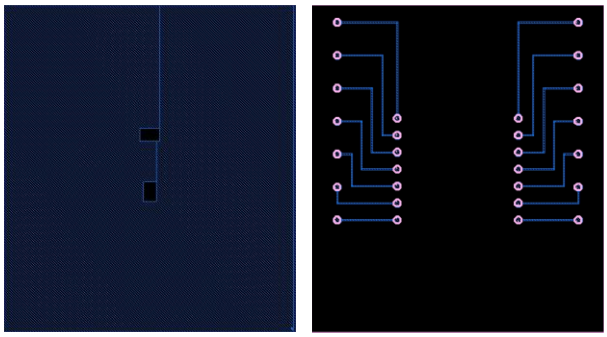
a) b)



c)

Fig.9. Fabricated chips.

A 500 µm thick boron-silicate wafer will be used to design and manufacture the cover glass-window structure, which is currently on fabrication stage. On the top face, it is complete metalized except in the two windows (Fig. 9a). On the bottom, it can be found the electrical connections between silicon and PCB (Fig. 9b).



a) b)

Fig.9. Layout of the cover-glass.

Flip-chip technology will be used to link cover glass and silicon dice, in order to decrease errors due to align mismatching. The resulting completed flip chip assembly is smaller than a traditional system. The short connections reduce inductance, allowing higher-speed signals, and also carry heat better. On the other hand, flip chip is not suitable for easy replacement, or manual installation. In addition, they require very flat surfaces to mount to, which is not always easy to set, or sometimes difficult to maintain as the boards increase or decrease their temperature. Also, the short connections are very stiff, so the thermal expansion of the chip must be matched to the supporting board or the connections can break.

As result, a test device will be obtained (Fig. 10) which can be easily placed in the board containing the signal adaptation circuits. The electrical connection between glass and PCB will be made using a wire bonding process.

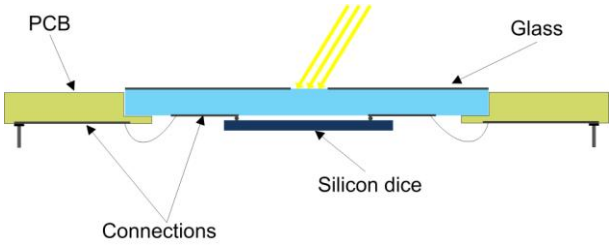


Fig.10. Test device.

5. Experimental results

In order to check the validity of CMOS process for intended purpose, a set of 24 chips were encapsulated using a standard DIL-16 (Fig. 11).

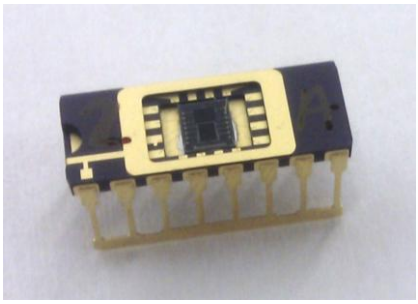


Fig.11. Encapsulated chip.

For each sensor, all photodiodes were tested in dark and light conditions. The test consists of getting the I-V plot of the photodiode, and checking if the noise voltage level working in the reverse bias region is below a certain threshold (about 0.1 μA), which means that the photodiode is capable of detect the presence of light. An example of the test for one photodiode can be seen in Fig. 12. All the chips were validated.

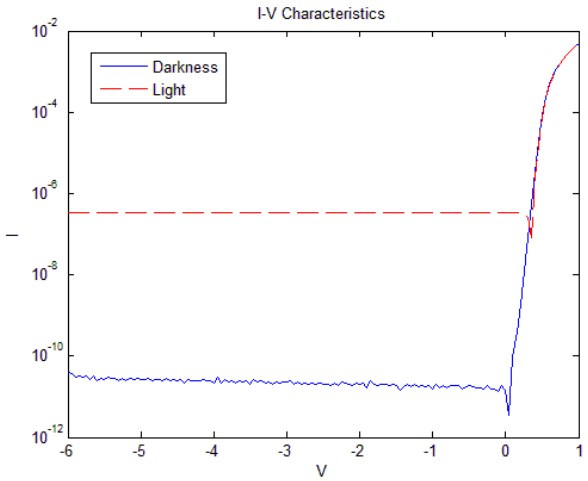


Fig.12. Example photodiode I-V characteristics.

5. Conclusions

We have presented the design of a high precision solar sensor. A set of prototypes has been manufactured to evaluate several parameter influences in sun sensor performance. The designs have been tested and validated, so they are ready for the assembly process and, after that, the calibration stage. CMOS process has been validated, so the future work will be the integration of the sensor and the auxiliary circuits of signal adaptation in the same bulk, leading to a smaller final device than actual.

Acknowledgment

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