NOISE ANALYSIS AND NOISE ESTIMATION OF AN RF SAMPLING FRONT-END USING AN SC DECIMATION FILTER

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ABSTRACT: In this paper we present the noise analysis of an SC filter for RF sampling and downconversion. The filter implementation is made in 0.12 µm CMOS and is primarily intended for WLAN in the 2.4 GHz band and with 20 MHz signal bandwidth. The fundamental noise properties of switched capacitor circuits are discussed while deriving the necessary equations needed for the filter noise calculation. The influence of amplifier noise is also discussed, and a technique to remove low-frequency noise and DC offset from the amplifiers is presented. Finally, a noise estimation of a complete RF sampling front-end is made. Our results are verified by simulations using Cadence Spectre RF simulations.

INTRODUCTION

With the increasing number of standards used around the world today there is an enormous need for low cost multi-standard RF front-ends. The traditional view of software-defined radio (SDR), where the analog-to-digital converter (ADC) is placed directly at the antenna or after the low-noise amplifier (LNA), puts unrealistic requirements on the ADC in terms of sampling rate and resolution resulting in too high power consumption. The key to success is to have an RF front-end architecture that is highly flexible without putting too tough requirements on the ADC. One approach to do this is the RF-sampling front-end shown in Fig. 1. The basic idea is to sample the RF signal after the LNA and do further processing and necessary decimation before AD conversion. Today’s CMOS technologies demonstrate very high speeds, making the RF sampling technique appealing in a context of multi-standard operation at GHz frequencies.

Looking at the RF front-end in Fig. 1, the traditional mixer is replaced by a sampler (zero-IF conversion) and a discrete time switched capacitor (SC) filter. Decimation is performed to decrease the sample rate from a value close to the carrier frequency to a value suitable for AD conversion [1, 2]. A high sample rate is still desired to utilize oversampling in the ADC.

The noise analysis of a zero-IF receiver front-end, which adopts an RF sampling approach, is addressed in this paper. The problem of RF sampling and downconversion has already been discussed in [1, 2, 3]. Besides decimating and bandlimiting the signal, the switched-capacitor (SC) filter has to have a low noise figure as well not to spoil the noise figure of the analog front-end. The noise added by the SC filter should be of the same order as for a traditional mixer based receiver.

In this paper we will describe the chosen filter topology and focus on its noise properties. Even though the theory of noise in SC circuits is widely described in literature it becomes very intricate when dealing with more complicated circuits [4]. The noise properties of the RF sampling filter are derived including the influence of noise from the amplifiers used between the filter sections. The noise calculations are also verified by simulations using Cadence SpectreRF. The last section provides the final conclusions from this work.

RF SAMPLING FILTER TOPOLOGY

The RF sampling filter consists of four cascaded sections of the type shown in Fig. 2. For this particular filter implementation the decimated sample rate should be 1/16 of the carrier frequency. For a 2.4-2.5 GHz carrier frequency, the output rate of 150-156.25 MHz is acceptable in terms of A/D conversion rate. The filter coefficients for one filter section are derived by expanding the expression \((1+z^{-1})^3\) to \(1+3z^{-1}+3z^{-2}+z^{-3}\) [3]. These coefficients, and thereby the capacitor sizes, are therefore scaled as \([1\ 3\ 3\ 1]\). As one can see, four samples are needed to implement the wanted function. However, to maintain a decimation rate of two and to have a time slot for the averaging, three time-interleaved filter banks must be used. The amplifiers between succeeding stages are necessary to avoid unwanted IIR effects due to charge sharing between the cascaded sections. More details about this filter implementation can be found in [3].
NOISE IN SIMPLE SC CIRCUITS

Noise in a sampling circuit must be characterized in terms of the folding effect [5]. The noise at the output of a simple switched capacitor can be expressed by the power spectral density $S(f)$, which is shaped with respect to the sampling frequency $f_S$ and hold time $\tau_h$:

$$S(f) = (1 - \tau_h f_S)4kT R + (\tau_h f_S)^2 \text{sinc}^2(\tau_h f) \frac{2kT}{C_S f_S}$$  \hspace{1cm} (1)

The first term of $S(f)$ can be referred to as the track noise, and the other as the hold noise. Apparently, the track noise is proportional to the on-resistance of the switch and the duty factor $(1-\tau_h f_S)$, but its contribution to the total power spectral density (PSD) can be neglected when the $RC$ time constant is much smaller than the sampling period $1/f_S$, and the hold factor $\tau_h f_S$ does not approach zero. In practice, those conditions are often met and the hold noise tends to prevail over its track counterpart. Most of the power of the noise in the hold circuit is located in the first lobe of the sinc$^2(\tau_h f)$ function, being limited by a “zero” at $f=1/2\tau_h$. The equivalent noise bandwidth of $S(f)$ can be estimated as $1/2\tau_h$, such that the PSD integrated over the whole frequency is:

$$I = (\tau_h f_S)^2 \frac{2kT}{C_S f_S} \cdot \frac{1}{2\tau_h} = (\tau_h f_S) \frac{kT}{C}$$  \hspace{1cm} (2)

Consider the SC circuit shown in Fig. 3. This example will be used to demonstrate how the noise is generated by the switches and propagated to the output. Noise is also introduced by the amplifier. For simplicity the amplifier is assumed to have unity gain and and a single pole AC response. Using the superposition principle the noise contribution from each source can be estimated separately and then summed up with the rest to get the total noise.

During the clock phase $\Phi_1$ the input is first tracked and then held on the sampling capacitor $C_S$, in form of a constant voltage. When $\Phi_2$ and $\Phi_3$ goes high the sampled voltage is passed on to the output capacitor through the two latter switches and the buffer. Note that only the hold component is passed on in this way. The duty factor of the sampling switch is 1/4 so the hold factor is 3/4, while the effective hold factor of the switches clocked by $\Phi_2$ and $\Phi_3$ is 1 (because of resampling), which raises the transferred noise by a ratio $(4/3)^2$. The noise at capacitor $C_S$ has a low frequency PSD of:

$$S_1(f) = (3/4)^2 \frac{2kT}{C_S f_S}$$  \hspace{1cm} (3)

When resampling at the output capacitor we obtain:

$$S_{1,\text{out}}(f) = \frac{2kT}{C_S f_S}$$  \hspace{1cm} (4)

Now, consider the noise from the second switch ($\Phi_2$). When in track mode, the noise is band limited by its signal path to the output and next it is held on the output capacitor with a hold factor 3/4. The following transfer function can be derived:

$$|H(\omega)|^2 = \frac{1}{1 + (\omega R C_p)^2} \times \frac{1}{1 + (\omega R C_{out})^2}$$  \hspace{1cm} (5)

where $\omega_T$ represents the buffer pole (considered here as infinite). The equivalent noise bandwidth of a single pole system is known to be $B_N=1/(4RC)$. Assuming infinite bandwidth of the buffer and that $C_p \ll C_{out}$ a single pole approximation can be used. Knowing this we can estimate the noise contribution of this switch to the output as follows:

$$S_{2,\text{out}}(f) = 4kT R \times \frac{2B_N}{f_S} \times \left(\frac{3}{4}\right)^2$$  \hspace{1cm} (6)

assuming the track noise part can be neglected. Assuming $f_S=500$ MHz, $C_S=250$ fF, and the on-resistance of the switches is 50 $\Omega$, the total noise at the output is calculated to be 140.8 aV$^2$/Hz. This should be compared with the 139.9 aV$^2$/Hz that was obtained from PNOISE simulations using Cadence Spectre RF.

Worth mentioning is also the importance of having the clocks $\Phi_2$ and $\Phi_3$ operating in phase. Particularly when $C_p$ is a small parasitic capacitor. For example, in case $\Phi_3$ is in phase with $\Phi_1$ instead of $\Phi_2$. The signal will be sampled one more time on the small parasitic capacitance, $C_p$, in Fig. 3 before it is transferred to the output. This will severely boost the noise, while the signal transfer function will still remain the same.

Next example is shown in Fig. 4. Here, two time interleaved capacitors are used to collect input samples. Following the same principle as above (Eq. 3-4), the noise coming from the sampling switches $\Phi_1$ and $\Phi_2$ is:

$$S_{1,2}(f) = \frac{2kT}{f_S} \times \sum_{k=1}^{n} \frac{C_k}{(\sum_{k=1}^{n} C_k)^2} = \frac{kT}{C_S f_S}$$  \hspace{1cm} (8)

The noise from the two averaging switches operated by $\Phi_3$ can be calculated after deriving the transfer function. The transfer function for each of the two switches are (assuming $C_p$ is negligible):

$$\frac{1}{1 + (\omega R C_S)^2} \times \frac{1}{1 + (\omega R C_{out})^2}$$  \hspace{1cm} (9)
The noise from switch \( S_1 \) is generated and transferred to the output when using a time interleaved filter section.

Assuming infinite bandwidth of the amplifier and having two equal poles \((C_5=C_{out})\), the noise bandwidth \( B_N=1/(\sqrt{2\times4RC_S})\). The total noise from the two averaging switches is:

\[ S_{av}(f) = 2 \times 4kTR \times \left( \frac{1}{2} \right)^2 \times \frac{2B_N}{f_S} \times \left( \frac{3}{4} \right)^2 \]  

(10)

The contribution from the switch at the output is exactly the same as in previous example (Eq. 7). Using \( f_S=1 \text{ GHz}, C_S=250 \text{ nF} \); and the on-resistance of the switches are \( 50 \Omega \), the total noise at the output in this case is calculated to be \( 41.8 \text{ aV}^2/\text{Hz} \). This should be compared with the \( 45.8 \text{ aV}^2/\text{Hz} \) that was obtained from simulations.

### NOISE IN FIR FILTER SECTION

Consider a practical SC filter section shown in Fig. 5 [3]. The buffer is assumed to have unity gain and a single pole AC response. To simplify, we also assume the switch at the output to be on. The switches \( S_1-S_4 \) would be referred to as the sampling switches, and \( S_5-S_8 \) as the averaging switches. With respect to clock signals, \( \phi_1-\phi_4 \), the noise of each sampling switch is first tracked and then held on the corresponding capacitor in a form of a constant voltage. When the Sum clock goes high the averaging is performed, and at the same time the result is passed on the output capacitor. Only the hold component is passed on in this way. The duty factor of the sampling switches is \( 1/6 \) so the hold factor is \( 5/6 \). Following the same principle as for the examples in previous section, the total noise from the sampling switches \((S_1-S_4)\) is:

\[ S_{SaSw}(f) = \frac{2kT}{f_S} \times \frac{\sum C_k}{(\sum C_k)^2} = \frac{kT}{4CF_S} \]  

(11)

It also shows the advantage of the averaging.

Now, consider noise from the averaging switches \( S_5-S_8 \). In order to find the equivalent noise bandwidth for the two averaging switches the noise transfer function is needed. The noise from switch \( S_5 \) (and \( S_6 \)) has the following transfer function:

\[ |H(\omega)|^2 = \frac{1}{8} \times \frac{1 + (3\omega RC)^2}{1 + (1.5\omega RC)^2} \times \frac{1}{1 + (\omega T)^2} \times \frac{1}{1 + (\omega RC)^2} \]  

(12)

where \( \omega_T \) represents the buffer pole (considered here as a significant band limitation). The equivalent bandwidth \( B_{eq5} \) can be found by comparing the integral of \(|H(2\pi f)|^2\) taken over the frequency range \( f=(0,\infty) \) with \((1/8)^2B_{eq5}\).

Knowing this we can estimate the noise contribution of this switch to the output as follows:

\[ S_{Av5}(f) = \frac{4kTR}{f_S} \times \frac{1}{8} \times \frac{2B_{eq5}}{f_S} \times \frac{2}{3} \]  

(13)

where \( 2B_{eq5}/f_S \) is the folding factor and \((2/3)\) is the hold factor. In a similar way (but with a different transfer function) the contribution of switches \( S_6, S_7 \) can be estimated. In this way the noise from the four averaging switches is:

\[ S_{Av5}(f) = \frac{kT}{f_S} \times \left( \frac{B_{eq5}}{9} + B_{eq6} \right) \]  

(14)

The above behavioral analysis can be compared to a simulation run in Cadence (PNOISE analysis is used). The noise of the switches is modeled using 100 \( \Omega \) noisy resistors at \( T=300 \text{ K} \). The other parameters are: \( C=75 \text{ fF}, f_T=3 \text{ GHz}, f_S=400 \text{ MHz} \). The calculated bandwidths are \( B_{eq5}=B_{eq8}=5.43 \text{ GHz} \) and \( B_{eq6}=B_{eq7}=3.89 \text{ GHz} \).

The noise contributions from the switches in a simple section (Fig. 5) are given in Table 1. As shown, the Spectre simulation results and the estimates derived from the behavioral model for the noise produced by all switches \( S_1-S_8 \) differ by less than 10%. It is also worth to mention that taking into account an input capacitance of the buffer (\~60 \text{ fF}) practically does not change the above results.

In a practical FIR filter where three SC sections operate in parallel [3], the total output noise would increase three times. However, since they are time interleaved the effective hold factor for each section seen at the output is only \( 1/3 \), and for the rest of the cycle a section contributes with no noise power. The sections are clocked by Sum signals in a way so that they do not load one another. This makes the noise contribution of each section to decrease by \((1/3)^2\). The total noise from the three time interleaved sections will then be \( 3 \times (1/3)^2 \) times the noise from a single section. This reduction in noise due to interleaving has also been verified with the simulator resulting in \( 11 \text{ aV}^2/\text{Hz} \).

<table>
<thead>
<tr>
<th>TABLE 1. Noise contributions from a simple SC section.</th>
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<tbody>
<tr>
<td><strong>Behavioral model</strong></td>
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<tr>
<td>Sampling Sw.</td>
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<tr>
<td>Averaging Sw.</td>
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<tr>
<td>All Switches</td>
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</table>
AMPLIFIER RELATED NOISE

The amplifier topology used is shown in Fig. 6. It consists of a single gain stage followed by a source follower. This circuit is chosen for its good linearity and well defined gain, $A_v = [(W/L)_1/(W/L)_2]^{1/2}$ [6].

Now, consider the amplifier to be noisy. Its noise can be modeled as a noise voltage source with PSD composed of a thermal- and a 1/f-part (which are uncorrelated). This noise is limited in frequency by the buffer bandwidth. Additionally, when transferred as a track noise to the output it would experience an extra attenuation by the output sampler. However, when $\omega_T \ll 1/RC$ the latter effect can be neglected and in this case the track noise at the output can be estimated from:

$$S_{B,track}(f) \approx \frac{1}{1 + \left(\frac{\omega}{\omega_T}\right)^2} \times \left(4kT R_{eq} + \frac{A_{1/f}}{\omega}\right)$$

(15)

The equivalent noise bandwidth of the thermal component is $\omega_T/4$ [5] and upon sampling this noise would fold with a factor $\omega_T/2f_S$. Unlike this the 1/f component would not fold since it is narrowband and usually becomes negligible for $f > 10$ MHz. Hence, we infer that the noise contribution of the amplifier would be:

$$S_B(f) \approx 4kT R_{eq} \times \frac{\omega_T}{2f_S} \left(\frac{2}{3}\right)^2 + \frac{A_{1/f}}{\omega} \left(\frac{1}{3} + \left(\frac{2}{3}\right)^2\right)$$

(16)

Here, we consider the output sampler to switch at $f_S$ with a duty factor equal to 1/3. While for the wideband component the hold part prevails, for the 1/f component both the track and hold component must be taken into account. The effect of 1/f noise at low frequency can be reduced in different ways. The simplest approach is to use PMOS transistors instead of NMOS transistors because of their lower 1/f-noise. However, this will give higher thermal noise since the transconductance of a PMOS transistor is lower than for a NMOS transistor for a given power consumption. Other techniques like for example chopper amplifiers [7] can also be used in SC circuits. The DC-offset and 1/f-noise problem is a well known issue for all zero-IF receivers and is usually solved by allowing the low-frequency part of the data to be sacrificed without significant loss of information. In the case where this becomes an issue a low-IF receiver is usually chosen instead. However, there are innovative techniques to improve the 1/f-noise performance of a traditional mixer as described in [8, 9]. These techniques involve dynamic current injection [8] or twice the LO frequency and an extra LO stage in the mixer [9]. In this this paper we will introduce a novel way to get rid of the 1/f-noise, DC-offset, and gain mismatch in the differential amplifier topology shown in Fig. 6, when used in a RF sampling SC filter. The circuit shown in Fig. 7 looks similar to the classical chopper amplifier. To see the distinction, consider this circuit when operating together with an SC filter section following the amplifier. Note that discrete time samples are used in this case. First, let us define the output as the output of the SC section after the amplifier and the input as the output from the preceding stage. The gain of the amplifier is $A = A_1 = A_2$ and the uncorrelated noise of $A_1$ and $A_2$ is $n_1$ and $n_2$, respectively. A DC offset can also be included in $n_1$ and $n_2$. The difference equation is used to derive the signal transfer function (STF) and the noise transfer function (NTF):

$$\text{out}_p[k] - \text{out}_n[k] = \frac{A}{8C}(C\text{in}_p[k] - \text{in}_n[k]) + \frac{C}{8}(n_1[k] - n_2[k]) + 3C(n_2[k - 1] - n_1[k - 1]) + 3C(n_1[k - 2] - n_2[k - 2]) + C(n_2[k - 3] - n_1[k - 3])$$

(17)

Now, taking the $z$-transform of this expression and after some simplification we get the STF and the NTF:

$$\text{STF} = \frac{\Delta \text{out}(z)}{\Delta \text{in}(z)} = \frac{A}{8} \times [1 + 3z^{-1} + 3z^{-2} + z^{-3}]$$

(18)

$$\text{NTF} = \frac{\Delta \text{out}(z)}{\Delta \text{in}(z)} = \frac{A}{8} \times [1 - 3z^{-1} + 3z^{-2} - z^{-3}]$$

(19)

where $\Delta \text{out}(z) = \text{out}_p(z) - \text{out}_n(z)$, $\Delta \text{in}(z) = \text{in}_p(z) - \text{in}_n(z)$, and $\Delta \text{n}(z) = n_1(z) - n_2(z)$. While the signal is lowpass filtered the amplifier noise undergoes highpass filtering instead. The normalized STF and NTF are both plotted in Fig. 8. The great advantage from this is that 1/f-noise, DC offset, and low frequency thermal noise is not affecting the noise performance of the filter anymore. Fig. 9 shows the result of a simulation with and without switching the amplifiers for one filter section. When using this technique Eq. 15 and 16 are no longer valid. We estimate that the noise folding factor would only slightly be affected if $\omega_T$ is large compared to $f_S$, while the 1/f noise component can be neglected.

Further, consider a gain mismatch in the amplifier. Let the gain $A$ be equal to $(A_1 + A_2)/2$ and $\Delta A = (A_1 - A_2)/2$. Deriving the output in the same way as with the noise

![Fig. 6. Amplifier schematic.](image1)

![Fig. 7. Switching of amplifiers to remove 1/f-noise.](image2)
before we get:

\[
\frac{\Delta A}{8} \left((in_p(z) + in_n(z)) \times [1 - 3z^{-1} + 3z^{-2} - z^{-3}] \right)
\]

As seen from Eq. 20 the gain mismatch creates a common-mode signal that is also highpass filtered just as the noise before. Reducing the sensitivity to gain mismatch by the highpass filtering is another benefit from this circuit. The only minor disadvantage of switching the amplifiers as discussed before is when taking its parasitic input capacitance into account. Without the switching the small parasitic input capacitance will only add a week IIR response to the FIR filter (as long as the parasitic input capacitance is small compared to the sampling capacitors). The transfer function in this case is described by:

\[
H(z) = \frac{1}{8C + C_{in}} \times \frac{C + 3Cz^{-1} + 3Cz^{-2} + Cz^{-3}}{1 - \frac{C_{in}}{8C + C_{in}} z^{-2}}
\]

The DC gain of \(H(z)\) is achieved by setting \(z\) to one. As expected \(H(1)=1\) in this case. In case of switching the amplifiers, the value of the charge stored at the parasitic input capacitance will change polarity compared to the case above and the transfer function this time is:

\[
H(z) = \frac{1}{8C + C_{in}} \times \frac{C + 3Cz^{-1} + 3Cz^{-2} + Cz^{-3}}{1 + \frac{C_{in}}{8C + C_{in}} z^{-2}}
\]

and the DC gain is:

\[
H(1) = \frac{8C}{(8C + 2C_{in})}
\]

Using Eq. 23 and \(C=75\ \text{fF}\) and \(C_{in}=60\ \text{fF}\) a DC gain of 0.83 is achieved instead of 1 as above without switching. This is a small disadvantage since the amplifiers input capacitance can be made smaller in case of using the switching technique. This because the \(1/f\) noise (area dependent) and DC offset (related to transistor matching) is no longer a problem and the gain mismatch problem is not considered to be an issue either. This gives the possibility to use smaller transistors in the amplifier, and thereby smaller parasitic input capacitance, without degrading the performance. Without the switching technique large transistors are needed to get low \(1/f\) noise and achieve good matching to reduce DC offset and gain mismatch.

**NOISE ANALYSIS OF COMPLETE RF FIR FILTER**

In a front-end using the SC filter shown in Fig. 10 there will be no or very limited blocker suppression. Therefore, the total gain in the receiver chain is set by the maximum allowed blocker and the input range of the ADC. Maximum signal strength at the antenna is -30 dBm and is transformed to a differential signal of -27 dBm (40 mVpp) at the input of the LNA. At the ADC input 1 Vpp is desired why the required voltage gain, \(G\), is 25 (28 dB). The LNA will provide 16 dB gain and the four amplifiers in the filter 3 dB each.

The front-end should have a noise factor, \(F\), of 10. From this the maximum allowed noise spectral density at the ADC can be calculated as \(S_{ADC,\text{in}} = FkTR_{\text{in}}G^2 = 2588\ \text{aV}^2/\text{Hz}\), where \(R_{\text{in}}=100 \ \Omega\). Now let us calculate the noise contribution from the LNA and the four filter sections. A wideband LNA with a noise factor of 2, 16 dB gain, and 3 GHz bandwidth is used. At the output of the LNA the noise level is \(f_{LNA}kTR_{\text{in}}G_{LNA}^2 = 33\ \text{aV}^2/\text{Hz}\). The noise at the output of each SC section consists of three parts:

- Noise from sampling on the filter capacitors, \(kT/C\)
- Resampled noise from preceding sections
- Noise from preceding amplifier that undergoes noise folding when sampled for the first time

For the four sections in the filter the capacitors have been scaled to improve the noise performance. They are scaled as 1:2:3:4. The sampling noise from SC\(_1\) is scaled up with the decimation rate compared to the operating frequency of the first filter section, and scaled down by the capacitor scaling ratio compared to the first section. The noise contribution from the four sections are therefore scaled as \(1 \times, 1 \times, 4/3 \times, \) and \(8/4 \times\) the noise contribution of the first section. At the output of SC\(_1\) in Fig. 10 the total noise is \(2\times11\ \text{aV}^2/\text{Hz}\) (11 aV^2/Hz as described earlier, \(2\times\) because of differential design). The corresponding bandwidth of the three first amplifiers are 1.65 GHz, 1.1 GHz,
and 860 MHz, respectively. The amplifiers also have a noise power spectral density at the output of 14 aV^2/Hz and a power gain of two. The wideband noise from the LNA is sampled and folded according to:

\[ \sum_k PSD_{LNA} \frac{2BW_{LNA}}{f_S} \frac{C_k^2}{(\sum_n C_n)^2} \frac{1}{3} \]  

(24)

where 1/3 is due to interleaving. Using Eq. 24 and the numerical values \( PSD_{LNA} = 33 \text{ aV}^2/\text{Hz} \), \( BW_{LNA} = 3 \text{ GHz} \), \( f_S = 400 \text{ MHz} \), and the term from capacitor averaging is 20/64. This gives 73.6 aV^2/Hz (22 from SC1 and 51.6 from the LNA). The complete results from the noise calculation (as described above) is shown step by step in Table 2. The total noise spectral density at the output is 1995 aV^2/Hz, to be compared with the 2588 aV^2/Hz allowed at the ADC input in order to get a receiver noise factor of 10. This clearly shows it is fully possible to achieve good enough noise performance using an RF sampling front-end using this type of SC filter for decimation.

### Table 2: Noise contributions from the different parts in the RF sampling front-end.

<table>
<thead>
<tr>
<th>Point in the RF chain</th>
<th>Noise power spectral density [aV^2/Hz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>@ antenna</td>
<td>0.414</td>
</tr>
<tr>
<td>@ LNA output</td>
<td>33.0</td>
</tr>
<tr>
<td>@ SC1 output</td>
<td>22 + 51.6 = 73.6</td>
</tr>
<tr>
<td>@ SC2 output</td>
<td>22 + 2 \times 73.6 + 24.1 = 193.3</td>
</tr>
<tr>
<td>@ SC3 output</td>
<td>29.3 + 2 \times 193.3 + 32.1 = 448</td>
</tr>
<tr>
<td>@ SC4 output</td>
<td>44 + 2 \times 448 + 50.2 = 990.2</td>
</tr>
<tr>
<td>@ the output</td>
<td>2 \times 990.2 + 14 \approx 1995</td>
</tr>
</tbody>
</table>

Obviously, scaling up the capacitor size along with decimation of the frequency plus having amplifiers providing gain>1 reduces the impact of noise imposed on the signal by the following SC sections. The drawback is that wideband noise from the amplifiers undergoes folding. The bandwidths of the amplifiers in this example were quite high and could be reduced. Theoretically those bandwidths do not have to be much larger than the downconverted signal frequency (baseband frequency). The main reason for not having that low amplifier bandwidth is that in case of incomplete settling due to the transients sampling jitter might become a problem.

### SUMMARY AND CONCLUSIONS

In this paper we have carefully analyzed the noise properties of SC circuits exploited in an RF sampling front-end. The noise properties of an SC filter have been derived and verified by simulations. The influence of wideband noise and noise folding from amplifiers has also been analyzed in detail. Moreover, a switching technique used together with the amplifiers has been presented, that solves the 1/f noise and DC offset problem usually associated with zero-IF receivers. Simulation results clearly show how 1/f noise from the amplifiers can be removed. The technique used also reduces the sensitivity to gain mismatch introduced by the amplifiers.

Finally, a complete noise estimation of an RF sampling front-end for WLAN was presented. By using the proposed circuit technique, a receiver noise figure better than 10 dB is feasible. The noise can be reduced further by capacitor scaling and by reducing the bandwidth of the amplifiers. Ultimately, the presented work shows the possibilities of designing a flexible RF front-end by using the sampling and decimation technique and still achieving acceptable noise performance.

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