SC Filter for RF Downconversion with Wideband Image Rejection

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Abstract—In this paper we present an SC filter for RF downconversion using the direct RF sampling and decimation technique. The circuit architecture is generic and it features high image rejection for wideband signals and good linearity. An SC implementation in 0.12 µm CMOS suitable for an RF of 2.4 GHz and 20 MHz signal bandwidth is presented as a demonstrator. Simulation results obtained using Cadence Spectre simulation tools are included.

I. INTRODUCTION

Present approaches to software-defined radio (SDR) are based on the idea of converting the RF signal directly to digital form and then performing all signal processing in the digital domain. This method is not yet successful, as it puts too high requirements on the AD-converter and also asks for very high performance digital signal processing. Looking for new alternatives for an RF front-end, one can replace a traditional mixer by a sampler and implement analog IF filtering using a discrete-time technique, which renders the design to be more robust and more flexible in frequency planning. At the same time a reduction of the sample rate from a value close to the carrier frequency to a value suitable for AD-conversion appears feasible [1,2]. However, a complete direct sampling receiver front-end for multi-standard SDR has not been reported so far. Contemporary integrated CMOS circuits demonstrate very high speeds making the RF sampling technique appealing in a context of multi-standard operation at GHz frequencies.

As for any receiver the image problem appears critical. Basically, a good practice to avoid this problem is using the zero-IF architecture. This approach is well suited for wideband standards [3]. In this case the conveyed digital data is distributed over a wide frequency band, and its low-frequency part corrupted by DC offset and 1/f noise can be sacrificed, usually without significant loss of information.

A design of a zero-IF receiver front-end, which adopts an RF sampling approach, is addressed in this paper. To enable A/D conversion the sampled signal has to be decimated and band-limited. The decimation process introduces new image bands and an appropriate band-selection filter to remove these must be included. This task can be accomplished by SC circuits operating on the available samples. The problem of RF sampling and downconversion has already been discussed in [1,2]. However, a more efficient image suppression is demonstrated here, especially useful for wideband signals, such as those of the Wi-Fi WLAN standards operating in the 2.4 GHz band.

In Section II the concept of the sampling downconversion filter incorporating decimation is derived. The prototype filter model is digital. It scales with frequency and provides efficient image suppression for a wide RF input range. In Section III an SC implementation of the circuit is discussed in detail. Simulation results from Cadence Spectre are shown to validate this design. Section IV provides the final conclusions from this work.

II. FILTER/DECIMATOR PROTOTYPE

Using a simple S/H circuit it is possible to downconvert the RF signal to a predefined IF [4]. Specifically, to avoid the image problem the zero-IF is preferred, i.e. a sampling frequency equal to the carrier frequency. As the sampled signal is discrete in time it can be processed further like a digital signal using an SC filter based on a relevant digital prototype. As a candidate, a CIC decimation filter can be chosen [5], which has the transfer function:

\[ H(z) = \frac{1}{R^N} \left( \frac{1 - z^{-N}}{1 - z^{-1}} \right)^R \]

where \( R \) and \( N \) are natural numbers. In a purely digital implementation the filter is usually arranged in a cascade composed of an integrator (\( N\times \)), decimator (\( R\downarrow \)), and a comb filter (\( N\times \)) as shown in Fig.1.

![Figure 1. Structure of CIC decimation filter.](image-url)
The block in the middle represents decimation by a factor of \( R \), so the following comb filter operates at \( R \) times lower frequency than the integrator. The CIC filter has a low-pass frequency response, which can be estimated based on (1) as
\[
|H(f)|^2 = \left| \frac{\sin(\pi R f / f_s)}{R \sin(\pi f / f_s)} \right|^2
\]
(2)
The image bands occurring in decimation are located at the integer multiples of \( f_s / R \) between 0 and \( f_s / R \). From (2) it can be observed that aliasing from those bands would be limited by the filter suppression from the filter notches. In Fig. 2 the filter performance for \( f_s = 2400 \text{ MHz} \), \( R = 16 \), for both \( N = 2 \) and \( N = 3 \) is shown. For \( N = 3 \) and signal bandwidth of 20 MHz we find the image rejection for the first image band to be around 75 dB. For the following bands at 300, 450, 20 MHz we find the image rejection for the first image band can be found that (3), which includes decimation (4)
\[
H(z) = \left( \frac{1+z^{-1}+z^{-2}+z^{-3}}{2} \right)^N = \left( \frac{1+z^{-1}+z^{-2}+z^{-3}}{2} \right)(2 \downarrow \left( \frac{1+z^{-1}+z^{-2}+z^{-3}}{2} \right))(2 \downarrow) \quad \text{(4)}
\]
which, in fact, makes an FIR filter of the order \( N \times (R-1) \). The poles of (1) have been cancelled and one can expect the corresponding frequency response to be less susceptible to parameter inaccuracies as well. Another advantage would be the possibility of distributing the decimation process so that each block in the cascade operates at lower frequency than the preceding block. Since \( (1+z^{-1})(k \downarrow) = (k \downarrow)(1+z^{-1}) \) it can be found that (3), which includes decimation \( R \downarrow \), can be implemented as follows
\[
H(z) = \left( \frac{1+z^{-1}+z^{-2}+z^{-3}}{2} \right)(2 \downarrow \left( \frac{1+z^{-1}+z^{-2}+z^{-3}}{2} \right))(2 \downarrow) \quad \text{(4)}
\]

III. FILTER IMPLEMENTATION

For this particular filter implementation the decimated sample rate should be \( 1/16 \) of the carrier frequency. For a 2.4-2.5 GHz carrier frequency, the output rate of 150-156.25 MHz is acceptable in terms of A/D conversion rate. The ADC can be of sigma-delta type utilizing the high oversampling ratio in this way. The filter function shown in Fig. 2 can be implemented with \( N = 3 \) and \( R = 16 \) using four cascaded sections of the type shown in Fig. 3.

A. Filter structure

The relevant SC circuit realization of Fig. 3, except for the buffer/amplifier, is given in Fig. 4. The filter coefficients for one filter section are derived by expanding the expression \((1+z^{-1})^3 \) to \(1+3z^{-1}+3z^{-2}+z^{-3} \). These coefficients, and thereby the capacitor sizes, are therefore scaled due to \([1 3 3 1]\). As one can see, four samples are needed to implement the wanted function. However, to maintain a decimation ratio of two and to have a time slot for the averaging switches, three time-interleaved filters must be used as shown in Fig. 5. A new value is fed to the output every second clock cycle. The output sequence from the first of the four cascaded filter sections is then, \((X_0+3X_1+3X_2+X_3), (X_2+3X_3+3X_4+X_5), (X_5+3X_6+3X_7+X_8), \ldots \) are not present in the output sequence of the filter as intended. The clocking needed for one filter section is shown in Fig. 5. The clock signal for succeeding stages is a decimated version of that used for the first section. The buffers/amplifiers between succeeding stages are necessary to avoid unwanted IIR effects due to charge sharing between the cascaded sections. Using an approach where the filter coefficients are zeroed by a reset switch before a new sample is collected, can be used instead of buffers. However, this will introduce an extra loss in the filter transfer function.

The frequency response of the 4-section filter obtained by circuit simulation is shown in Fig. 6. It corresponds very well to the response of the digital prototype (CIC) discussed before (Fig. 2). In Fig. 6 presented are frequency responses

![Figure 2. Normalized frequency response of CIC decimation filter for R=16 and f_s=2.4 GHz (only the first two lobes are shown).](image-url)

Apperently, all the prospective blocks have the same function including simple decimation by 2. With those arrangements (4) appears well suited for an SC implementation. In particular, the advantage of the repetitive structure of (4) can be used, avoiding diverse capacitor scaling needed e.g. when expanding (3) into a sum of components (that we discuss in the next section).
of three different models: (i) ideal switches and ideal buffers, (ii) transistor switches and ideal buffers, (iii) a complete transistor implementation (STM CMOS 0.12 µm process). In the latter case, amplifiers/ buffers of the type shown in Fig. 7 were used between the filter sections. A total gain of about 12 dB was achieved compared to (i) and (ii) where unity gain buffers were used. As seen in Fig. 6 the simulated frequency response of the transistor level implementation match very well with the filter responses of the other models, except for the gain that was added in transistor level implementation. The minimum image rejection achieved in a 20 MHz frequency band around 150 MHz for this filter is >75 dB. This should be sufficient to fulfill the requirements for a WLAN receiver, especially when some pre-filtering is used. The overall linearity of the filter is set by the linearity of the amplifiers. Simulated IIP3 for the whole filter is +2 dBm. This filter combined with a typical LNA of 15 dB gain and IIP3 = -5 dBm, sets the IIP3 of the receiver frontend to -13.6 dBm, which is still sufficient for a WLAN standard, such as 802.11b [8].

The implementation of this filter requires 4×24 unit capacitors (four cascaded sections containing three time-interleaved capacitor arrays of 8 unit capacitors each). One can consider expanding (3) into a sum of components Σak z-k as well, and based on this synthesize the corresponding filter. If the same filter is implemented as one simple block the sequence of samples needed to get the same function for N=3, R=16 is (X0,2X1,3X2,5X4,9X8). The total number of unit capacitors needed then are 3×529 (3× needed to maintain an overall decimation rate of 16 for the entire filter). Clearly, this implementation would entail an excessive area overhead.

B. Buffer Design

The buffer topology used is shown in Fig. 8. It consists of a single gain stage followed by a voltage follower. The gain stage is of common source type with a diode coupled NMOS load. This circuit is chosen because of its well defined gain, $A_v = \left(\frac{W_1}{L_1}\right)^{1/2}/\left(\frac{W_2}{L_2}\right)^{1/2}$, and its good linearity. The nonlinear V/I characteristics of M1 is cancelled out by the nonlinear I/V characteristics of M2 [7]. Furthermore, ac coupling is used at the input for proper biasing of the input transistor M1. Designed for CMOS 0.12 µm process, the buffer of $A_v = 1.44$, in simulations achieved IIP3 = 11.5 dBm and output noise of 8 aV^2/Hz.

C. DC Offset Cancellation Loop

DC offset is a common problem in direct conversion receivers. In our case charge injection due to LO leakage from the switches creates a DC offset. First order compensa-
tion is done by introducing dummy switches operating at the opposite clock phases compared to the main switches. Unfortunately, this technique does not prove to be sufficient. The remaining offset will be removed by introducing a DC offset cancellation loop as shown in Fig. 8. Every time a new sample is transferred to the input of the amplifier a compensating charge is injected or removed by one of the capacitors $C_f$ in Fig. 8. However, this circuit also has a few drawbacks. The low-pass filter at the input of the OTA requires a low cut-off frequency. A signal of frequency lower than this will be seen as a DC offset too, and thereby removed by the DC offset cancellation circuit. The capacitor $C_f$ connected in parallel with one of the time-interleaved filter banks (of total capacitance $8C_u$) during the averaging will lower the gain by $C_f/(8C_u+C_f)$. This implies that $C_f$ should be small. On the other hand, $C_f$ needs to be large enough to compensate the DC offset introduced by the circuit. The charge injected from the clocked switches is proportional to their total gate capacitance and the clock swing used ($V_{DD}$), resulting in $Q=C_{gate}V_{DD}$. A large portion of this will be removed by the dummy switches. The remaining part needs to be removed with charge transferred from $C_f$. The maximum charge that can be transferred by $C_f$ is set by the value of $C_f$ together with the output swing of the OTA. Simulations show that $C_f=50$ fF is enough and this will decrease the gain by 8% ($C_u=75$ fF).

**D. Noise characterization**

Noise in a sampling circuit must be characterized in terms of the folding effect [6]. The amount of noise at the output of a simple switched capacitor can be captured as $kT/C$ distributed in frequency and shaped by $(t_0/3t_f)\text{sinc}^2(t_0/3t_f)$, where $t_0$ denotes the hold time. Its equivalent bandwidth can be estimated as $\pm 0.5/t_0$. For the SC filter with decimation as presented above, all transistor switches and buffers introduce wideband noise. For a given filter section there is noise coming from the previous section, noise imposed by the switches, and by the output buffer as well. Sampled noise of $\pm B_N$ bandwidth undergoes folding with a factor $2B_N/f_s$.

Clearly, larger capacitors help to reduce this effect. Averaging performed in every clock cycle reduces the noise PSD. Buffers with gain $>1$ improve the SNR significantly. The full discussion on the filter noise performance is given elsewhere [9]. In simulations the SC filter achieved a noise figure of 22 dB, which we find an acceptable value.

**IV. CONCLUSIONS**

A downconversion SC filter for a zero-IF receiver has been demonstrated. The filter is tunable in a wide frequency range and can be used e.g. for a WLAN receiver operating in the 2.4 GHz band. It will perform the necessary filtering of the images before decimation. The decimation rate of the filter is 16, which gives an output rate of 150-156 MS/s. The minimum image rejection in a 20 MHz frequency band around 150 MHz is about 75 dB and it is higher for the following image bands (up to 1200 MHz). This is satisfactory and should be sufficient for a WLAN receiver. The implementation of this filter requires 4x24 unit capacitors. By cascading filter sections the required circuit area will be low and a minimum of clock phases to the filter sections have to be distributed. The circuit simulations show a very good match with the established CIC-filter theory. To remove the harmful DC offset extra circuits have been proposed, which only affect the signal at very low frequencies. The noise of the SC filter mainly consists of $kT/C$ noise from its switches, noise introduced by the buffers, and noise imposed by the clock jitter. Gain provided by the buffers (12 dB) improves the noise performance resulting in an acceptable noise figure of 22 dB. The noise contribution can be further reduced by increasing the capacitor sizes. However, the settling-time requirement and the silicon area overhead impose an upper limit on capacitor sizing.

**REFERENCES**


