Thermal challenges of Wide Band Gap power electronics component in electrical vehicle

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Abstract: The cooling of power electronics is a fundamental for the best compromise between efficiency, compactness and cost.

For the next generation of High Voltage boxes we focus here on liquid forced convection cooling. Firstly, some examples of cold plates schematics, and cold plate design constraints, are illustrated. Some potential innovation for the design of these configurations is obtained by simulations via topology optimization (TO); TO offers, thanks to the weak turbulence level, an alternative to the traditional engineer design.

Secondly, the new generation of transistors adopting Wide Band Gap (SiC and GaN) material offers improved features. Also, a recent packaging strategy defined as "Top cooled" is composed of a thermal exposed pad in front of the heatsink, and not anymore onto the PCB.

The packaging size is the key relevant parameter for the cooling design. The size of the exposed pad will influence both the thermal resistance of the thermal path between the die and the heatsink, and the spreading capability of the material. Finally, this influence can be analytically proved, quantified, and experimentally verified. The packaging size will also finally influence the surface of exchange with the cooling fluid, reinforcing this effect.

Keywords: wide band gap, GaN, SiC, packaging, power electronic, cooling, heat transfer, EV, PHEV

1. Introduction

1.1 Requirements for powerelectronic cooling

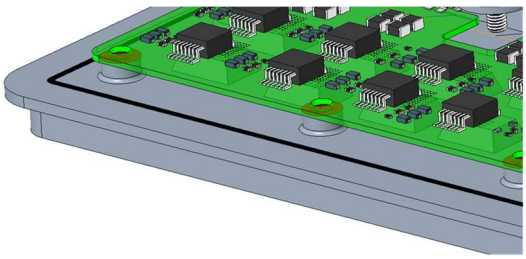

Figure 1: Typical powerelectronic stage

The problem that is addressed in the present paper concerns one or many automotive High Voltage power electronic boards [1] that needs to be passively cooled through a moving fluid. High performances are achieved through some direct contacts, whereas the remaining part of the electronic can be maintained at an acceptable temperature through the overall cooling of the housing and the internal air temperature.

Figure 2 is a general reminder that a trade-off typically exists between the power density to cool (Heat transfer Coefficient) and the losses (i.e. pressure drop, from the pump). Alternative cold plate performances have to be always compared in terms of needed pressure drop. Additionally, the available “budget” of pressure drop must be spitted among the different components to be cooled; that includes the small MOSFET and the large passives components.

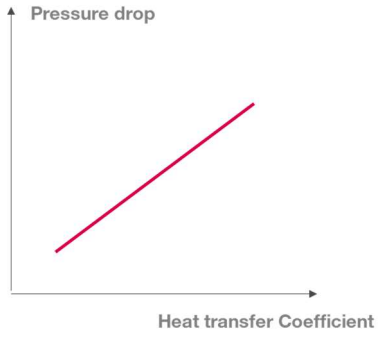

Figure 2: Win/Loss trade-off

1.2 Wide Band Gap materials for car embedded applications.

The Keyes merit factor [3], among others, proposes a comparison of the different materials from a thermal merit point of view [4], Figure 3.

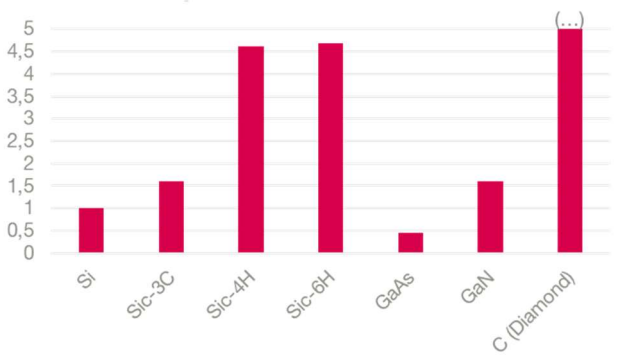

Figure 3: Comparison of materials using Keyes Merit factor (normalised by Silicon)

Obviously, diamond is reaching much higher values. SiC-4H and SiC-6H crystal structures are performing largely better as compared to Silicon. The higher stability versus temperature, figure 4, and the industrial maturity of SiC is also a key factor for its selection, as compared to GaN for instance. GaN exhibit higher potential in terms of efficiency improvement [2].

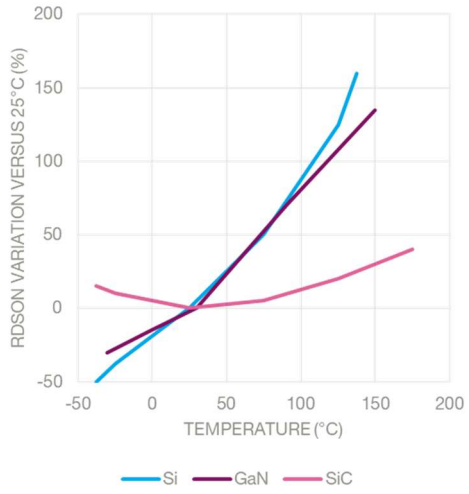

Figure 4: Comparison of materials: stability of RDson versus Temperature

Consequently, two ways are possible to improve power electronics design using SiC [1]: Efficient improvement or power density improvement, or a compromise between both. For instance, efficient improvement can be obtained by replacing IGBT at 75KHz, 30W dissipated by SiC switch version still at 75Khz but dissipating only 18W. Power density can be improved by choosing 200Khz SiC. In that case, the dissipation will be still at 30W, but the PFC coils can be reduced up to 50.

2 Mechatronic implementation

2.1 General considerations

As wide band gap can appear as a game changer, the transistor die packaging can be revisited.

Embedded die is one solution, where the die is inserted directly inside the PCB, and the heat transfer is managed through copper layer and vias design. Embedded die concepts demonstrate an improvement when to compared to medium thermal quality packaging, but only equivalent to the best packaging [5,6].

Integrated module is a second option: few dies are integrated inside a separate module. For these configurations, high thermal performance is usually expected when materials such as ceramics are employed. This solution is widely used in the design of inverters. This interesting but also challenging solution of integrated modules for On Board Charger (OBC) and converters Direct Current Direct Current (DCDC) will not be treated in the following as the paper only focuses on the analysis of more standard and affordable SMD components

2.2 SMD components implementation

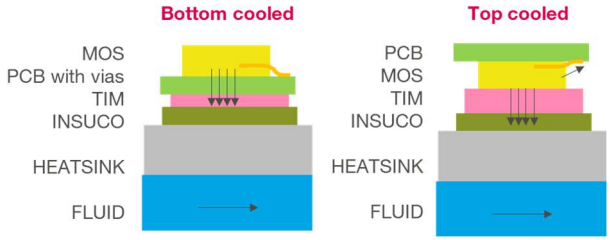

Figure 5: Bottom and Top cooled SMD mechatronic implementation

Nowadays, the thermal bottleneck for bottom cooled packaging concerns the maximum PCB temperature; this in turn requires potentially to increase the PCB class, thus producing a raise in the effective cost of the configuration. For top-cooled components, the potential bottleneck concerns 1. the thick TIM that is needed to compensate the mechanical tolerances; 2. the maximum solder temperature of the electrical connection, as the component is still conductively connected to the PCB by it.

For both packaging, the thermal resistance of the electrical insulation layer, when needed, has also a dramatic thermal penalty.

Additionally, suppliers of top-cooled packaging are promoting the possibility to preserve a clean (free) PCB surface at the opposite side of the FETs; the free surface can therefore be exploited for the placement of other components, thus increasing the

overall power density. However, this view is highly optimistic, as multiple constraints on layout and mechanical integration can limit the benefit of top-cooled component implementation.

Regardless of the positioning (bottom or top-cooled), how to increase the power density of MOSFETs still remains an open topic. In fact, reduced size packaging is obviously improving the power density; nonetheless, the challenge to cool them becomes more evident when comparing a typical MOSFET size and the smallest structure that can be produced in mass with a Die Cast process: MOS cooling is performed by only few pins, instead of the entire pin array arrangement.

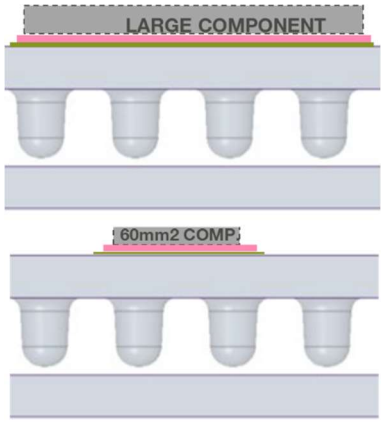

Figure 6: Comparison of a large component and a 60mm2 Mosfet on top of a typical Pin-array cold plate. Bottom appears the pin array that is immerged in the main fluid flow.

3. Thermal Performance quantification

For one concern high voltage boxes as On Board Chargers, filters and possibly converters (from high voltage battery to low voltage battery), the thermal study focus mainly on steady states.

From modelling point of view, the problem can be simplified into thermal resistances series. For top-cooled packaging, at minimum it consists in the junction-to-exposed Rth, i.e. internal to the packaging, followed by the intermediate material, then by the heatsink (aluminium bae and convective heat transfer to the fluid) :

$$Rth_{tot} = Rth_{jc} + Rth_{IM} + Rth_{heatsink} \quad [1]$$

The internal thermal behavior can differ largely from one MOSFET manufacturer to another, with typically Rth_{jc} from 0.2 to 1 °K/W.

The intermediate material (IM) layer accounts for thermal Interface Material, electrical insulation layer when needed. It is playing the main role in the determination of the overall thermal resistance. An overview including High Voltage insulation is proposed Figure 7. Expensive materials as ceramic are excluded from this view. The range covers the other different possibility of materials, and for bottom-cooled, the different possibilities of vias.

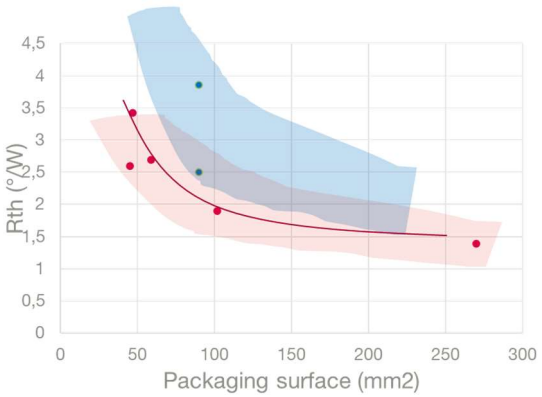

Figure 7: Thermal resistance for different MOSFET. Points: measurements. Line: 1D model. Semi-transparent area: range. Grey refers to bottom-cooled, pink refers to top-cooled

if bottom cooled, the thermal resistance of the PCB is added, even if the TIM thickness can be largely reduced. However, another important effect is due to the difference between the packaging surface and the exposed pad surface. In bottom-cooled, the electrical connection and the thermal exposed pad are on the side, a creepage distance is needed. In top-cooled, the electrical connection and the thermal exposed pad are opposite, meaning that almost the complete packaging surface can be covered with the thermal exposed pad. This effect becomes more predominant when the packaging becomes smaller and smaller. At some point, only few vias are compatible with small packaging size.

Still Figure 7, the points refers to measurements done with different Wide Band Gap technologies and different tested components, but with the same interface material conditions. Lastly, it is shown that the middle tendency is correctly captured by a one dimensional model, i.e.

$$Rth_{IM} \sim 1/\text{Surface} \quad [2]$$

At some point, the thermal spreading has to be considered to correct the 1D assumption. Analytical solutions can be derived for simple single isotropic materials [7], and even for multiple, possibly orthotropic, materials [8]. The spreading correction is mandatory to correctly model the heat transfer in the heatsink base and therefore the expected surface of exchange with the fluid.

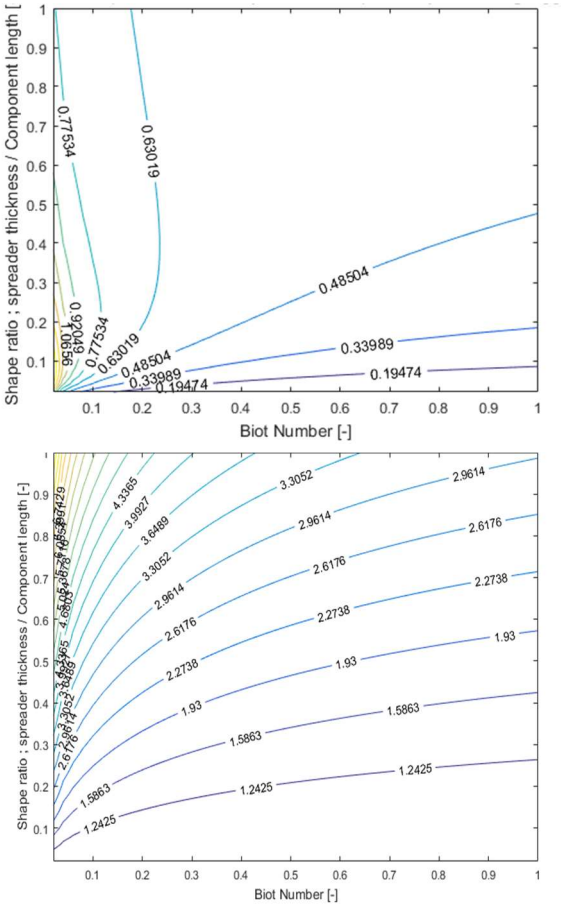

Figure 8: Coupled Conduction-convection in the solid (as cold plate base). Top: Non dimensional thermal resistance. Bottom: Non dimensional temperature cone width

The result of [7] is given for a single material figure 8. The thermal resistance and the temperature width at bottom position are declined as :

$$Rth_{adim} = Rth * k * L_{comp} \quad [3]$$

$$Width_{Temp} / L_{comp} \quad [4]$$

The spreading enlargement, estimated from Schweitzer and Chen approximation [9] is then presented. Typically, a temperature cone enlargement is expected in a aluminum DieCast base up to a factor 2 in direction, a factor 4 in surface.
Even if this spreading effect has to be accounted for, the surface resulting from the upper layer, the previously mentioned interface materials, is still a key factor here. In the interface material, it was linked to the solid conduction. Here, it is linked to the convective surface between metal and fluid that can be reached by the temperature cone.

4. Simulation approaches

4.1 Multidimensional Simulation approach

Heat transfer is a multi-centuries domain, and it is expected that engineering design can propose efficient cooling. Even if other interesting technologies exist, the upcoming parts are focusing on well-established and flexible Die Cast aluminium cold plates in order to illustrate the design process.

In addition to the quantification of the section 4, modern simulation software can assist in the design of overall configurations by means of the so-called “digital twin”. To do so, the (Fourier’s) heat balance equation is solved in the solid domain; the mass, fluid momentum balance, and heat equations are solved in the fluid domain. For a fast and efficient numerical resolution, the two time-steps that differs largely should be resolved separately and coupled.

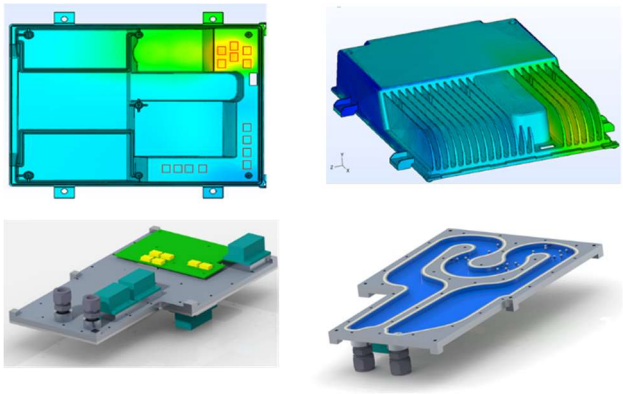

Figure 9: Top: air-cooled example. Bottom: liquid-cooled example.

The design methodology and its cooling capability is tested initially for air-cooled conditions and then for liquid cooling (Figure 9), where MOSFET are implemented, and passives (transistors, coils) are approximated using simple resistances. In air-cooled conditions, the agreement simulation versus experiment is very correct (Figure 10).

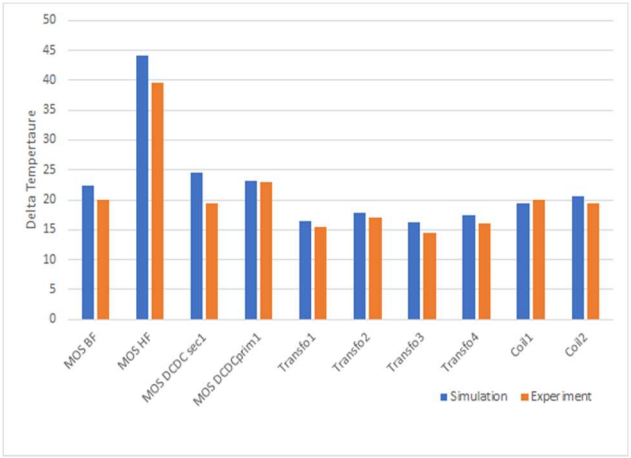

Figure 10: Air-cooled example; comparison simulation/experiment

For liquid cooling conditions, Figure 11, some compromises have to be found between flow velocity, pressure drop in bends, and local surface increase as pins or fins.

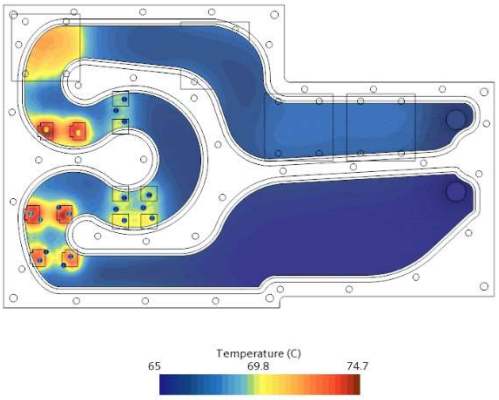

Figure 11: liquid-cooled example; simulation prediction of skin temperature

4.2 Potential breakthrough: alternative simulation approach

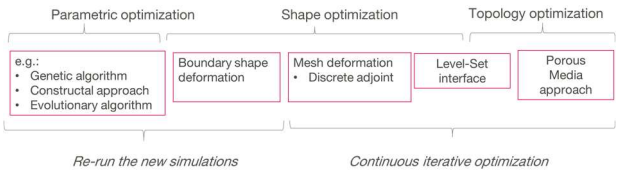

Figure 12: Categories of optimization approaches

Optimization is a type of simulation that deals with different possible categories: parametric optimization; shape optimization or topology optimization (Figure 12). Some of its key advantages are : the generation of design concepts; the ability to balance different objective functions; its potential automatization for R&D cost diminishing. One category, the topological optimization, is the subject of the present paper. Topological optimization is for instance widely used in structural mechanic design. O. Pironneau, following control theory, proposed a first approach to Fluid Mechanic in 1974 [10]. Only recently, Dede [11] and others, demonstrated the possibility for application to convective heat transfer. As turbulence remained a modeling issue, Dwight & Brezillon proposed the so-called “frozen turbulence” as an interesting compromise when instabilities and large eddies are not playing a major role [12].

In the present example, fluid and thermal are considered, including the (fixed) solid geometry. The coupling with the solid areas is treated with Conjugate Heat Transfer. Incompressible fluid (e.g. Poisson solver) with temperature equation is solved. K-eps turbulence model (frozen turbulence during optimization) is adopted. Finite-Volume approach is used in OpenFOAM platform development. One single material - in the form of a porous media - is adopted through the Random Approximation of Material Properties (RAMP). Adaptative Mesh refinement (AMR) is also applied to reach the needed level of details. The numerical solvers are modified with the implementations of a solution regularization (Helmotz filter) and of the Method of Moving Asymptotes (MMA) for the optimization evolution. The algorithm follows the steps : 1) AMR; 2) primal problem; 3) adjoint problem; 4) solution update with sub-looping between 1-4 and 2-4. For more details, the readers are encouraged to refer to the reference [13].

Boundary conditions also request some modifications: whereas in academic testcases the skin temperature is imposed at some locations and the outlet flux increase is the optimization criterion, in power electronics typically the flux is imposed at the component case locations, the outlet flux is then conserved, and the component case temperature diminishing is the optimization criterion. As seen in the requirement section, this criterion must be balanced together with the pressure drop limitation to define the objective function.

It is presented here a simple testcase where three areas have to be cooled, with inlet and outlet that are imposed to be on the same side, Figure 13. Even bidimensional optimization (afterward extruded) present some interesting features. For instance, a deflector is generated by the solver to derive a part of the flow to the opposite side. Continuing further with 3D simulations, the optimization is reducing the pressure drop by rounding the angles, reducing the (initially recirculating) dead zones. Fins-like structure are generated that participate both to the cooling and to the flow deflection. Some areas look more complex, as a kind of pins. Obviously, such geometry should be reworked in order to guarantee the manufacturing.

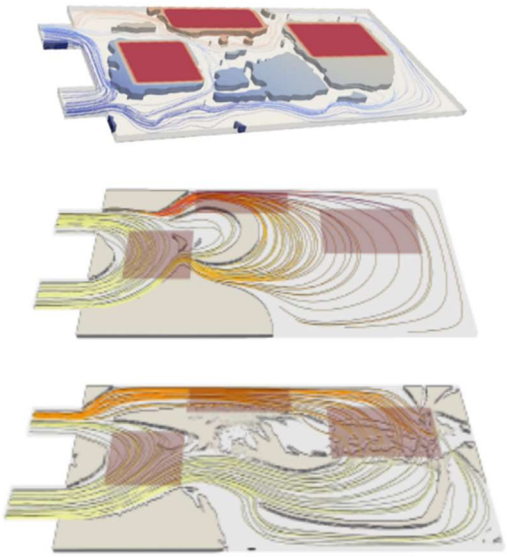

Figure 13: Proof of concept: Simulations results with 3 components. Alpha threshold is superimposed with streamlines. Top: 2D simulations extruded. Centre: 3D simulations, objective function set for pressure drop. Bottom: objective function set for component temperature.

5. Conclusion

Wide Band Gap components are expected to support the increase of power density of the embedded power electronics of electrified mobility.

Logically, the main factor driving the implementation is the power density. When possible, the spreading of the small thermal spot should be encouraged by the design of the thermal path.

Traditional and innovative simulations can support the design process of the cold plate. Topological optimization can be a powerful tool for cold plate design, first by generating ideas for fluid-thermal designers; later possibly by Identifying some compromises pressured drop / efficiency and generating designs. An overall increased efficiency of R&D is then expected with the computational time decrease tendency. However, many opened topics as absolute/local minimum proof, experimental validations, sensitivity analysis still need to be clarified.

6. Acknowledgement

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8. Nomenclature

Bi: Biot number, Bi = h_{comp}.d /k

c Velocity of light

d: depth of the metal

h fluid convection coefficient

k: Metal conductivity

L_{comp}: width of component

KFM Keyes Merit Factor $KFM = \lambda\sqrt{cV_{sat}/4\pi\varepsilon}$

V_{sat} semiconductor limiting velocity for electron motion

ε semiconductor dielectric constant

λ semiconductor conductivity