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FPGA-Based Real-Time Simulation of Finite-Element Analysis Permanent Magnet Synchronous Machine Drives

Christian Dufour, Jean Bélanger, Simon Abourida, Vincent Lapointe
Opal-RT Technologies, 1751 Richardson, suite 2525, Montréal (Québec), Canada
tel : 514-935-2323 fax : 514-935-4994
www.opal-rt.com

***Abstract*- This paper presents a real-time simulator of a permanent magnet synchronous motor (PMSM) drive based on a finite-element analysis (FEA) method and implemented on an FPGA card for HIL testing of motor drive controllers.**

The proposed PMSM model is a phase domain model with inductances and flux profiles computed from the JMAG-RT finite element analysis software. A 3-phase IGBT inverter drives the PMSM machine. Both models are implemented on an FPGA chip, with no VHDL coding, using the RT-LAB real-time simulation platform from Opal-RT and a Simulink blockset called Xilinx System Generator (XSG).

The PMSM drive, along with an open-loop test source for the pulse width modulation, is coded for an FPGA card. The PMSM drive is completed with various encoder models (quadrature, Hall effects and resolver). The overall model compilation and simulation is entirely automated by RT-LAB. The drive is designed to run in a closed loop with a HIL-interfaced controller connected to the I/O of the real-time simulator.

The PMSM drive model runs with an equivalent 10 nanosecond time step (100 MHz FPGA card) and has a latency of 300 ns (PMSM machine and inverter) with the exception of the FEA-computed inductance matrix routines which are updated in parallel on a CPU of the real-time simulator at a 40 us rate. The motor drive is directly connected to digital inputs and analog outputs with 1 microsecond settling time on the FPGA card and has a resulting total hardware-in-the-loop latency of 1.3 microseconds.

I. INTRODUCTION

In the past, motor controllers were typically developed and tested by using a real motor drive very early in the design process. However today, it is more common to test controllers using simulated motor models in a real-time environment. This methodology offers several distinct advantages. For example, the simulated motor drive can be tested with borderline conditions that would damage a real motor, often a costly prototype. The motor itself may be under development in parallel to the controller and therefore may not even be available for testing. While testing, a controller is interfaced with the real-time simulated motor drive through a set of proper I/Os: this is called hardware-in-the-loop (HIL) simulation. Such motor drive simulation is required by hybrid vehicle OEMs and other motor drive manufacturers to accelerate development and testing time by using real-time simulation before making tests on physical prototypes [5].

A digital motor drive controller can have a very small sampling time below 10 microseconds and therefore requires that the real-time simulated motor has a computational time much lower than this value. This requirement exists because the computational time for the model (including the I/O access times) adds a delay in the loop of the final closed-loop response of the controlled motor. If this added delay is too large (a real motor has no such latency), the HIL simulation may diverge from the controller response with a real motor.

Additionally, in applications with pulse width modulation (PWM) frequencies greater than 10 kHz and with PWM-synchronized acquisition of the analog input signals by the controller, the simulator must have a sample rate small enough for its analog outputs to generate the PWM waveform with enough resolution. For example, synchronous acquisition can be tricky if the simulator generates less then 10 analog output points (e.g., motor currents) per PWM period.

Another point of concern is the precision of the model used. Most PMSM drive simulators in use today are based on Park two-axis models, which make important precision-limiting assumptions regarding flux distribution and electric torque production.

Finite-Element Analysis-based methods [1][2] can solve this accuracy problem. In [1], a real-time simulation of a FEA-based PMSM drive was demonstrated using RT-LAB.JMAG package from Opal-RT, the RT-LAB implementation of JMAG-RT, from the Japan Research Institute (JRI).

Finally, an even more difficult challenge is to design an automated electronic control unit fault insertion testing (FIT) system, where the response of the microcontroller software to electronic component level failures is verified. FIT is an essential part of the validation of safety critical automotive electronics. This requires high-bandwidth test equipments because of the typically high slew rates that arise from electronic equipment faults. FPGA-based HIL simulation offers a solution to this challenge because of its ultra-low latency.

In this paper, we report on an FPGA-based real-time simulation of FEA-modeled permanent magnet synchronous machine drives. The proposed model combines the advantages of high accuracy FEA-methods and ultra-low latency of FPGA-based simulation.

II. PROPOSED METHOD FOR FEA-BASED SIMULATION OF A PMSM DRIVE ON AN FPGA CARD.

The proposed PMSM model is a phase-domain model capable of simulating either FEA-type, PMSM (sinusoidal back-EMF) or BLDC (trapezoidal back-EMF and no rotor saliency) models using the fixed-point arithmetic feature of XSG. An IGBT inverter model drives the machine on the FPGA. It is connected, on the FPGA card itself, with a resolver connected to 1 us D/A converters and quadrature encoder model connected to 10 ns resolution digital outputs. Along with 10 ns resolution digital inputs for IGBT gate capture, it results in a very high bandwidth motor HIL test system. Such a motor HIL test system presents several interesting characteristics such as:

- The FEA machine model has superior precision over standard (i.e. single reference frame) Park d-q model. FEA models simulate real motor characteristics like cogging torque and saturation of inductances.
- An 3-phase IGBT inverter that includes switching losses and voltage offset drops is modeled on the FPGA itself. The inverter is driven directly from the simulator digital inputs with 10 ns accuracy.
- The complete motor HIL has an input-output latency under 1.5 us (300 ns for the PMSM and inverter alone) and 10 ns resolution digital inputs for IGBT gate capture. The model is suitable for testing motor controller with sample rates in the 5-10 us range.
- The 1 us analog output rate enables the test of motor drive with high frequency carrier. For example, with 50 kHz PWM, the simulator can output PWM current waveform with good resolution (20 points per period with 1 us D/A).
- The model implements advanced test features like neutral point stator voltage sensing, motor short-circuit and open-phase testing. Other modules can be implemented like minimum dead–time insertion or other user-defined models made with Simulink XSG block programming language.

The latency is defined here has the time delay occurring between a change in the digital input level of the IGBT gate and the corresponding response in the motor currents (i.e. change of slope) seen at the analog outputs.

FPGA simulators of induction motor drives have been proposed in the literature [6] using custom-made floating-point arithmetic. The proposed model is made with the RT-LAB-XSG real-time simulator. Using Xilinx System Generator block set, a fixed-point model of the PMSM drive equations have been derived and implemented on the FPGA card. Only the inductances matrix update is made on the CPU in synchronism with the FPGA model. To enable real-time speed, the inductance and nominal speed Back-EMF tables are pre-computed in this approach before the real-time simulation takes place.

A. Computational engine model separation

In the proposed approach, the electric equations of the PMSM and its IGBT inverter are computed on the FPGA computational engine. This notably includes the 1-D nominal speed back-EMF table. On the other part, the 2-D inductance inverse matrixes $L^{-1}(\theta,I_{abc})$ as well as the electric torque are computed on the CPU and transmitted on the FPGA where interpolation methods are used to up-sample the inductance at 10 ns rate. Storing the inverse of the inductance matrix table on the FPGA itself is difficult and is under investigation. The slower update rate of the inductance value only slightly affects the current distortion at high speed (12000 RPM) and does not affect much the computed torque. It is anyway normal to compute the electrical torque on a slower computational engine because it is used in mechanical equations.

By storing the nominal speed Back-EMF profile on the FPGA, the real back-EMF voltage is found by simple scaling of this stored value by the actual speed.

Figure Fig.1 describes the model separation for HIL simulation of FEA-based model of a PMSM drive. The PMSM drive equations are solved on the Opal-RT OP5130 FPGA card while the PMSM inductance values are computed on a CPU at slower rate. Once again, the FEA model data are pre-computed from JMAG-RT software, from the Japanese Research Institute. This results in a JMAG .rtt file which is used by RT-LAB. At run time, the inverse of the inductance matrix is computed on a CPU of the simulator. Both CPU and FPGA parts of the simulator communicate synchronously through Opal-RT SignalWire link. A console PC (not shown) monitors and controls the real-time simulation process.

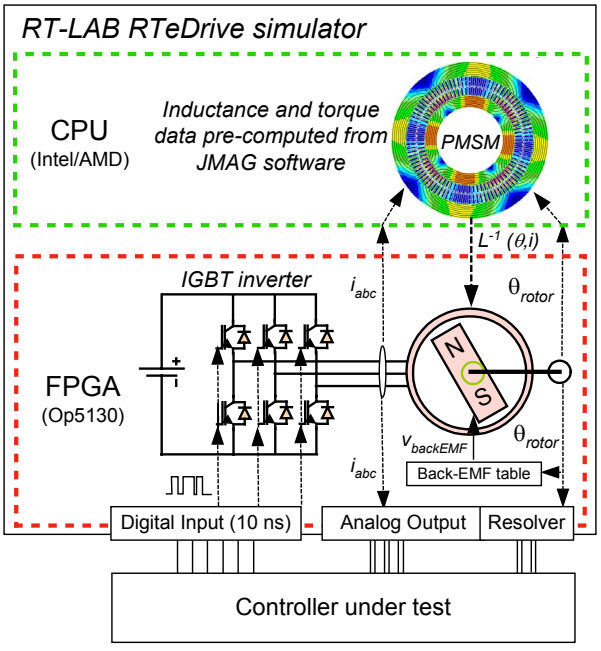

Fig.1. Real-time simulation of FEA-based PMSM drive on an FPGA chip

B. PMSM equations with star connected windings

The general PMSM equation in the phase domain is:

$$[L]^{-1}\int(V_{abc}-\frac{d\psi_{abc}}{dt}-RI_{abc})dt=I_{abc} \qquad (1)$$

where

$[L]$ is the inductance matrix, $L=\begin{bmatrix}L_{aa} & L_{ab} & L_{ac}\\ L_{ba} & L_{bb} & L_{bc}\\ L_{ca} & L_{cb} & L_{cc}\end{bmatrix}$,

and I_{abc} is the stator current inside the winding, ψ is the magnet flux linked into the stator windings, R is the stator resistance and V_{abc} is the voltage across the stator windings.

As mentioned in [3], the star connection is the most common connection in industrial applications due mainly to higher efficiency and smoother torque. The proposed model assumes a star connection and benefits from this because it simplifies the resulting machine equations.

Indeed, in the case of star connected stator windings, there are only two independent state variables because one winging current is defined as the sum of the two other currents $i_a - i_b = i_c$ With this, the following a rank-2 state-space equation is found:

$$\begin{bmatrix}V_{ac}\\ V_{bc}\end{bmatrix}-\frac{d}{dt}\begin{bmatrix}\psi_a-\psi_c\\ \psi_b-\psi_c\end{bmatrix}-\begin{bmatrix}R_a+R_c & R_c\\ R_c & R_b+R_c\end{bmatrix}\begin{bmatrix}i_a\\ i_b\end{bmatrix}=Ldi/dt \qquad (2)$$

with $Ldi/dt=\begin{bmatrix}L_{aa}+L_{cc}-L_{ac}-L_{ca} & L_{ab}+L_{cc}-L_{ac}-L_{cb}\\ L_{ba}+L_{cc}-L_{bc}-L_{ca} & L_{bb}+L_{cc}-L_{bc}-L_{cb}\end{bmatrix}\frac{d}{dt}\begin{bmatrix}i_a\\ i_b\end{bmatrix}$

This is important when programming these equations in the FPGA using fixed-point arithmetic because it diminishes the FPGA resources requirements. For implementation, all values are scaled in their respective per-unit bases to facilitate fixed-point scaling. Most operations are made with 18 bit quantities (matching the embedded multiplier bit length of the Virtex II-pro FPGA chip) with the exception of the flux integrators, which are made with 47 bit multipliers and adders.

C. RT-LAB RTeDrive Real-Time Simulator

The PMSM drive was implemented using the RT-LAB real-time simulation platform. RT-LAB is a real-time simulation platform that enables the distributed simulation of complex electromechanical devices, power systems, and controllers on multi-CPU/FPGA targets. Some devices (e.g., mechanical equations, speed controllers, large power systems) can be implemented in Simulink with Intel or AMD microprocessors as the real-time simulation targets. The PMSM model presented in this paper is implemented in XSG with the FPGA card as a target. RT-LAB manages communication between the CPUs, the FPGA card, and the console PC. Communication between the CPU and the FPGA card is made with a high-speed link called SignalWire (1.2 Gbit/s, 200-ns latency).

The complete PMSM drive model was implemented using RT-LAB 8.1 software with XSG support. The models were first designed in Simulink using the XSG blockset. RT-LAB then targeted the different subsystems to their respective hardware. The target hardware for RT-LAB consisted of PCs (Intel or AMD) with support for multi-processor/multi-core configurations and, for XSG models, an Opal-RT FPGA card with embedded digital I/O (10-ns resolution), analog inputs (2-microsecond rate), and analog outputs (1-microsecond rate). The Opal-RT FPGA card used in the tests is based on the Virtex II Pro XC2VP7 chip

To use the simulator for FPGA simulation of a FEA-based PMSM drive, the user has to do the following steps:

1- Obtain a JMAG-RT description file (.rtt) from the physical characteristic of the motor.

2- Extract the nominal speed Back-EMF voltage using a routine provided with the simulator.

3- Compile the model. RT-LAB will automatically call the proper code generation program (RTW or XSG) and generate executable file and bitstreams at this point.

4- Load and execute the model on mixed CPU/FPGA targets with HIL-connected controller or with open-loop, constant speed, sinusoidal/PWM voltage source (as in the tests presented in this paper).

This process is described in Fig.2 below.

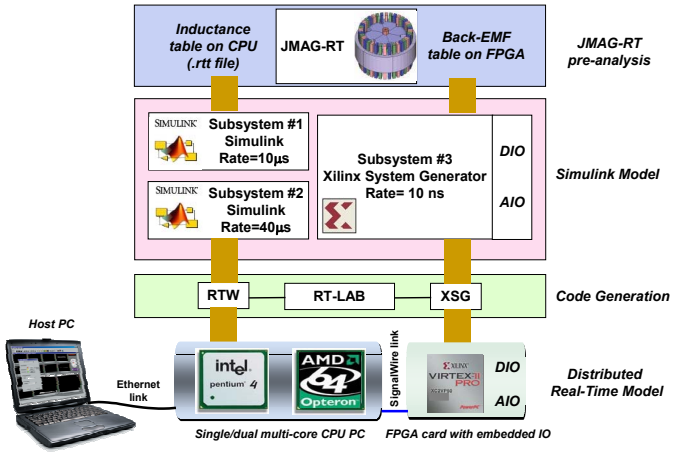

Fig.2. Workflow structure of the RT-LAB real-time simulator from the model specification to the real-time execution

OpXSG-MachDrive FPGA library

Opal-RT offers a library of advanced motor drive models called OpXSG-MachDrive. This library of FPGA IP-core contains the following device models: phase domain PMSM, BLDC machine, JMAG-based PMSM (presented in this work), resolver encoder, Resolver-to-Digital decoder, quadrature encoder, Hall effect sensors, 3-phase inverter model and PWM modulator with dead-time. Because the library is made from Xilinx System Generator blockset, user can also program its own custom models.

III. VALIDATION TESTS

In this section, we present actual simulation results obtained from the real-time simulation on the FPGA. The first objective of these tests is to validate the model against some references. The first test verifies the coherence of the FEA-model with a standard linear Park model. The second test compares the average electric torque produced by the real-time FPGA model of the FEA-based PMSM drive against a reference simulation made at small time step (1 us) with JMAG-RT. The correctness of the PWM inverter model is then verified, especially with regards to dead time. The last tests verify that the model correctly simulates the motor currents as they would be seen by an actual controller though the sensors. In particular, we want to verify that current harmonics are correctly simulated at the analog outputs of the simulator.

The proposed tests are made in open loop mode. This means that the rotor speed and stator frequency are set equal like if the motor shaft had infinite inertia. This is sufficient to test current and torque loops of vector controller. The rotor speed is anyway a relatively slow varying quantity with regards the electrical bandwidth of the drive.

A. Permanent magnet motor used for the tests

The motor used for the tests is a 4-pole internal permanent magnet (IPM) machine with 24 slots and rotor outer diameter of 55 mm. The motor is rated at 1 kW and 12000 RPM. It has a magnet flux of 0.16 Wb and stator resistance of 3.3Ω.

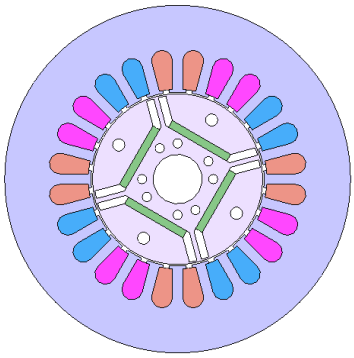

Fig.3. Cross-sectional view of the PMSM used in the tests

B. Open-loop FPGA simulation of FEA-based PMSM model and comparison with sinusoidal flux and linear inductance model

This simulation example demonstrates the difference between FEA-based and sinusoidal flux and inductance model (equivalent to a Park model but not using the Park transform unlike the model proposed in [4]). Both models are implemented in the FPGA using very similar calculation structure with the exception of the inductance calculation made on a CPU of the RT-LAB simulator for the FEA model. In the case of sinusoidal flux machines, the complete model executes on the FPGA including the inductance calculation (stored in a table).

For the test, sinusoidal 3-phase voltages are applied to the motor terminals. Figures 4 and 5 show well the difference between standard Park and FEA-based PMSM models. The two figures are plotted from actual real-time simulation data as they are view in the RT-LAB Console. The figure shows the non-sinusoidal nature of the Back-EMF voltage FEA-based model. This Back-EMF profile, along with the cogging torque and non-linear inductive nature of the PMSM motor results in important torque ripples, which are not simulated by the Park model. In that case of the FEA-based model, one can notice the presence of a 12th harmonic component on torque, current and Back-EMF voltage because of slots effects.

The figures also show a good coherence between the FEA-based model and Park model in the sense that for similar Back-EMF (i.e. same maximum amplitude) and inductance profiles (not shown), the current and torque have similar average values.

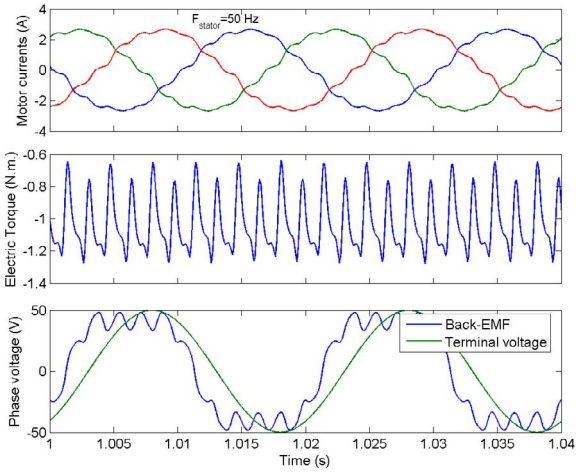

Fig.4. Motor currents, electric torque, terminal and Back-EMF voltages for JMAG model

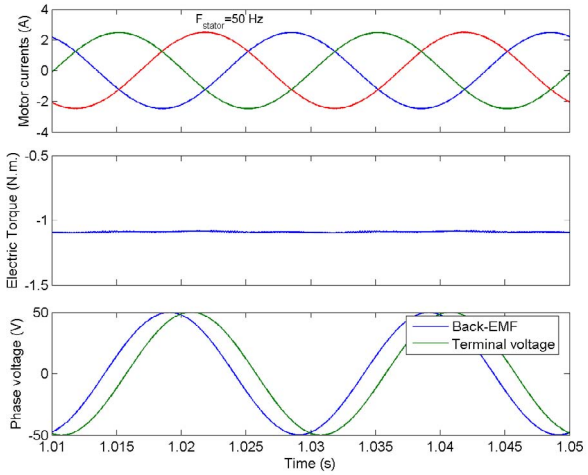

Fig.5. Motor currents, electric torque, terminal and Back-EMF voltages for PMSM models

In the figures, the negative torque means that the motor runs in regenerative mode. To produce positive torque, the terminal voltage has to be shifted ahead of the Back-EMF.

C. *Average Electric torque production*

In this test, we compare the average electric torque production of the FEA-based FPGA model with a simulation model using RT-LAB.OpJMAG package running at 1 us. The OpJMAG package is basically the RT-LAB adaptation of the JMAG-RT software from JRI.

The test is conducted in open-loop with a sinusoidal voltage source with variable frequency and phase angle with regards to the rotor position.

In table 1, the bold entries are from JMAG-RT (RT-LAB. JMAG) models running at 1 us and serves as reference. One can observe that the error is under 1% for most entries not close to null torque. Small average torque measurements are made difficult because the motor as a (zero-current) cogging torque amplitude of 0.35 N.m. At null speed, the torque depends on the rotor angle itself and only the null result is shown.

TABLE 1
COMPARISON OF AVERAGE TORQUE BETWEEN
FEA-BASED (OPXSG_JMAG) AND JMAG-RT (**BOLD**) MODELS

		Stator voltage angle vs. Back-EMF (Degrees)				
Stator frequency (Hz)		-30	-15	0	15	30
	-400	-1.572 **-1.581**	-0.688 **-0.689**	0.003 **-0.004**	0.678 **0.668**	1.557 **1.539**
	-100	-1.430 **-1.438**	-0.640 **-0.646**	0.006 **-0.004**	0.608 **0.604**	1.394 **1.391**
	-50	-1.030 **-1.039**	-0.509 **-0.514**	-0.002 **-0.005**	0.481 **0.480**	1.093 **1.092**
	-10	0.051 **0.047**	-0.030 **-0.030**	-0.003 **-0.001**	0.096 **0.097**	0.246 **0.246**
	0	0 **0**	0 **0**	0 **0**	0 **0**	0 **0**
	10	-0.247 **-0.246**	-0.098 **-0.097**	0.002 **0.001**	0.032 **0.030**	-0.046 **-0.047**
	50	-1.090 **-1.088**	-0.479 **-0.479**	0.008 **0.005**	0.519 **0.514**	1.045 **1.039**
	100	-1.384 **-1.381**	-0.601 **-0.602**	0.007 **0.004**	0.650 **0.646**	1.443 **1.438**
	400	-1.547 **-1.534**	-0.666 **-0.664**	0.004 **0.004**	0.692 **0.693**	1.580 **1.581**

D. *Inverter model*

The PMSM drive model also comprises an IGBT/MOSFET/GTO inverter model. The inverter model includes conduction loss and voltage offset drop of the switches and diodes. The inverter simply models the inverter switching function without interpolation (unlike in [1][5]) because of the 10 ns resolution of the IGBT gate signal. The voltage output for each phase of the inverter can be modeled as (neglecting the voltage drops in the switches for the sake of clarity):

$$V_x = V_{dc} * \{G_{up} == 1 \,|\, (G_{up} == 0 \,\&\, G_{lo} == 0 \,\&\, I_x < 0)\} \quad (3)$$

where

V_x: Output voltage of the inverter for each phase $x=\{abc\}$
V_{dc}: DC-link voltage
G_{up}: conduction state of the upper IGBT (On-> 1, Off->0)
G_{lo}: conduction state of the lower IGBT (On-> 1, Off->0)
I_x: current output of the inverter branch. A positive current is defined as entering the load for each phase $x=\{abc\}$

When no IGBT pulses are present, the above equation is overridden by a special logic that switches the anti-parallel diodes so the inverter acts as a natural rectifier if its back-EMF is larger than half the DC-link voltage.

Switching losses are not taken into account directly by this inverter model. To include these losses into a real-time simulation, one could use a table of converter efficiency with dependency on inverter power [7]. The efficiency table would modify the power drawn by the inverter at the DC-link by modifying the total DC-link current according to the table.

The correct modeling of inverter dead time is very important for automotive applications. Dead time usually diminishes the available torque and can cause some distortions in the motor currents. Dead time is included in the proposed inverter model in the last part of Equation (3).

In the following test, we compare the effects of dead time in the FPGA simulation and compare this with a simulation made with JMAG-RT and an interpolating inverter model called TSB from Opal-RT Technologies [1][5].

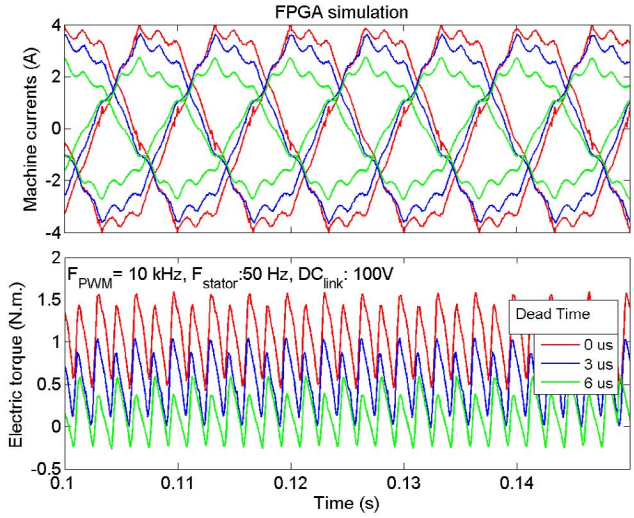

Fig.6. FPGA simulation of FEA-based drive with 10 kHz inverter and variable dead time.

For this test, the fundamental frequency of the stator voltage is 50 Hz, has a 30 degrees angle with the Back-EMF and is modulated at 10 kHz. The DC-link voltage is set at 100V and the resulting modulation index has a maximum value of 0.5.

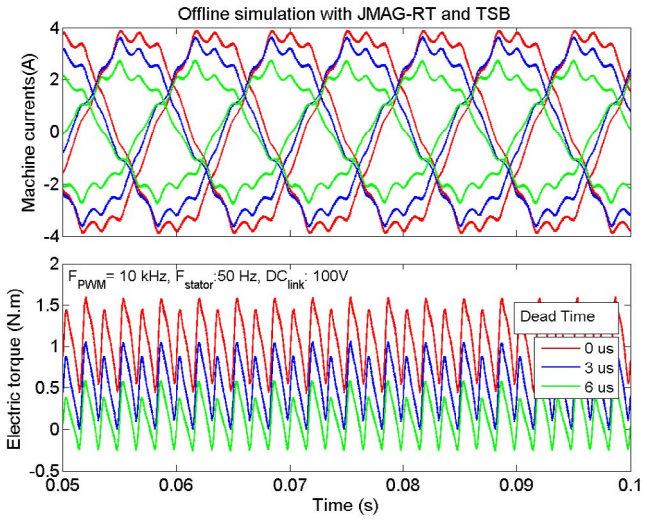

Fig.7. Offline simulation with JMAG-RT and Time-Stamped Bridge (TSB) with 10 kHz PWM and variable dead time.

The test consists of varying the dead time of the PWM waveform applied to the FEA-based PMSM drive. One can observe that the FPGA simulation (Fig.6) of the drive closely matches the simulation of the same model made offline with JMAG-RT and interpolating inverter models (Fig.7).These inverter models where proven to be accurate in real industrial applications (see [5] in particular). On both figures, one can observe that the produced electrical torque decreases with increased dead time. We stress again that the FPGA simulation is made on the FPGA card as monitored on the Console PC of the real-time simulator and is not a ModelSim-type of simulation.

E. Current profiles at Analog Outputs

A crucial aspect of the proposed motor controller tester (that is, the simulator) is the fidelity of replication of the motor current signals produced by the simulator and read by the actual controller during HIL testing. In a real motor, and in a FEA-based model, slot effects can by observed in the motor currents, as additional harmonics are present. The FEA-based FPGA model outputs the motor currents at the analog outputs of the FPGA card and we verify in this section that these signals, measured by a real oscilloscope, contain the expected current harmonics. This harmonic content is then compared to off-line simulation results.

12000 RPM case with 40 kHz PWM source

Fig.8 shows the analog output of one phase of the motor current with a scaling of 3.7 V/A. In this case, the motor drive is driven in open-loop with a 40 kHz PWM voltage having a fundamental stator frequency and rotor-related phase of 400 Hz and 30 degrees respectively. For the 4-pole PMSM used, this corresponds to a 12000-RPM rotor frequency.

Fig.9 depicts the same simulation case made at 1 us with JMAG-RT. It is interesting to notice that the current ripples are well simulated in the FEA-FPGA model despites the 40 us update rate of the inductance matrix made on the CPU.

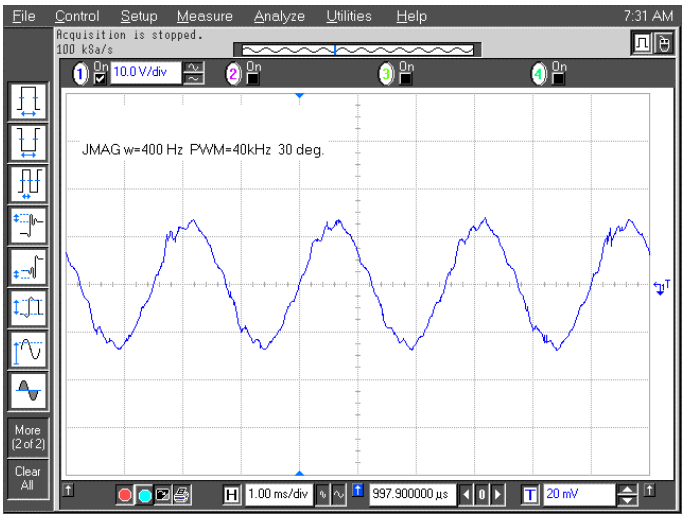

Fig.8. Motor current at the Analog Outputs (3.7V/A) for the FEA FPGA model (40 kHz PWM, 400 Hz rotor speed).

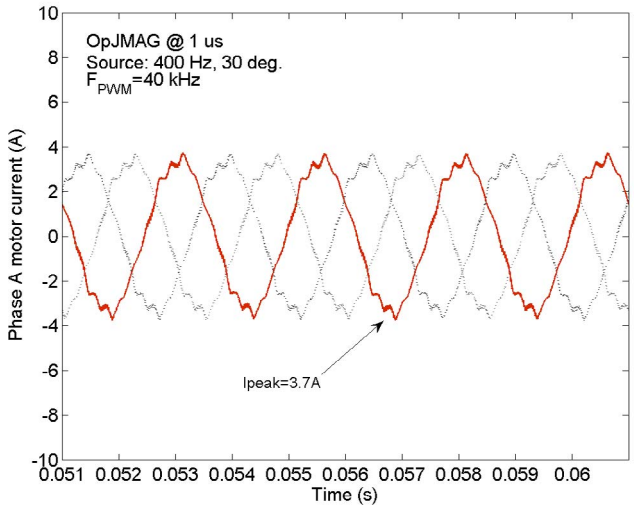

Fig.9. OpJMAG 1us reference simulation of PMSM drive (40 kHz PWM, 400 Hz rotor speed)

1500 RPM case with 20 kHz PWM source

Figure Fig.10 shows a similar analog output measurement for a fundamental 50Hz stator frequency (1500 RPM), a voltage angle of –15 degree and a PWM modulation frequency of 20 kHz. Again, a reference simulation made with JMAG-RT at 1 us shows that the currents harmonics are well represented in the FPGA simulation.

In both cases (50 Hz and 400 Hz), despite the difficulties to correlate the analog output signals of the motor current to off-line reference simulations, it must be understand that the motor current are directly used to compute the electrical torque on the

CPU of the simulator. Therefore, the current waveform is accurate because average torque is accurate itself (see Table 1).

The simulator enables the users to verify that its vector controller current/torque loops work correctly in the presence of realistic motor currents that include slot-induced harmonics.

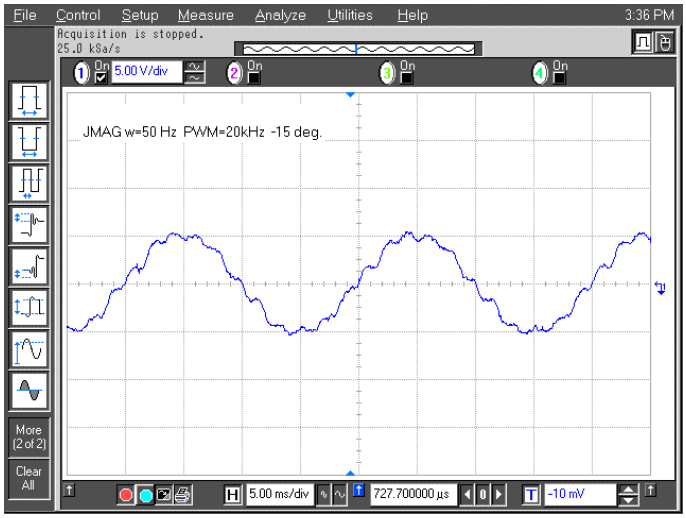

Fig.10. Motor current at the Analog Outputs (3.7V/A) for the FEA FPGA model (20 kHz PWM, 50 Hz rotor speed).

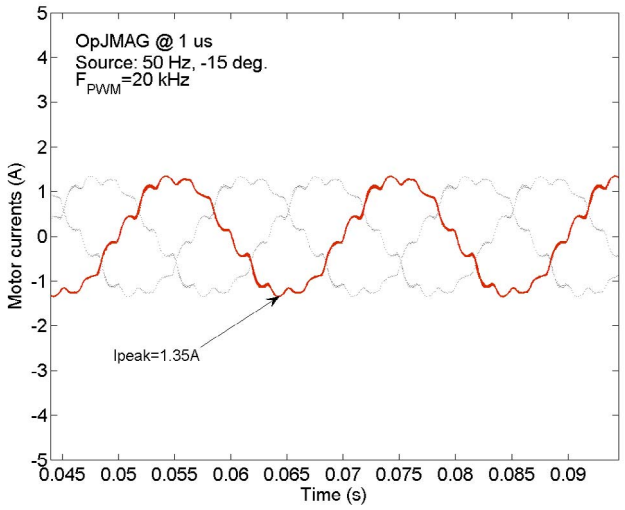

Fig.11. OpJMAG 1us reference simulation of PMSM drive (20 kHz PWM, 50 Hz rotor speed)

F. FPGA synthesis results

The Opal-RT FPGA card used in this paper is based on the Virtex II Pro XC2VP7 chip. This chip has 11088 logic cells, 44 RAM blocks and 18-bit embedded multipliers. The FEA-based PMSM drive along with resolver and quadrature encoders and a test PWM source used 4/5 of the available LUT and 1/3 of the available RAM blocks and embedded multipliers, leaving space for other models to be implemented on the FPGA card.

CONCLUSION

In this paper, we have presented a real-time simulator of a PMSM drive modeled from FEA-analysis software and executed on a FPGA card. The PMSM model is implemented by its the phase-domain equations. This phase-domain model is then feed by the PMSM back-EMF and winding inductances values which are pre-computed from the JMAG-RT FEA software, stored in tables for fast access and using interpolation methods to increase precision. In particular, the PMSM inductance inverse matrixes are computed in a CPU of the simulator running in parallel with the FPGA-executed PMSM drive model.

Validation tests have shown that the FEA-FPGA PMSM model reproduces correctly the torque of the model, that the average torque of the model is accurate across the spectrum and that the simulator adequatly reproduces the current harmonics of the motor at its analog outputs.

With the 24-slot motor used, a 12th harmonic component is present in the motor current. At 400Hz stator frequency, this results in a 4800 Hz component which is near the expected limit of fidelity of the simulator in this regards because the inductance matrix is updated at 40 us in this paper (25 kHz update rate). Work is under way to implement the inductance update methods on the FPGA itself to avoid this limitation.

As mentioned in [2], PMSM inductances $L(\theta, I_{abc})$ have a small dependency on current amplitude I_{abc}. This would greatly simplify the eventual implementation of the inductance update routine directly on the FPGA (in RAM blocks for example) and making the model insensible to CPU rate.

Finally, the proposed FPGA motor drive simulator has an input-output latency below 1.5 us and should be adequate for testing motor vector controller with sample rate down to 10 us.

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