Cheetah: A high frame rate, high resolution SWIR image camera

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ABSTRACT

A high resolution, high frame rate InGaAs based image sensor and associated camera has been developed. The sensor and the camera are capable of recording and delivering more than 1700 full 640x512pixel frames per second.
The FPA utilizes a low lag CTIA current integrator in each pixel, enabling integration times shorter than one microsecond. On-chip logics allows for four different sub windows to be read out simultaneously at even higher rates.
The spectral sensitivity of the FPA is situated in the SWIR range [0.9 – 1.7 µm] and can be further extended into the Visible and NIR range.
The Cheetah camera has max 16 GB of on-board memory to store the acquired images and transfer the data over a Gigabit Ethernet connection to the PC. The camera is also equipped with a full Cameralink™ interface to directly stream the data to a frame grabber or dedicated image processing unit. The Cheetah camera is completely under software control.

Keywords: InGaAs, SWIR, High-speed camera, Cameralink ™, hyperspectral imaging, Optical coherence Tomography, fast Thermography

INTRODUCTION

Short Wavelength Infrared or SWIR imaging and sensing applications are a very interesting extension of the visible and NIR imaging applications. In geology, bio-chemistry and meteorology a lot of interesting features, such as material composition and cloud coverage, can be easily detected and measured. Additionally the SWIR range can be used for thermographic applications of hot objects or for the detection of fast thermal events, such as break heating or interface layers temperature profiling. Finally the SWIR range is of great interest to applications requiring active illumination as high intensity (laser) illumination sources in the 1.5 µm range are eye safe.

A lot of applications in the SWIR range are high speed by nature or are requesting high speed and high throughput sensors: e.g the Focal planes or FPA's used in hyperspectral imagers, where a two-dimensional imager is used essentially as a linear array and where frame (or object line) rates in the order of several kHz are required.

At this moment InGaAs is the most mature and widespread material for imaging in the [0.9 – 1.7 µm] band; the material can be grown lattice matched on InP substrates with high throughput MOCVD machines. It is the same material, which with some minor process variations is used in most of nowadays optical communication applications. For this reasons it is the natural choice for SWIR application or after removal of the substrate for broadband applications in the [0.6 – 1.7 µm] or even [0.4 – 1.7 µm] range. With this cutoff wavelength it is possible to use the InGaAs detectors uncooled for most high speed applications; cooling of the detectors is only required for medium to low light level applications, requiring integration times longer than a few msec at an operating temperature > 50 ^{o}C.

DETECTOR INTERFACING

A narrow bandgap material detector needs always to be interfaced to a Silicon ReadOut Integrated Circuit or ROIC, as the material properties and the present status of the technology do not allow for complex interfacing in the InP or InGaAs material.

Generally three different basic detector interfacing circuits are used to collect and readout the photocurrent, generated in an infrared detector (see Figure 1)

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- A Source Follower per Detector or SFD circuit, where the detector current is integrated on the photodiode itself,
- A Direct injection stage or DI, where the bias over the detector is kept low and constant independent of the integration capacitor voltage swing
- A Charge sensitive TransImpedance Amplifier or CTIA, where the bias over the detector is kept constant by and active amplifier and where the photocurrent is accumulated on the feedback capacitor.

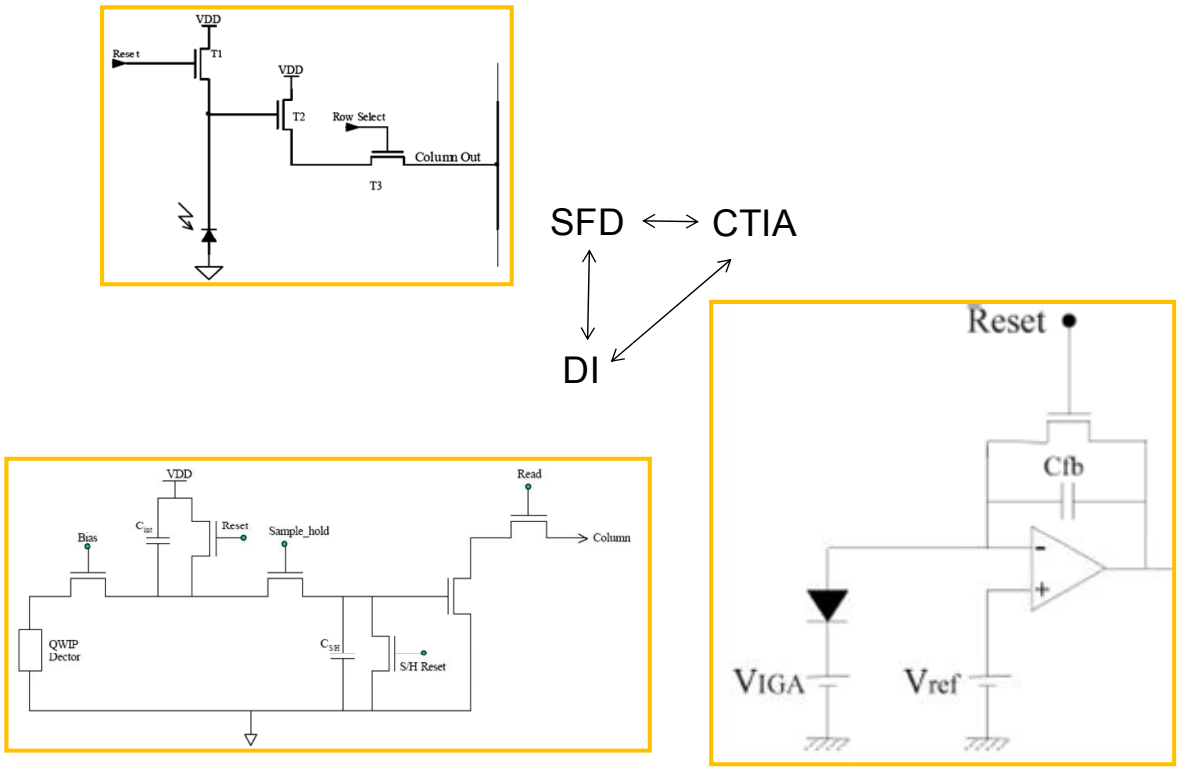

Figure 1: Schematic representation of the 3 commonly used interfaces for IR detectors:
SFD: Source follower per detector, Charges are accumulated on detector capacitance
DI: Direct Injection stage, detector is kept at constant bias
CTIA: Charge sensitive TransImpedance Amplifier

Although being of great simplicity and often used in visible CMOS imagers, the SFD solution is not very attractive in IR applications, as due to the high reverse bias, the dark current is high – certainly at high operating temperatures; additionally the sensitivity of the SFD structure is low due to the high intrinsic detector capacitance in the InGaAs.[1,2,3]

The DI structure is also a very simple and power lean interface, which works very well in thermal infrared applications with a high DC signal pedestal and low contrast ratio. The SWIR InGaAs detectors are facing a near zero DC signal and a very high contrast ratio of the signal. In the darker parts or under very low light level conditions the DI stage suffers from a considerable image lag as, can be derived from the injection efficiency formula (1):[4,5]

$$\eta_{inj} = \frac{G_m.R_{\det}}{1+G_m.R_{\det}} * \frac{1}{1+\frac{j\omega C_{Det}.R_{\det}}{1+G_m.R_{\det}}} \qquad (1)$$

As a result the only low dark current, low lag and broad application interface circuit for SWIR detectors is the CTIA interface stage; the most important drawback is its transistor count and the higher unit cell power dissipation.[6,7,8] The last argument can be easily overcome by making the power dissipation in the interface stage variable and controlled by an on-board DAC. For high sensitivity applications, where a small integration capacitor is required the transistor count

is also not really an issue. In any case the CTIA interface yields a linear, low lag interface for SWIR detectors, capable of spanning an integration time range from 100 nsec up to 1 sec or longer, depending on the cooling of the detector. For high speed applications the short integration times are most important and can be obtained by sinking a DC current of max. 200 nA per cell or an overall matrix power dissipation of 220 mW.

ROIC ORGANISATION AND TIMING CONSTRAINTS

The analog chain of the ROIC is sketched in Figure 2. The ROIC is designed to operate with a synchronous shutter: all pixels are reset simultaneously and the image information is sampled at the same moment on an in-pixel Sample&Hold capacitor.

Then the sampled information is transferred row by row to column registers located at the bottom and the top side of the matrix in an odd-even arrangement. As for the minimum Window Of Interest or WOI, the line readout time is only 13 Clock cycles of 25 nsec long, it is necessary to make a pre-sampling of the row information, before the information is shifted onto the internal output bus.

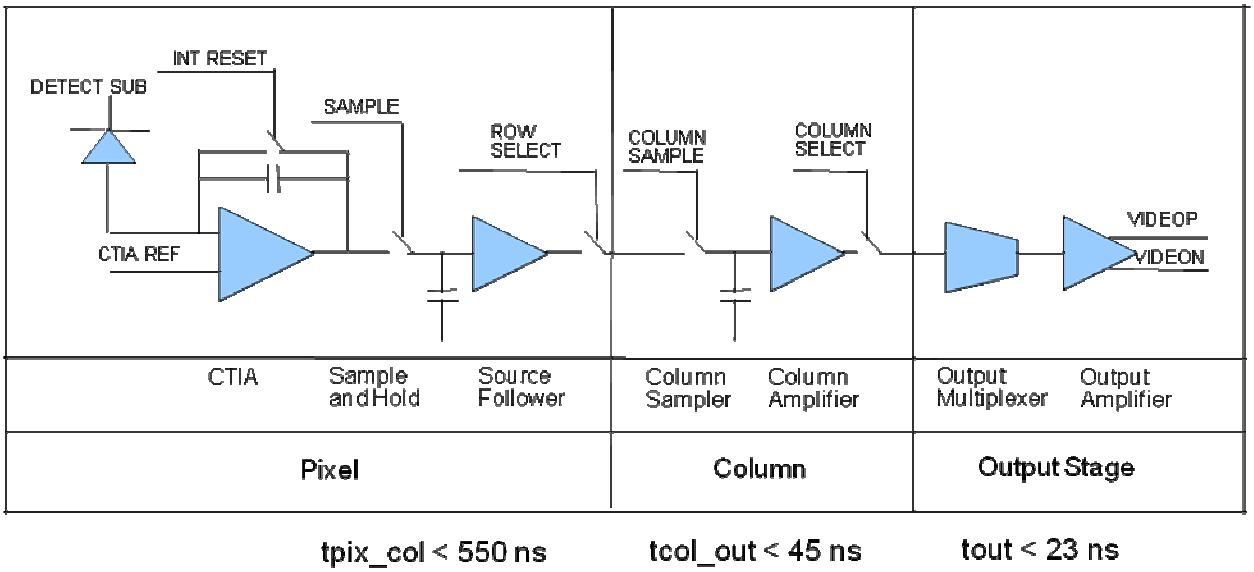

Figure 2: Analog signal chain for the high speed ROIC, The times, given at the bottom of the figure, indicate the time constants for each charging/discharging operation.

Due to the high serial readout rate and to keep the power dissipation within limits the information is put in two steps onto the output bus: firstly the internal node of the column buffer is charged and in the next cycle the pre-charged node is put onto the output bus. In this way it is possible to realize a 0.1 % settling between the dark and light value within 20 nsec.

Finally the output buffer is capable of driving a < 600 Ω complex impedance. The ROIC/FPA can be operated either in 16 or in slow speed 4 output mode. With 16 outputs some 1720 full frames can be recorded per second; in 4 output mode the frame rate is reduced with app. a factor of 4.

Besides of the full frame readout the ROIC can read up to 4 WOI's on one integrated image. Each window can be placed independent of the others in the full Field of View of the FPA; it is even possible to partially overlap the windows. The 4 WOI's are of special interest when working in hyperspectral applications, where only a limited amount of spectral bands needs to be transferred and which allows to push the frame rate to even higher values. A minimum full width WOI of 4 rows can be read and treated in 5 µsec, resulting in a WOI frame rate of 200 kHz.

Like most nowadays CMOS imagers and ROICs the circuit can be read left to right or right to left and top to bottom or bottom to top. Finally the circuit allows to control the power dissipation and hence the bandwidth of all elements in the analog chain. Most power controls are done with a 3 or 4 bit DAC. All the above settings are controlled via a SPI interface which is operated via a 4 wire interface: data in, data out, clock and select.

FPA MANUFACTURING AND PACKAGING

The $In_{0.53}Ga_{0.47}As$ layer is grown lattice matched on 3" InP substrates. The photodiodes are formed by a Zn diffusion in a planar process. After the diffusion layer a passivation layer is deposited, contact holes are defined and the metal contacts are deposited. At the end of the process the backside of the wafers is lapped and an antireflective coating is applied. [9]

A 640*512 InGaAs array is flip-chipped with In bumps on top of the ROIC circuit. The photodiode array is surrounded by 9 columns and rows of substrate contacts.

After flip-chipping the FPA is mounted on a thick film substrate, together with some bias voltage buffering capacitors and current mirror control resistors. This assembly is then mounted in a Covar butterfly package with 64 leads. The large number of leads is mainly caused by the 32 leads required for the 16 differential outputs. It is possible to introduce a TE-cooler in the package in order to reduce the detector operating temperature with some 20 ^{o}C.

CAMERA ORGANISATION

The packaged device is mounted on a heat sink, which is cooled by venting holes and ventilators in the front of the camera. The sensor is first mounted on a sensor board, which contains the necessary bias conditioning circuits and buffer amplifiers for the ROIC output stages.

The second Board then contains the analog power supplies for the sensor board. The Analog to digital converters, associated memory and controlling FPGA are mounted on a half height board. Each board services 4 analog outputs of the ROIC, the boards incorporate one 4 channel 14 bit ADCs with a 65 MHz conversion rate per channel, which output is connected to the DDR2 bank, which can contain up to 4 GB of memory.

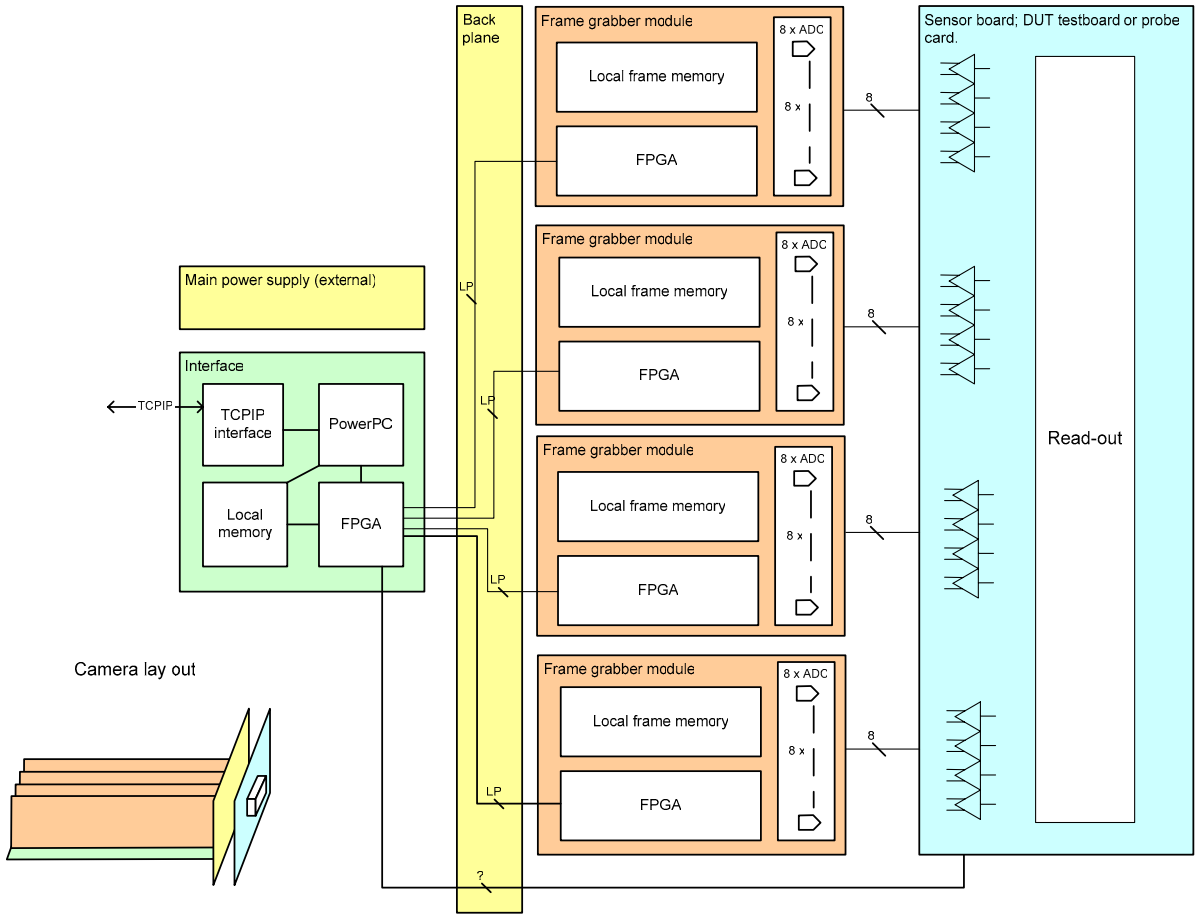

Figure 3: Schematic block diagram of the Cheetah camera.

The camera is controlled by multiprocessor board with a PowerPC™ and Virtex-4 FPGA. The PowerPC controls the Gig-E communication channel for the commanding of the camera and the transfer of the data, contained in the frame grabber memories. The acquired image data are transferred via the FPGA from the frame grabber boards. The FPGA is also responsible for the driving of the ROIC, the sending of commands to the ROIC via the SPI bus and for the configuration of the camera.

The camera can operate as well in pre-view mode as in burst recording mode. It is also possible to read out the image data directly without buffering over an auxiliary full Cameralink™ channel.

The camera is also equipped with a SMA connector for triggering purposes; multiple trigger schemes can be programmed in the firmware of the camera.

FPA AND CAMERA PERFORMANCE

The main characteristic of the FPA are summarized in the below table.

Table 1: Summary data of the 640*512 FPA

Parameter	Target Value	Measured results	Unit
Technology	0.35 µm CMOS		
Vdd	3.3		V
Current 16 output mode	350		mA
Current 4 output mode	190		mA
Clock Frequency	40		MHz
Total output rate	640		MHz
Full frame rate 16 output	1740		Hz
Full frame rate 4 lines	200 000		Hz
Output range	2	1.8	V dif.
Common mode voltage	1.5	1.2 – 1.6	V
Sensitivity High Gain	25.0	22.8	µV/e-
Sensitivity Low gain	1.9	1.8	µV/e-
Saturation charge HG	80 000	75 000	e-
Saturation charge LG	1 000 000	960 000	e-
Linearity	< 2	1.78 (LG) / 1.93 (HG)	% FS
Dark Current	3 500 000	2 800 000	e-/sec
Noise High Gain	110	192	e-
Noise Low gain	530	600	e-
FPN @ short Tint	< 5	2.3 (LG) / 2.9 (HG)	% FS

All results are in good correspondence with the design values. The full well capacity is somewhat lower than expected, but this is mainly caused by the accommodation of the overall output signal, including the Fixed Pattern Noise, within the digitalization window of the ADC.

The only more or less serious deviation is coming from the noise performance. Both for low and high gain an excess noise of app. 170 to 220 e^-_{rms} is measured. Part of this excess noise (app. 100 e^-) can be attributed to charge partitioning noise in the reset transistor of the CTIA stage; another part is most probably still coming from (differential) noise on the detector and CTIA virtual ground line.

Table 2: Main properties of the Cheetah camera.

Parameter	Target	Unit
Control and data	Gig-E	
Additional data channel	Cameralink ™	
Power supply	12	V
Current Inl. cooling	5	A
TEC cooling	➢ 270	K
Internal Memory	Max. 16	GByte
Recording time	15	sec

A full picture of the camera is given in Figure 4.

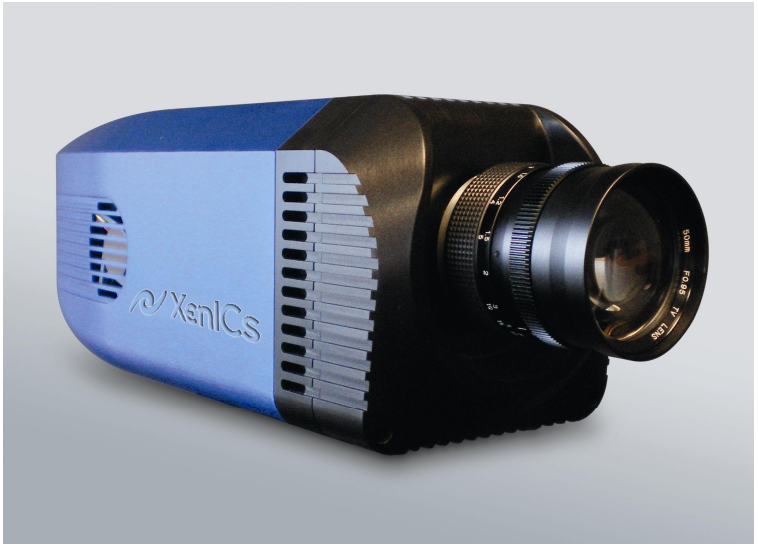

Figure 4: Photograph of fully assembled Cheetah camera. Ventilation holes in the front are for detector cooling, holes in the back are for electronics, mainly interface card cooling.

CONCLUSIONS

XenICs has successfully concluded the development of a high speed, full VGA format InGaAs camera with a frame rate as high as 1740 frames/sec and 200 000 frames of 4 lines/sec. The power consumption, linearity and sensitivity are in line with the design values. The noise of the camera is 200 and 600 e^-_{rms} for high gain and low gain, respectively, which corresponds with an excess noise of 200 e^-_{rms}. This issue needs to be further investigated; some amelioration can be expected from a more careful camera layout, whereas another part shall come from the revision of the pixel clocking.

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