Below-IC Post-CMOS Integration of Thick MEMS on a Thin-SOI Platform Using Embedded Interconnects

Vijay Rajaraman¹, Jan-Jaap Koning²,⁴, Eric Ooms³, Gregory Pandraud¹, Kofi Makinwa¹, Henk Boezen²

¹ Delft University of Technology, The Netherlands; ² Eindhoven University of Technology, The Netherlands; ³ NXP Semiconductors NV, Nijmegen, The Netherlands; ⁴ NovioMEMS BV, Nijmegen, The Netherlands

Introduction.

- A novel below-IC MEMS technological approach for post-CMOS integration of thick and high aspect ratio (HAR) SOI-MEMS in a thin-SOI BCDMOS (Bipolar-CMOS-DMOS) platform, on the backside in the SOI handle wafer, is presented.

- Key enablers of this post-CMOS MEMS integration technique are – the formation of low resistance (~ 40 \(\Omega\)) embedded polysilicon interconnects and the formation of small leakage and large resistance (> 10¹² \(\Omega\)) oxide-lined isolation trenches during standard CMOS processing, and the use of Deep Reactive Ion Etching (DRIE) process for post-CMOS backside micromachining of HAR MEMS.

Integration Approach

![Integration Approach Diagram](image)

Results

![Results Diagram](image)

Conclusions

- Post-CMOS below-IC thick, HAR MEMS integration in a thin-SOI BCDMOS platform using polysilicon interconnect was demonstrated. Measurements show that placing the MEMS adjacent-beneath the integrated thin-SOI devices, 30 \(\mu\)m away from the device region, does not affect their electrical characteristics – design rule!