Crosstalk-Induced Delay, Noise, and Interconnect Planarization Implications of Fill Metal in Nanoscale Process Technology

Arthur Nieuwoudt, Member, IEEE, Jamil Kawa, Member, IEEE, and Yehia Massoud, Member, IEEE

Abstract—In this paper, we investigate the crosstalk-induced delay, noise, and chemical mechanical polishing (CMP)-induced thickness-variation implications of dummy fill generated using rule-based wire track fill techniques and CMP-aware model-based methods for designs implemented in 65 nm process technology. The results indicate that fill generated using rule-based and CMP-aware model-based methods can have a significant impact on parasitic capacitance, interconnect planarization, and individual path delay variation. Crosstalk-induced delay and noise are significantly reduced in the grounded-fill cases, and designs with floating fill also experience a reduction in average crosstalk-induced delay and noise, which is in contrast to the predictions of previous studies on small-scale interconnect structures. When crosstalk effects are included in the analysis, the observed delay behavior is significantly different from the delay modeled without considering crosstalk effects. Consequently, crosstalk-induced delay and noise must be simultaneously considered in addition to parasitic capacitance and interconnect planarization when developing future fill generation methods.

Index Terms—Chemical mechanical polishing, crosstalk-induced delay, design for manufacturability, dummy fill, noise.

I. INTRODUCTION

TODAY, the decreasing feature sizes and tighter manufacturing tolerances associated with nanoscale process technology, design for manufacturability (DFM) has become an increasingly critical aspect of the physical design process [1]–[3]. In current and future process technologies where the utilization of subwavelength lithography places tighter constraints on the depth of focus [4], the control of the metal and interlayer dielectric (ILD) thickness variations associated with the electroplating and chemical mechanical polishing (CMP) processes during copper interconnect fabrication is crucial for realizing integrated circuits that meet performance, reliability, and yield requirements. Fill metal (dummy fill) placement is rapidly becoming an important component of the DFM toolbox for the minimization of manufacturing variations due to CMP [5]. However, as the number of metal layers increases and interconnect dimensions decrease, the parasitic capacitance increases associated with fill metal have become more significant, which can lead to timing and signal integrity problems.

Previous research has primarily focused on two important aspects of fill metal realization: 1) the development of fill metal generation methods [6]–[14], which we discuss further in Section II and 2) the modeling and analysis of capacitance increases due to fill metal [15]–[22]. Several studies have examined the parasitic capacitance associated with fill metal for small-scale interconnect test structures in order to provide general guidelines on fill metal geometry selection and placement [15]–[18], [22]. For large-scale designs, [20] and [21] report incremental capacitive increases of 7% and 32% due to floating-fill metal in 180 and 130 nm technology, respectively. Despite previous research efforts on quantifying the incremental capacitance increases associated with dummy fill, the crosstalk-induced timing and noise impact of fill metal has not been extensively examined for large-scale designs in sub-90 nm process technologies where both parasitic capacitance and interconnect planarization are vital concerns.

In this paper, we investigate the crosstalk-induced delay, noise, and CMP-induced thickness-variation implications of dummy fill generated using rule-based wire track fill techniques and CMP-aware model-based methods for designs implemented in 65 nm process technology. We first examine the impact of fill metal on several interconnect test structures, which provides important insights into the performance and reliability implications of both intralayer and interlayer capacitive coupling due to dummy fill and their effect on crosstalk-induced delay and noise. We then explore the crosstalk-induced timing, noise, capacitance, and CMP-induced thickness-variation implications of fill metal on several large-scale designs implemented in 65 nm process technology.

The results indicate that dummy fill generated using rule-based and CMP-aware model-based methods can have a significant impact on parasitic capacitance, interconnect planarization, and individual path delay variation. Crosstalk-induced delay and noise are significantly reduced in the grounded-fill cases, and designs with floating fill also experience a reduction in average crosstalk-induced delay and noise, which is in contrast to the predictions of previous studies on small-scale interconnect structures. When crosstalk effects are included in the analysis, the observed delay behavior is significantly different from the delay modeled without considering crosstalk effects. This work provides the first simultaneous


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Digital Object Identifier 10.1109/TVLSI.2008.2010830
investigation of the crosstalk-induced timing, noise, wire capacitance, and interconnect planarization implications of dummy fill metal for large-scale designs implemented in nanoscale process technology.

The rest of this paper is organized in the following manner. Section II discusses the fundamental concepts in interconnect planarization, fill metal placement, interconnect delay, and crosstalk noise. Section III describes the interconnect planarization, capacitance, delay, and crosstalk effects associated with different dummy fill generation methods for three large-scale designs implemented in 65 nm technology. Section VI concludes the paper.

II. BACKGROUND

A. Interconnect Planarization and Fill Placement

Several important factors are driving the need for interconnect planarization in nanoscale process technologies. First, variations in metal and ILD thickness caused by the electroplating and CMP processes are cumulative in higher metal layers and can cause connectivity issues in both vias and horizontal wires. Furthermore, metal and ILD thickness variations produce changes in interconnect resistance and capacitance, which can result in unanticipated timing and signal integrity problems [23], [24]. Finally, the utilization of subwavelength lithography in 65 nm and smaller process technologies places tighter constraints on the depth of focus [4], which metal or ILD surface variations exacerbate. With typical depth of focus budgets in the tens of nanometers in current process technologies, metal and ILD surface variations can lead to a total lack of feature printability [23].

Since the realized metal and ILD thickness in a particular region is a function of the interconnect geometry and metal density, fill metal is inserted to provide a more uniform post-CMP surface that results in improved interconnect planarization. Traditional rule-based dummy fill generation techniques place fill metal in a regular pattern to meet a certain foundry-specified metal density in a particular region [15]. Fig. 1(a) displays a typical example of rule-based fill placement where the fill metal is placed in the wire routing tracks. While rule-based methods have demonstrated that a modeling framework for fill metal that can consider capacitance, ground capacitance, interconnect delay, and crosstalk noise. Section V describes the interconnect planarization, capacitance, delay, and crosstalk effects associated with different dummy fill generation methods for three large-scale designs implemented in 65 nm technology. Section VI concludes the paper.

![Fig. 1. Typical example of fill placement for (a) rule-based and (b) model-based fill generation techniques.](Image)
can potentially increase the coupling capacitance between adjacent nets. However, grounded fill typically causes greater incremental capacitance increases than floating fill, and the placement of vias for connecting the fill metal to the power grid can be problematic [15].

B. Interconnect Delay and Crosstalk Noise

As process technology continues to scale, larger wire aspect ratios have increased the coupling capacitance ($C_c$) between two wires compared to the ground capacitance ($C_g$) between a particular wire and the substrate. This leads to larger crosstalk-induced noise and delay increases, which can cause signal integrity and timing problems. To provide insight into the contributions of $C_c$ and $C_g$ to wire delay, consider a first-order Elmore delay model [26],

$$D = 0.7R_d(C_d + C_g + S_f C_c) + R_l(0.7C_l + 0.4C_g + 0.4S_f C_c)$$

(1)

where $C_l$ is the load capacitance, $R_l$ is the resistance of the signal wire, $S_f$ is the switching factor associated with the interconnect, and $R_d$ and $C_d$ are the driver resistance and capacitance. In a standard timing analysis, $S_f = 1$. Therefore, $C_d$ and $C_c$ have the same effect on delay since the adjacent signal wire connected to $C_c$ is assumed to be grounded. However, when crosstalk-induced delay is considered, $S_f \approx 2$ or greater is typically assumed to account for the impact of the simultaneous switching of adjacent interconnect lines [26], [27]. Therefore, $C_c$ has a greater incremental impact on timing than $C_g$ when crosstalk effects are taken into account.

$C_c$ can also generate noise on quiet signal lines. A simplified model for the noise voltage due to capacitive crosstalk on quiet victim wire near a switching aggressor line is [28]

$$V(t) = \left(\frac{C_c}{C_c + C_d + C_g}\right) V_{DD} e^{-t/\tau}$$

(2)

where $\tau = R_d(C_c + C_d + C_g)$. Based on (2), the ratio between $C_c$ and $C_g$ determines the height of the noise generated on the victim line. Therefore, as $C_c$ increases, the magnitude of the crosstalk-induced noise decreases. Conversely, as $C_g$ increases, the magnitude of the crosstalk-induced noise increases. Therefore, both the size of $C_c$ and the ratio between $C_c$ and $C_g$ have important implications for crosstalk noise.

Given the importance of $C_c$ and $C_g$ for both delay and crosstalk noise, understanding the effect of grounded and floating-fill metal on capacitance is crucial. Fig. 2 illustrates the first-order impact of floating and grounded-fill metal on capacitance based on a parallel plate model. When no fill metal is present, the capacitance is inversely proportional to the distance between the two wires. When grounded-fill metal is inserted between the two signal lines, the fill metal shields the coupling capacitance but increases the effective ground capacitance. For floating fill, the coupling capacitance is the series combination of the capacitance between the two signal lines and the fill metal [15].

While the simplified models in (1) and (2) provide important insights into the relationship between delay, crosstalk noise, and the underlying coupling and ground capacitances values, they do not provide the flexibility and accuracy to capture crosstalk effects in the complex IC environment, where any given signal line may be impacted by multiple aggressor lines switching at different times during a particular timing window [29]. Therefore, in this paper, we employ commercial timing analysis, noise analysis, and RC extraction tools for the subsequent investigation of the delay and noise impact of fill metal as discussed in Section III.

III. DESIGN EXAMPLES AND SIMULATION ENVIRONMENT

To investigate the crosstalk-induced timing, noise, capacitance, and CMP-induced thickness-variation implications of dummy fill, we examine both small-scale interconnect test structures and large-scale designs implemented in a standard 65 nm process technology. We first examine the impact of fill metal on several interconnect test structures, which provide important insights into the implications of capacitive coupling due to dummy fill and their effect on crosstalk-induced delay and noise. We then explore the interconnect planarization, capacitance, delay, and noise implications of fill on several large-scale designs. For each large-scale design example, we examine cases with both floating and grounded fill generated using three different fill generation methods.

To generate rule-based fill for the small-scale interconnect test cases and for the large-scale design examples, we utilize the automated wire track fill feature in Astro [30]. We employ minimum width rectangular fill shapes in each wire track that are oriented parallel to the signal wires. This effectively balances the parasitic capacitance and the number of fill shapes [17], [18], [21]. We generate the CMP-aware model-based fill using the method and design tool presented in [11]. The method employs a model-based layout pattern-dependent algorithm to reduce the thickness range of the topography associated with each metal layer. The algorithm leverages the electroplating and CMP models presented in [24] and [11], respectively, which are calibrated to 65 nm process technology. Note that we also utilize the electroplating and CMP models presented in [24] and [11] to evaluate the realized metal and ILD thickness and its variation for each metal layer. The CMP-aware model-based fill generation algorithm and its implementation are described in further detail in [11].

For timing and noise analysis in both the small-scale interconnect test cases and the large-scale design examples, we utilize PrimeTime SI [31]. To determine the electrical characteristics associated with interconnect in each of the small-scale and large-scale design examples, we initially perform RC extraction...
utilizing the full-chip extraction tool, Star-RCXT [32]. Once we identify the important nets in the design using the results from the initial extraction process and timing/noise analysis tools, we simulate the capacitance of the important nets utilizing the field solver Raphael NXT [33]. Note that we set that capacitance accuracy level in the field solver to 1% to balance CPU runtime and accuracy. In the small-scale interconnect test cases, the important nets with capacitance extracted using the field solver include all of the signal nets in the examples. In the large-scale design examples, the important nets with capacitance extracted using the field solver include the top 60 critical delay paths in the cases both without and with crosstalk effects as well as the top 100 nets with the most noise. Therefore, all of the capacitance, timing, and noise results reported in Sections IV and V, with the exception of data listed in Table III, are based on the interconnect capacitance values obtained from the field solver Raphael NXT. The full-design capacitance data listed in Table III are generated based on a combination of results from Star-RCXT and Raphael NXT.

IV. IMPACT OF FILL METAL ON SMALL-SCALE INTERCONNECT TEST STRUCTURES

A. Test Cases

We simulated three small-scale interconnect test structures implemented in a standard 65 nm process technology, which are depicted in Fig. 3. In each test case, the interconnect lines have a 65 nm width and are approximately 100 μm long. The wires are connected to both driver and load buffers. In test case 1, the two signal lines are implemented on M3 with a 65 nm wire spacing while the signal lines in test case 2 are separated by one wire track (195 nm separation). Test case 3 has four total signal lines with a 65 nm intra-layer wire spacing for the two signal lines implemented on both M3 and M5. The wires are placed over a silicon substrate. Test cases 1 and 2 demonstrate the impact of intralayer capacitive coupling, while test case 3 illustrates the interplay between interlayer and intralayer capacitive coupling. Note that the wire width and spacing utilized in the small-scale test cases are typical of the interconnect configurations in the intermediate routing layers of the large-scale designs discussed in Section V.

For each test case, we generate several different floating and grounded-fill subcases, which are displayed in Fig. 3 and also listed in Table I. Note that 1X and 2X listed under the fill type in the table refer to the buffer spacing utilized in the test cases. The buffer spacing is defined as the minimum spacing between the generated fill metal and any given signal line on a particular metal layer. In test case 1, subcases B/E demonstrate the impact of floating and grounded intralayer fill while subcases C/D/F/G illustrate the effect of floating and grounded interlayer fill both above and below the signal lines. Test cases 2 and 3 have a similar set of subcases with both intralayer and interlayer fill. Note that the rule-based fill generated in this section is similar to the maximally intersecting interlayer fill cases discussed in [22].

B. Results

Table I displays the capacitance, delay, and noise results for the small-scale interconnect test cases. In test case 1, adding intralayer floating fill only (subcase B) does not substantially impact the capacitance. However, when floating fill is added to the layer above the signal lines (subcase C), the additional metal not only increases the coupling capacitance between the signal lines but also causes an increase in the ground capacitance since the signal lines are more effectively coupled to the intralayer floating-fill lines, which have a relatively large area exposed to the substrate as depicted in Fig. 4. When floating fill is added to the layer below the signal lines (subcase D), the ground capacitance substantially increases since the signal lines are more effectively coupled to the floating fill between the interconnect and the ground plane. For the subcases with grounded fill in test case 1 (subcases E-G), the fill metal decreases the coupling capacitance and increases the ground capacitance as illustrated in Fig. 2.

In test case 1, the incremental increase in delay without crosstalk effects closely tracks the incremental increase in total capacitance \( C_g + C_e \), which is the trend predicted...
by (1). When crosstalk effects are considered, the delay and noise depends on both $C_z$ and the ratio between $C_z$ and $C_y$, as discussed in Section II-B. The delay and noise generated due to crosstalk effects are greater in the floating-fill cases than they are in the grounded-fill cases since the grounded fill suppresses the coupling capacitance more effectively. In the interlayer floating-fill cases, the crosstalk-induced delay and noise may be larger or smaller than they are in the case with no fill metal due to changes in the ratio between $C_z$ and $C_y$. Since the noise-induced delay contribution is smaller in the grounded-fill cases, the total delay including crosstalk effects is smaller in subcase F (grounded fill) compared to the total delay in subcase D (floating fill), which have the same fill metal geometry.

The trends associated with capacitance, delay, and crosstalk effects in test case 2 are similar to those in test case 1. In the cases with only intralayer floating fill, the fill between the signal lines (subcases B and C) causes an increase in coupling capacitance due to the effect illustrated in Fig. 2. Increasing the buffer spacing to 2x causes a decrease in capacitance, which leads to smaller delay and noise compared to the cases with 1x buffer spacing. Overall, test case 1 has larger crosstalk-induced noise and delay values as well as larger total delays than test case 2 since the total capacitance is larger in test case 1 due to the closer physical proximity of the wires. Therefore, many of the nets with the greatest crosstalk-induced noise and delay in the large-scale design examples described in Section V will resemble the wire configuration in test case 1.

Since test case 1 approximates the behavior of the nets with large crosstalk-induced noise and delay values, we simulated an interlayer version of test case 1 in test case 3. The general trend for the different floating and grounded-fill subcases in test case 3 is similar to the aforementioned trends in test case 1. In the multilayer floating-fill cases, capacitive coupling to ground via the mechanism described in Fig. 4 is significantly larger (subcases

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### TABLE I

RESULTS FOR THE SMALL-SCALE INTERCONNECT TEST CASES

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Sub-Case</th>
<th>Fill Type</th>
<th>Fill Layers</th>
<th>Ground Cap. M3 (fF)</th>
<th>Ground Cap. M5 (fF)</th>
<th>Intra-Layer Coupling Cap. (fF)</th>
<th>Inter-Layer Coupling Cap. (fF)</th>
<th>Total Cap. (fF)</th>
<th>Delay Without Crosstalk Effects (ns)</th>
<th>Crosstalk Induced Delay (ns)</th>
<th>Total Delay with Crosstalk (ns)</th>
<th>Noise Area (V·ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Case 1</td>
<td>A</td>
<td>No Fill</td>
<td>N/A</td>
<td>3.49</td>
<td>8.80</td>
<td>12.29</td>
<td>0.265</td>
<td>0.123</td>
<td>0.388</td>
<td>0.118</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>Floating (1x)</td>
<td>M3</td>
<td>3.42</td>
<td>8.76</td>
<td>12.18</td>
<td>0.266</td>
<td>0.123</td>
<td>0.388</td>
<td>0.117</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>Floating (1x)</td>
<td>M3/M4</td>
<td>3.82</td>
<td>9.35</td>
<td>13.17</td>
<td>0.274</td>
<td>0.130</td>
<td>0.404</td>
<td>0.125</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>D</td>
<td>Floating (1x)</td>
<td>M2-M4</td>
<td>6.10</td>
<td>8.63</td>
<td>N/A</td>
<td>14.73</td>
<td>0.291</td>
<td>0.106</td>
<td>0.397</td>
<td>0.111</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E</td>
<td>Grounded (1x)</td>
<td>M3</td>
<td>10.26</td>
<td>7.60</td>
<td>17.86</td>
<td>0.317</td>
<td>0.084</td>
<td>0.400</td>
<td>0.089</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>F</td>
<td>Grounded (1x)</td>
<td>M3/M4</td>
<td>11.83</td>
<td>6.92</td>
<td>18.79</td>
<td>0.324</td>
<td>0.072</td>
<td>0.396</td>
<td>0.081</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>G</td>
<td>Grounded (1x)</td>
<td>M2-M4</td>
<td>13.28</td>
<td>6.80</td>
<td>19.68</td>
<td>0.331</td>
<td>0.067</td>
<td>0.398</td>
<td>0.080</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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![Fig. 4. Multilayer floating fill can increase both coupling and ground capacitance.](image-url)
TABLE II

<table>
<thead>
<tr>
<th>Design Example</th>
<th>Size (µm)</th>
<th>Standard Cells</th>
<th>Nets</th>
<th>Wires</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design A</td>
<td>248x248</td>
<td>6720</td>
<td>8074</td>
<td>98873</td>
</tr>
<tr>
<td>Design B</td>
<td>475x475</td>
<td>48199</td>
<td>48437</td>
<td>608571</td>
</tr>
<tr>
<td>Design C</td>
<td>1114x1114</td>
<td>149482</td>
<td>163227</td>
<td>1717943</td>
</tr>
</tbody>
</table>

C—E) than it is in the case, where the floating fill only exists on the layer between the two sets of signal lines (subcase B). The grounded fill suppresses the coupling capacitance between the nets, which substantially increases the delay without crosstalk but reduces the impact of crosstalk-induced noise and delay. Interestingly, the total delay associated with the grounded-fill metal is lower than the total delay of the cases with floating fill and no fill due to the smaller crosstalk-induced delay contribution in the grounded-fill cases. While these results must be conservatively interpreted since crosstalk-aware static timing analysis can produce pessimistic results [29], they imply that the delay implications of grounded-fill metal may not be as large as previously predicted.

V. IMPACT OF FILL METAL ON LARGE-SCALE DESIGNS

A. Design Examples and Experimental Setup

To investigate the interconnect planarization, capacitance, and crosstalk-induced delay and noise impact of dummy fill, we leverage the large-scale design examples listed in Table II. The design examples are implemented in 65 nm process technology and range from a moderate-sized block to a small chip-level design. We model the capacitance, timing, and noise in each design using the simulation environment described in Section III.

We insert dummy fill using three different fill generation methods: 1) rule-based with the maximum possible metal density; 2) rule-based with the minimum allowed metal density; and 3) the model-based fill metal generation methodology presented in [11]. The methods are discussed further in Sections II-A and III. For each fill placement method, we generate cases that have buffer spacing values of one, two, three, and ten times the minimum wire spacing. We consider both floating and grounded-fill metal. The metal densities averaged over the routing layers for the design examples with each fill generation technique and buffer spacing are listed in Fig. 5. Note that in the 10x buffer spacing cases, there may not be enough legal fill metal regions available to satisfy the minimum density requirement. The fill metal is placed to satisfy the foundry’s minimum and maximum metal density rules in a given region if the buffer spacing constraints can be met. The metal density plays an important role in determining capacitance and interconnect planarization.

B. Fill Impact on Wire Capacitance

Table III lists the incremental increases in average wire capacitance ($\Delta C$) for all of the wires in the design due to dummy fill inserted using rule- and model-based methods modeled with CMP-induced wire and ILD thickness variations. For each of the fill cases in a particular design, we normalize $\Delta C$ by dividing the average capacitance value of all of the nets in the design by the average capacitance value of all of the nets in the given design without fill. For the maximum metal density rule-based method with 1x buffer spacing, $\Delta C$ can be as large as 53% and 31% for grounded and floating fill, respectively. For both grounded minimum density rule- and grounded model-based fill generation methods with 1x buffer spacing, $\Delta C$ drops to values between 9% and 21% due to the lower metal density.

For the floating-fill cases with 1x buffer spacing, $\Delta C$ ranges from 7% to 12% when fill metal is inserted using the minimum density rule-based method while $\Delta C$ is less than 6% for the model-based method for the three design examples. The substantial difference in $\Delta C$ between the minimum density rule- and model-based methods in the floating-fill cases stems from the fill patterns associated with the fill generation methods. In the rule-based method, the fill metal is regularly spaced between adjacent signal lines and causes increases in coupling capacitance. In contrast, the model-based fill generation methodology does not place the fill metal in a regular pattern, which has the tendency to decrease the capacitance as has been observed with rule-based fill generation methodologies that produce staggered floating-fill patterns [19]. Since the model-based fill generation method utilized in this work is designed to reduce CMP-induced thickness variation only, the reduced capacitance in the floating-fill cases is an unintended consequence of the fill shapes utilized by the CMP-aware model-based fill generation method [11].

The breakdown of the capacitance increases due to dummy fill into ground and coupling capacitance components is important for understanding crosstalk-induced noise and delay. Table IV lists the average ground and coupling capacitance values for the wires in the top 60 delay paths and in the top 100 nets with the most noise normalized to the average capacitance values for the designs with no fill metal. In the floating-fill cases, the average coupling capacitance is approximately equal to the average coupling capacitance in the designs with no fill metal. However, the ground capacitance becomes larger due to coupling to ground through the floating-fill metal as depicted in Fig. 4. In the grounded-fill cases, the ground capacitance is significantly increased and the coupling capacitance is greatly decreased compared to the designs with no fill metal. The general trends in ground and coupling capacitances for the large-scale designs closely resemble the trends for the small-scale interconnect test structures.
TABLE III
INCREMENTAL INCREASE IN AVERAGE WIRE CAPACITANCE (ΔC) DUE TO DUMMY FILL INSERTION WITH CMP-INDUCED THICKNESS VARIATIONS

<table>
<thead>
<tr>
<th>Design</th>
<th>Buffer Spacing</th>
<th>No Fill Cap. (fF)</th>
<th>Incremental Capacitance Increase - Grounded Fill</th>
<th>Incremental Capacitance Increase - Floating Fill</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Max. Density Rule-Based</td>
<td>Min. Density Rule-Based</td>
<td>Model Based</td>
</tr>
<tr>
<td>Design A</td>
<td>1x</td>
<td>44.10%</td>
<td>10.34%</td>
<td>15.94%</td>
</tr>
<tr>
<td></td>
<td>2x</td>
<td>16.66%</td>
<td>6.52%</td>
<td>9.92%</td>
</tr>
<tr>
<td></td>
<td>3x</td>
<td>15.78%</td>
<td>6.44%</td>
<td>6.99%</td>
</tr>
<tr>
<td></td>
<td>10x</td>
<td>5.14%</td>
<td>3.10%</td>
<td>2.55%</td>
</tr>
<tr>
<td>Design B</td>
<td>1x</td>
<td>43.10%</td>
<td>9.38%</td>
<td>14.40%</td>
</tr>
<tr>
<td></td>
<td>2x</td>
<td>14.65%</td>
<td>6.02%</td>
<td>7.38%</td>
</tr>
<tr>
<td></td>
<td>3x</td>
<td>13.65%</td>
<td>5.93%</td>
<td>5.72%</td>
</tr>
<tr>
<td></td>
<td>10x</td>
<td>4.81%</td>
<td>3.47%</td>
<td>2.13%</td>
</tr>
<tr>
<td>Design C</td>
<td>1x</td>
<td>53.17%</td>
<td>17.25%</td>
<td>21.08%</td>
</tr>
<tr>
<td></td>
<td>2x</td>
<td>21.94%</td>
<td>10.81%</td>
<td>13.86%</td>
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<tr>
<td></td>
<td>3x</td>
<td>20.83%</td>
<td>10.66%</td>
<td>10.13%</td>
</tr>
<tr>
<td></td>
<td>10x</td>
<td>8.52%</td>
<td>5.88%</td>
<td>5.39%</td>
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TABLE IV
AVERAGE GROUND AND COUPLING CAPACITANCES VALUES NORMALIZED TO THE AVERAGE CAPACITANCE VALUES FOR THE DESIGNS WITH NO FILL

<table>
<thead>
<tr>
<th></th>
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<tr>
<td>Fill Method</td>
<td>1.57</td>
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<td>1.25</td>
<td>1.20</td>
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<td>1.11</td>
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<td>Buffer Spacing</td>
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<td>1.19</td>
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<th>Min. Density Rule-Based: Grounded</th>
<th>Model-Based: Grounded</th>
<th>Max. Density Rule-Based: Floating</th>
<th>Min. Density Rule-Based: Floating</th>
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C. Fill Impact on CMP-Induced Thickness Variation

Fig. 6 displays the CMP-induced metal thickness, ILD thickness, and cumulative topography variation ranges for designs with rule- and model-based fill normalized to the variation ranges associated with the designs with no fill. We define the thickness-variation range (ΔT) as the absolute difference between the largest and smallest metal thickness, ILD thickness, or cumulative topography value for each metal layer averaged over all of the metal layers. The thickness-variation range metrics (metal thickness, ILD thickness, or cumulative topography) are normalized by dividing the average ΔT values for the design with fill metal by the average ΔT value for the design with no fill metal. Note that the cumulative topography value at a given position on a particular metal layer is the summation of the metal and ILD thicknesses of the layers below the particular metal layer at the given position. The cumulative topography variation range has important implications for reliability and for depth of focus constraints as discussed in Section II-A.

The normalized ΔT values for metal thickness, ILD thickness, and cumulative topography exhibit similar trends for each fill generation method, level of buffer spacing, and design example as depicted in Fig. 6. For 1x buffer spacing, the maximum density rule-based fill method provides the smallest normalized ΔT values (ΔT < 10%) since the high metal density promotes a large degree of interconnect and ILD planarity. As the buffer spacing increases to 2x and 3x, the normalized ΔT
values for the designs with maximum density rule-based fill increase to the 25% to 35% range since the average metal density decreases as depicted in Fig. 5. For the designs with fill generated using the minimum density rule-based method, $\Delta T$ remains relatively constant for the 1x, 2x, and 3x buffer spacing cases due to the constant metal density across the three cases, and the normalized $\Delta T$ values range from 40% to 55%. For 10x buffer spacing, all of the fill methods provide relatively large $\Delta T$ values since the metal density is lowered to accommodate the large buffer spacing.

For the designs with fill metal generated using the model-based approach, the normalized $\Delta T$ values are substantially lower than those in the minimum density rule-based cases. Since the metal density of the designs with model-based fill is similar to the metal density of the designs with minimum density rule-based fill, the substantial improvement in $\Delta T$ associated with the model-based method can be attributed to its physics-based CMP-aware placement of the fill metal [11]. In several cases, the model-based method also provides lower $\Delta T$ values than the maximum-density rule-based method, which produces much larger metal density.

D. Delay Without Considering Crosstalk Effects

In this section, we discuss the delay implications of fill metal without explicitly considering the impact of crosstalk effects, which is the type of analysis performed in previous studies on dummy fill and timing [7], [13], [14]. We will contrast the data presented in this section with the results on crosstalk-induced delay in Sections V-G and V-H. Fig. 7 displays the critical path delay ($\Delta D$) and average delay ($\overline{\Delta D}$) without considering crosstalk effects for the top 60 delay paths for the different fill metal generation methods normalized to the delay of the design with no fill metal. To normalize $\Delta D$ and $\overline{\Delta D}$, we divide the delay for each delay path in the design with fill metal by the delay for the corresponding delay path in the design with no fill metal present. To obtain $\overline{\Delta D}$, we then average the normalized delay values for each delay path. Note that the path-wise delay, average crosstalk noise, and average crosstalk-induced delay results described in the following sections are normalized in a similar manner.

$\Delta D$ and $\overline{\Delta D}$ exhibit similar general trends with $\overline{\Delta D}$ typically being several percent larger than $\Delta D$. The $\overline{\Delta D}$ values averaged over the three fill generation techniques and the 4 simulated buffer spacing values for grounded fill are 5.2%, 4.9%, and 9.6% in designs A, B, and C, respectively, and for floating fill, the average $\overline{\Delta D}$ values are 2.2%, 1.7%, and 4.5% in designs A, B, and C, respectively. In terms of the fill generation methods, the relative delay increases closely match the trends for the average incremental wire capacitance increases displayed in Table III and discussed in Section V-B.

E. Path-Wise Timing Implications of Fill Metal

Since the timing requirements for a particular design can be violated due to delay increases on any given path, understanding the ways in which fill metal can impact timing on a set of individual delay paths is crucial. Fig. 8 displays the normalized increase in path delay and change in path order associated with the maximum density grounded rule-based fill generation method for design A compared to design A with no fill. Note that the delay paths (1 through 60) represent the delay between two unique sequential logic elements, and the paths are ordered in a descending manner based on their delay in the design with no fill present. Therefore, path 1 in Fig. 8 represents the critical delay path in design A with no fill.

The increase in delay on a particular path due to dummy fill can have a large range of values as depicted in Fig. 8(a). For the 1x buffer spacing case, the incremental increase in delay for a particular path ranges from 6.2% to 32.4%, and for the cases with 2x and 10x buffer spacing, the path delay increase ranges from 1.6% to 13.7% and from 0% to 6.5%, respectively. The large range of individual path delay increases also changes the relative order of the paths in terms of their delay as displayed in Fig. 8(b). Due to the large incremental delay increases associated with the fill metal, the critical delay path in the 1x buffer spacing design was the 11th longest delay path in the design with no fill metal. Furthermore, the critical delay path in the design with no fill metal becomes the 41st longest delay path in the...
**Fig. 8.** (a) Normalized increase in path delay and (b) change in path order associated with the maximum density grounded rule-based fill generation method for design A compared to design A with no fill.

**Fig. 9.** Absolute range of the normalized changes in path delay (maximum incremental change in path delay) for the top 60 delay paths.

Design with 1x buffer spacing. Therefore, the increase in delay for an individual path can greatly exceed the average delay increases reported in Fig. 7, and this can result in a significant re-ordering of the worst-case delay paths.

The wide range of delay increases for the individual delay paths occurs for all of the fill generation methods in each of the three design examples. Fig. 9 displays the absolute range of the normalized changes in path delay (maximum incremental change in path delay—minimum incremental change in path delay) for the top 60 delay paths. Note that design C has substantially smaller absolute path delay increase ranges than designs A and B since its top delay paths are individual signal lines in interconnect buses with a large number of bits. For designs A and B, the typical, maximum, and minimum path delay ranges for all of the fill generation methods are 6.9%, 26.2%, and 2.5%, respectively. Therefore, fill metal can cause significant delay increases in certain paths.

**F. Crosstalk-Induced Noise**

Fig. 10 depicts the average noise area (V-ns) (ΔN) for the 100 nets with the most noise in the designs containing fill metal normalized to the average noise area of the designs with no fill metal. For all of the simulated designs and fill configurations, the average normalized noise area (calculated based on 0.5 × (noise pulse width) × (noise pulse height)) for the top 100 nets with the most noise is 0.86 and 0.94 for the grounded and floating-fill cases, respectively. The reduction in ΔN for both the grounded and floating-fill cases can be attributed to the average normalized changes in ground and coupling capacitances listed in Table IV. In the floating-fill cases, the average coupling capacitance is approximately equal to the average coupling capacitance in the designs with no fill metal. However, the ground capacitance becomes larger due to coupling to ground through the floating-fill metal as depicted in Fig. 4. This leads to an average reduction in ΔN for the floating-fill cases, which is in contrast to previous predictions based on small-scale test cases that did not consider coupling to ground through the floating-fill metal [15], [16].

The fill generation method also plays a role in determining ΔN. As the buffer spacing is increased, ΔN becomes closer to the values obtained from the designs with no fill metal. In the ground-fill cases, ΔN for the designs with fill generated using the rule-based method with maximum metal density, the rule-based method with minimum metal density, and the model-based approach are 0.81, 0.90, and 0.87, respectively, which corresponds to the average metal density produced by the three fill generations methods of 38.4%, 19.9%, and 23.1%, respectively. In the floating-fill cases, ΔN for the aforementioned fill generation methods is 0.90, 0.94, and 0.99, respectively. The larger noise generated by the model-based method in the floating fill cases is due to the irregular spacing of the fill shapes required to achieve greater interconnect planarization [11], which increases the coupling-to-ground capacitance ratio as listed in Table IV.

While the insertion of fill metal reduces the average crosstalk noise area, the impact of fill metal on a particular net’s noise can significantly vary. The superimposed lines in Fig. 10 show the range of normalized noise area values for the 100 nets with the most noise. In general, the smallest and largest normalized noise area values are less in the grounded-fill cases than they are in the floating-fill cases. In some cases, the largest normalized noise area values can exceed 1. In these cases, the increase in metal and ILD thickness due to the improved interconnect planarization facilitated by the fill as well as the additional capacitive coupling between signal lines through the floating fill can lead to increases in crosstalk noise.
Fig. 10. Average noise area ($V_{ns}$) ($\Delta N$) for the 100 nets with the most noise in designs containing fill metal normalized to the average noise area of designs with no fill metal. Note that the superimposed lines show the range of normalized noise area values for the 100 nets with the most noise.

Fig. 11. Incremental crosstalk contribution to the path delay (total delay with crosstalk effects—delay without crosstalk effects) normalized to the no fill cases for the 60 largest delay paths.

G. Crosstalk-Induced Delay

The general trends associated with the different fill generation methods for crosstalk noise also exist for crosstalk-induced delay. Fig. 11 displays the average incremental crosstalk contribution to delay (total delay with crosstalk effects—delay without crosstalk effects) normalized to the no fill cases for the 60 largest delay paths. The average normalized crosstalk contribution to delay is typically less than the average crosstalk contribution to delay in the original designs without fill metal. The overall average normalized crosstalk-induced delay contribution for the designs with fill generated using the maximum density rule-based method, the minimum density rule-based method, and the model-based approach are 0.81, 0.92, and 0.88, respectively, for grounded fill, and 0.90, 0.96, and 0.95, respectively, for floating fill.

Based on the results presented in Fig. 11, the addition of grounded or floating-fill metal reduces the crosstalk contribution to the delay compared to the design with no fill metal present. Therefore, the normalized critical path and average delay ($\Delta D_{CT}$ and $\Delta D_{AV}$) due to fill metal when crosstalk effects are included in the analysis, which are displayed in Fig. 12, will be less significant than $\Delta D$ and $\Delta D$, which are depicted in Fig. 7. The $\Delta D_{CT}$ and $\Delta D_{AV}$ values for certain fill metal configurations, particularly in the grounded-fill cases, are less than the delay of the design with no fill metal present. Note that these crosstalk-induced delay trends are also observed in the small-scale test cases.
and (b) average delay (top 60 paths) with crosstalk noise included for different fill metal generation methods normalized to the delay of the designs with no fill metal with crosstalk noise included.

**Fig. 12.** (a) Critical path delay ($\Delta D_{cp}$) and (b) average delay (top 60 paths) ($\Delta D_{av}$) with crosstalk noise included for different fill metal generation methods normalized to the delay of the designs with no fill metal with crosstalk noise included.

H. Simultaneous Evaluation of Performance/Planarization

While the CMP-induced thickness variations, capacitance, delay, and noise are individually important, the overall effectiveness of a given fill generation technique must be evaluated by simultaneously evaluating all of the aforementioned metrics. Fig. 13 depicts the incremental wire capacitance and normalized average cumulative topography variation combinations ($\Delta C - \Delta T$ combinations) for the three design examples. For the design examples with grounded and floating maximum density rule-based fill, changing the buffer spacing from $1 \times$ to $10 \times$ results in an approximately linear tradeoff between $\Delta C$ and $\Delta T$. In contrast, the relatively constant metal density in the design examples with grounded and floating minimum density rule-based fill results in a smaller range of $\Delta C - \Delta T$ combinations. Overall, the minimum and maximum density rule-based fill methods produce designs with approximately the same performance in terms of $\Delta C - \Delta T$. The design examples with fill metal generated using the model-based method provide more desirable $\Delta C - \Delta T$ combinations than those generated using rule-based techniques when $1 \times$, $2 \times$, and $3 \times$ buffer spacing is utilized. This is due to the fact that the CMP-aware rule-based method from [11] places fill metal in a manner that reduces the CMP-induced thickness variations more effectively than the standard rule-based method for a given metal density as discussed in Section V-C.

We also simultaneously evaluate the CMP-induced thickness variation versus delay, both with and without crosstalk effects, and versus crosstalk noise for design example C in Fig. 14. The $\Delta D - \Delta T$ combinations depicted in Fig. 14 follow the general trend for the $\Delta C - \Delta T$ combinations depicted in Fig. 13 with the CMP-aware model-based method generally producing more favorable $\Delta D - \Delta T$ combinations than the rule-based approaches. However, when crosstalk effects are considered, the $\Delta D_{ct} - \Delta T$ combinations produced by the model-based method become less favorable. While the $\Delta D_{ct} - \Delta T$ combinations produced by the CMP-aware model-based method are still more favorable than those produced by the rule-based methods in design C, in designs A and B, certain maximum density rule-based cases actually provide superior $\Delta D_{ct} - \Delta T$ combinations to those produced by the CMP-aware model-based method. The $\Delta D_{ct}$ values significantly vary by design since they depend on the complex interplay between the delay contributed by the overall capacitance increases due to fill (Fig. 7) and the crosstalk contribution to delay (Fig. 11) as discussed in Section V-G.

The simultaneous evaluation of crosstalk noise and CMP-induced thickness variations depicted in Fig. 14 reveals that the maximum-density rule-based method produces superior $\Delta N - \Delta T$ combinations for design C. We also observe this trend for designs A and B. As discussed in Section V-F, the maximum density rule-based method provides greater coupling capacitance decreases for both floating and grounded fill than the minimum-density rule- and model-based methods. This allows the maximum density rule-based method to more effectively suppress the crosstalk noise in the designs. Given the fact that rule-based methods can outperform model-based methods that target CMP-induced thickness variations alone with respect
to certain combinations of performance metrics, model-based methods that simultaneously target all critical performance metrics including CMP-induced thickness variations, interconnect capacitance, crosstalk-induced delay, and crosstalk noise are needed in the future to comprehensively optimize interconnect performance and reliability in the presence of dummy fill.
VI. DISCUSSION AND CONCLUSION

In this paper, we presented a comprehensive investigation of the crosstalk-induced delay, noise, capacitance, and CMP-induced thickness variations associated with fill generated using rule-based and CMP-aware model-based methods for large-scale designs implemented in 65 nm process technology. Based on the results presented in this paper, we can provide several important conclusions.

1) The incremental capacitance, delay, and noise impact of fill is significant in nanoscale process technologies.

2) The fill generation method utilized greatly impacts the achieved capacitance, delay, noise, and interconnect planarization.

3) The shielding effect of grounded fill leads to smaller average crosstalk-induced noise and delay values compared to the design with no fill metal.

4) Large-scale designs with floating fill also typically experience a reduction in average crosstalk-induced noise and delay due to increased interlayer coupling to ground through the floating fill, which is in contrast to the predictions of previous studies.

5) The delay and noise impact of fill metal greatly varies depending on the individual net in the circuit, which can significantly change the critical delay path, the delay path ordering, and the path-wise crosstalk noise.

The aforementioned conclusions have important ramifications for the development and utilization of automated design methods for fill generation in current and future process technologies. Most importantly, given the difference in behavior between the crosstalk-induced delay results presented in Section V-G and the delay results without considering crosstalk effects discussed in Section V-D, future fill generation techniques and studies analyzing the performance impact of fill metal must take crosstalk delay effects into account. Furthermore, DFM-aware fill metal generation solutions should attempt to constrain the path-wise delay and noise increase based on each path’s available timing and noise slack while simultaneously achieving acceptably low CMP-induced thickness variation. The power consumption increase caused by the larger interconnect capacitance due to the inserted fill metal [34], [35] as well as other noise effects such as power supply noise and charge sharing [36], [37] may also need to be considered in future fill metal generation solutions.

While model-based fill generation techniques that simultaneously consider wire capacitance, crosstalk-induced delay, noise, power consumption, and interconnect planarization have yet to be developed [5], previous research on the development of fill generation techniques has provided important insights into the potential approaches for generating a comprehensive model-based fill synthesis framework [6]–[14]. The results presented in this paper underscore the pressing need for automated fill metal generation techniques that concurrently consider the aforementioned performance and reliability metrics, particularly crosstalk-induced delay and noise, for integrated circuits implemented in nanoscale process technologies.

ACKNOWLEDGMENT

The authors would like to thank C. Chiang, S. Sinha, Q. Su, and Q. Lu at Synopsys for their useful discussions pertaining to the design examples and to the model-based CMP-aware fill generation method.

REFERENCES


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