Inelastic Electron Tunneling Spectroscopy Study of Thin Gate Dielectrics

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A broad range of materials is currently being studied for possible use as the insulating layer in next generation metal-oxide-semiconductor transistors. Inelastic electron tunneling spectroscopy (IETS) has become a powerful tool to characterize both the structural and electrical properties of the resulting device structures made from these materials. IETS can address issues related to reactions and intermixing at interfaces, as well as properties related to carrier mobility, such as phonon modes and charge traps, for structures that are difficult to characterize accurately by other techniques.

1. Introduction
The remarkable advancement of computational power over the last few decades is the result of relentless efforts to shrink the size of the transistors that make up integrated circuits. This advancement has required that the equivalent oxide thickness (EOT) of the gate dielectric in the dominant complementary metal-oxide-semiconductor (CMOS) technology shrink in each new generation of integrated circuits in order deliver gains in performance and circuit density, a trend that is expected to continue.[1] As a result, tunneling currents through the gate dielectrics have become a major concern as the scaling trend continues for future generations of devices.

When the gate dielectric is only a few atomic layers, many conventional dielectric characterization tools, such as infrared spectroscopy, Raman spectroscopy, neutron scattering, and Rutherford backscattering, are ineffective at revealing structural and compositional information about the gate oxide. In contrast, the inelastic electron tunneling spectroscopy (IETS) technique, which is the topic of this Research News, becomes more sensitive for these metal-oxide-semiconductor (MOS) structures with an ultrathin gate dielectric.[2–4] This enhanced sensitivity is because IETS relies on a tunneling current to probe the structures, and this current increases as the gate dielectric thickness decreases. A wide variety of information about a MOS sample can be obtained by IETS with excellent sensitivity and resolution, including: phonon modes of the gate electrodes, dielectric, and substrate; various vibrational modes of the bonding structures at interfaces; impurities in the gate dielectric and at interfaces; trap levels and other electronic defects.

2. Basic Principles of IETS
The basic principles of the IETS technique are illustrated in Figure 1a. The total tunneling current across an insulating layer is measured as a function of applied voltage. In the absence of inelastic interactions, the I–V characteristic is a smooth curve, and its second derivative is nearly zero. However, when the applied voltage causes the Fermi level separation to be equal to the characteristic interaction energy of an inelastic energy loss event for the tunneling electron (see the middle band diagram in Figure 1a), an additional conduction channel related this inelastic event becomes available,[5] causing an increase in the slope of the I–V characteristic at this voltage. This change in slope of the I–V characteristic corresponds to a peak in its second derivative plot at a voltage corresponding to the characteristic energy of the inelastic interaction. Furthermore, the area under the peak is proportional to the strength of the inelastic interaction. In a typical MOS sample, IETS detects numerous inelastic modes corresponding to the wide variety of inelastic interactions that influence the tunneling current.

3. IETS Measurement Technique
The IETS spectrum is essentially a $dI/dV^2$ versus $V$ plot, where $I$ is the tunneling current and $V$ is the applied voltage. Therefore, it may seem that the simplest way to obtain the IETS spectrum is to measure the $I$–$V$ curve and then employ mathematical differentiation of the data to determine the first and second derivatives. However, this approach is rarely successful in isolating important features of a particular MOS structure due to unfavorable signal-to-noise ratios. A far more sensitive approach to collecting IETS spectra, which is used for the spectra discussed below, is an ac modulation/phase-sensitive detection technique.[6]

This ac modulation technique uses a small sinusoidal signal to modulate the voltage across the MOS sample. The response of the ac current through the sample to this modulation is then measured using a lock-in amplifier. Normally, a lock-in amplifier is used to identify the first harmonic component of a response
signal. For IETS, however, the most important response is in the second harmonic component, since the IETS spectrum is directly proportional to the amplitude of this second harmonic component. Mathematically, this result can be derived by taking a Taylor expansion of the \( I-V \) curve around a voltage bias \( V_b \) with \( V_m \cos \omega t \) as a small perturbation:

\[
I(V_b + V_m \cos \omega t) = I(V_b) + dI/dV |_{V_b} V_m \cos \omega t + \ldots
\]

\[
+ d^2I/dV^2 |_{V_b} V_m^2 \cos^2 \omega t + \ldots
\]

\[
= I(V_b) + G' |_{V_b} V_m \cos \omega t + \ldots
\]

\[
G'' |_{V_b} V_m^2(1 + \cos 2\omega t) + \ldots
\]

The first derivative of \( I \) is the conductance, \( G \), and the second derivative of \( I \) is the IETS signal, \( G' \). From Equation 1, it is clear that the coefficients of \( \cos \omega t \) and \( \cos 2\omega t \) in the Taylor expansion are proportional to these two derivatives of the \( I-V \) characteristic. As a result, lock-in detection of the first and second harmonic gives a scaled measure of the first and second derivative of the \( I-V \) curve, respectively. The lock-in measurement technique dramatically improves signal-to-noise performance over mathematical differentiation of the \( I-V \) curve since noise signals at frequencies other than the modulation frequency, \( \omega \), are rejected.

### 3.1. Modulation and Thermal Broadening

Many of the inelastic features of interest have intrinsic line widths or separations between features that are only a few millivolts. As a result, it is important for IETS to have sufficient resolution to identify such features clearly, which in turn depends on controlling the two most commonly encountered line width broadening effects: thermal broadening and modulation broadening.

Thermal effects will give rise to a full width at half maximum (FWHM) line width broadening of 5.4 \( kT \) in an IETS spectrum,[7] where \( k \) is the Boltzman constant and \( T \) is the temperature. This thermal effect translates into a broadening of 140 mV at room temperature, 35 mV at 77 K, and 1.9 mV at 4 K. In order to achieve acceptable resolution, therefore, most IETS spectra, including those reported in this Research News, have been taken at liquid helium temperature. However, there are certain features, such as the traps discussed later (Section 6), that can be observed clearly even at room temperature.

The lock-in measurement technique described above requires the selection of a particular amplitude for the ac modulation voltage. Modulation broadening refers to the fact that as this ac amplitude is increased, the minimum width in energy of a feature that can be resolved by IETS also increases because each point in the spectrum reflects the response of the sample averaged over a larger voltage range. The minimum energy resolution of IETS due to this modulation voltage effect has been calculated as \( 1.22 V_m \text{FWHM} \).[7,8] Therefore, for the best energy level resolution, a small ac modulation is desirable. However, for the best signal-to-noise performance, a large ac modulation voltage is desirable since the intensity of the IETS signal is proportional to the modulation amplitude. Taking both of these effects into consideration, an ac modulation voltage of 2 mV is a typical choice for IETS measurements on MOS structures since the resulting modulation broadening is on the order of the thermal broadening at 4.2 K.

### 3.2. Background Subtraction

While the primary features of interest in an IETS spectrum are due to inelastic tunneling, the IETS measurement also includes a significant contribution from elastic tunneling. In order to identify with the highest sensitivity the inelastic features, it is desirable to have a technique to subtract out the elastic tunneling background. An effective technique to accomplish this background subtraction utilizes the fact that the elastic tunneling background is a very weak function of temperature, while there is a strong dependence of the inelastic tunneling peak line widths on temperature, as discussed above.[8]

The first and second derivatives of the \( I-V \) curves can be expressed in terms of elastic and inelastic components of the conductivity, \( G = G_o + G_i \). Information about the inelastic modes, such as dielectric phonons, is entirely contained in \( G_i \), while the IETS technique measures \( G' \). The inelastic conductance, \( G_o \), is a thermally broadened step function with a temperature-independent height for a given inelastic mode. As a result, peaks in \( G'_i \) have a height that varies as \( 1/T \) and a width that varies as \( T \). At elevated temperatures, \( G'_i \) becomes an increasingly smooth function of voltage, while at temperatures that approach 0 K, \( G'_i \) becomes a more and more sharply peaked function of voltage. To exploit this temperature dependence in order to achieve the best possible estimate of \( G'_i \) from measurements of \( G' \), one can...
subtract the $G'$ measured at high temperature (normally 77 K) from $G'$ measured at the lowest attainable experimental temperature (normally 4.2 K). Since the elastic component of the conductivity, $G_0$, does exhibit a small dependence on temperature, it is necessary to define a ratio,

$$\rho = \frac{\left[ G'_{\text{4.2K}} \right]}{\left[ G'_{\text{4K}} \right]} \approx \frac{\left[ G'_{\text{77K}} \right]}{\left[ G'_{\text{4K}} \right]}$$

between the elastic components in IETS spectra at the temperatures of 77 K and 4.2 K. The value of $\rho$ can be determined quite accurately from measurements. In practice, after the IETS spectra for a MOS sample are collected at both 4.2 K and 77 K, $\rho$ is calculated by comparing these two spectra at a voltage where the inelastic fluctuations make a relatively small contribution to the total IETS signal. The IETS spectrum taken at 77 K divided by this constant $\rho$ is used to approximate the elastic background at 4.2 K. The estimate of the net inelastic spectrum, $G''$, is obtained by subtracting this elastic background spectrum from its $G'_{\text{4.2K}}$ counterpart.

### 3.3. Bias Polarity Dependence of the Inelastic Interaction

IETS spectra can be collected with either a positive or negative applied voltage. In either case, peaks in the spectra correspond to the same energy of inelastic interaction, but with the electron tunneling in opposite directions. The tunneling electron loses energy after an inelastic interaction, and its subsequent tunneling probability is reduced due to the increased effective tunnel barrier. As a consequence of this mechanism, the intensity of the peak in the IETS spectrum due to an inelastic interaction event near the interface where electrons are being injected into the oxide will be smaller than the peak due to a similar event near the opposite interface. The tunneling electron in the former case travels through most of the barrier with a lower electron energy (and thus it sees a higher tunnel barrier) than in the latter case. A more quantitative theoretical treatment of this phenomenon confirms this intuitive picture of the bias polarity dependence of IETS feature amplitude.

### 4. IETS Results for SiO$_2$/Si Gate Stacks

IETS measurements have been used to study SiO$_2$/Si systems for years because of its importance to CMOS technology. Since a vast knowledge base exists about this system from other characterization techniques, results for SiO$_2$/Si have been used to calibrate and validate the IETS technique. Figure 1b shows an example of the IETS spectrum for a high quality SiO$_2$ thin film grown thermally on Si. The most prominent features in this spectrum are those associated with Si phonons (between 10 mV and 70 mV) and those associated with various SiO$_2$ modes (between 135 mV and 170 mV). With the help of existing infrared absorption (IR) and neutron spectroscopy data published in the literature, a detailed analysis of the IETS spectrum leads to assignments that associate IETS features with various excitations of both the oxide barrier and the Si electrodes. The region of the spectrum between 10 mV and 70 mV corresponds to the expected Si phonon modes (both acoustic and optical ones), while the features between 135 mV and 170 mV are consistent with excitations of several oxide modes.

Because of the adequate signal-to-noise ratios and the very high stability and reproducibility of the IETS signals in these samples, a precise spectral analysis can be performed that deconvolves overlapping features and quantifies their relative contributions. For example, the region between 20 mV and 70 mV in Figure 1b reveals five overlapping modes. On the basis of a numerical deconvolution using Gaussians fits, these modes can be identified. The three peaks in the middle of the spectrum all arise from Si phonons (the one at 44 mV corresponds to the $\Sigma$ or $\Delta$ LA mode, the one at 53 mV corresponds to the $\Delta$ LO mode, and the one at 59 mV corresponds to $\Sigma$ or $\Sigma$ TO mode). The right-most peak at 63 mV corresponds to a LO rocking mode in SiO$_2$. A similar SiO$_2$ TO mode at 56 mV, expected to be weak, does not appear. The deconvolved modes in the range between 135 mV and 170 mV in Figure 1b are consistent with the following SiO$_2$ asymmetric stretch vibrational modes: an LO4 mode at 144 meV, a TO4 mode at 150 meV, and an LO3 mode at 155 meV. The origin of the feature at 165 meV is consistent with a vibrational mode resulting from phosphorus in the oxide.

In addition to the ability of IETS to probe microscopic bonding structures in the SiO$_2$/Si system, IETS can be used to study the effects of various CMOS fabrication processes. Wafer surface cleaning of the silicon prior to the formation of the gate oxide has been shown to have a significant effect on IETS spectra. In one study, two MOS samples were processed the same way, except that the top sample was treated with HF vapor and the bottom sample was treated with diluted HF (DHF) solution prior to the formation of thermal SiO$_2$. While the silicon phophon part of the spectrum (45 mV to 70 mV) is substantially the same for both samples, other parts are distinctly different. In particular, the IETS for the HF vapor-treated sample shows a broad hump between 20 mV and 40 mV, which may be associated with the excitation of a Si–F vibrational mode. In this way, IETS can provide specific information about the effect of wafer cleaning on the resulting MOS structure.

IETS can also be applied to the study of the effect of electrical stress on a MOS structure. When a MOS structure is subjected to such stress, characteristic features emerge in the IETS spectrum. These effects have been carefully studied in the SiO$_2$/Si system, where features between 130 mV and 170 mV, which are associated with the bonding structure of the silicon oxide barrier, are observed to change gradually with increasing stress time, while new features between 200 mV and 320 mV are created as the electrical stress progresses. The changes between 130 mV and 170 mV are consistent with the reordering of the microscopic bonding configurations in the silicon oxide barrier due to hot-electron induced structural damage, while the newly created features between 200 mV and 320 mV are associated with electron traps generated by the electric stress, which will be discussed in more detail in Section 6. In a separate study, the effect of electrical stress in a SiO$_2$/Si structure on Si phonons in the energy range below 80 mV has been measured. A significant shift in the energy of Si longitudinal phonon modes.

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is observed after constant voltage stress, but transverse phonon modes are largely unaffected.

5. IETS Results for high-k/Si Gate Stacks

The correspondence between IETS measurements on SiO$_2$/Si structures and other experimental techniques has established IETS as a reliable characterization tool. As a result, IETS is well suited to studying candidate materials for high-k dielectric oxide replacement of SiO$_2$ in CMOS technology where, due to the nanometer thickness of the relevant structures, other characterization tools cannot be easily employed. We discuss the application of IETS to two high-k candidate materials: HfO$_2$ and LaAlO$_3$.

HfO$_2$ is the high-k gate dielectric of choice for current CMOS technology and has also received the most attention of all high-k gate dielectrics. IETS can provide a wealth of information about the HfO$_2$/Si MOS interface structure and the phonon modes that degrade channel mobility. Figure 2a and 2b show the IETS spectra of an Al/HfO$_2$/Si sample for two important energy ranges.$^{[11,12]}$ This sample was sintered at 600 °C in N$_2$ in order to cause crystallization of the HfO$_2$. As a result, most of the HfO$_2$ IETS peaks are consistent with phonons of the monoclinic crystalline phase, although there is a weak peak at 67 mV corresponding to the tetragonal phase.$^{[11]}$ In addition, there is a peak corresponding to a Hf–Si–O bond, most likely related to the interfacial layer between HfO$_2$ and Si, and a peak corresponding to an Al–O bond, probably due to the reaction between HfO$_2$ and the top Al electrode. The reverse-biased (negative gate) spectrum contains many Si–O related features, suggesting a high density of Si–O bonds near the Si/HfO$_2$ interface, while the forward-biased (positive gate) spectrum shows primarily Hf–O features near the electrode/HfO$_2$ interface.

The carrier mobility in MOS field effect transistors (MOSFETs) made of high-k gate dielectrics is degraded because of the soft optical phonons in the high-k gate dielectric.$^{[14]}$ The reason that phonon scattering related to the high-k material is significant is because the optical phonon energies in high-k dielectrics are low enough to enable efficient electron–phonon interactions, while the corresponding phonons in lower-k gate dielectrics have energies too high for such interactions. IETS is ideally suited to probing this mechanism since electron–phonon interactions appear explicitly as peaks in the IETS spectrum. For example, in the IETS spectrum of an Al/HfO$_2$/Si sample shown in Figure 2a, one can clearly see the Hf–O vibrational modes around 15 mV, 35 mV, and 70 mV. Note that these modes are very close to the substrate Si phonon energies and are much lower than Si–O vibrational modes shown in Figure 2b. Since the Si phonons are efficient scatterers for the channel electrons, one would expect the same for the Hf–O modes on account of their very similar energies. In contrast, the energies of the Si–O vibrational modes are too high to cause significant scattering of the channel carriers.

In addition to HfO$_2$, other high-k gate dielectrics on silicon have also been studied by IETS. LaAlO$_3$ is of particular interest because of the possibility of epitaxial growth on Si,$^{[15]}$ without developing a SiO$_2$-like interfacial layer.$^{[15,16]}$ Figure 2c shows the IETS spectra of an epitaxial LaAlO$_3$/Si structure with a top Al electrode measured under positive and negative gate voltages. The modes obtained from deconvolving these IETS spectra can be identified with those measured on single-crystal LaAlO$_3$ by IR and Raman spectroscopy, as well as by theoretical calculations.$^{[17]}$ These phonon modes are located below 150 mV. The absence of Si–O bonds at the LaAlO$_3$/Si interface is evident in Figure 2c, since no detectable features appear near 150 mV, while the vibrational energies for Si–O bonds are distributed (as seen in Figure 2b).

6. IETS Studies of Traps

Traps in the gate dielectric can cause at least two different kinds of adverse effects in a MOSFET: (1) trap-assisted conduction, which causes an increased gate leakage current, and (2) trapping of carriers, which causes a shift in the threshold voltage and reduced carrier density.$^{[18]}$ IETS provides a direct characterization method for these two kinds of traps, which is not available from conventional measurements.

The I–V and IETS (d$^2$I/dV$^2$–V) plots associated with both of these trap effects are shown...
The strength of features in the positive-bias region will generally be different than for the corresponding features in the negative-bias region due to the asymmetry of the tunnel barrier. This dependence of IETS on both voltage and tunneling direction provides information that allows an accurate estimate of trap energy and position.

The model that allows such estimates of trap properties from IETS data is straightforward, and we outline it below. Assume that the total physical thickness of the dielectric is $x_0$, with a non-uniform dielectric constant, $\varepsilon(x)$. We wish to estimate the trap energy $\varepsilon(x)$ at a point $x_t$ from the silicon interface, at an energy $V_f$, defined as the energy above the Fermi level of the silicon, at which point trap-assisted tunneling will start to take place.

The IETS spectrum for charge trapping shows a valley followed by a peak feature. Both of these trap-related IETS features are relatively easy to distinguish from other IETS features, such as those due to phonons or other vibrational modes, because only trap features consist of both peaks and valleys; IETS features related to inelastic tunneling mechanisms manifest only as peaks.

Figure 3. a) Schematic illustrating the two different effects traps have on IETS spectra. Curve (1) represents trap-assisted conduction, and Curve (2) represents carrier trapping. b) IETS spectrum observed on a HfO$_2$/Y$_2$O$_3$ bilayer structure, where trap levels are identified by the nine arrows. Inset shows a transmission electron micrograph of the structure. Reproduced with permission from [21]. Copyright 2008, American Institute of Physics. c) IETS spectra of an n-MOSFET after a series of electrical stresses. The trap-related features that emerge with stress can be correlated with changes in the gate leakage and drain currents. Reproduced with permission from [12]. Copyright 2005, IEEE.
The occurrence of electron trapping and trap-assisted conduction after electrical stress inferred from $I–V$ characterization of the $n$-MOSFET can be directly verified by IETS measurements on the same structure.

Figure 3c shows the IETS spectrum of the $n$-MOSFET structure measured in the inversion region at liquid helium temperature.[22] A prominent trap-assistant tunneling feature (peak followed by valley) existed in the original spectrum at around 730 mV. A charge-trapping feature (valley followed by peak) appears around 320 mV after 300 seconds of stress. Other features highlighted in Figure 3c appear upon application of electrical stress and consist of combinations of charge trapping and trap-assisted conduction mechanisms, but are difficult to resolve due to the overlap of multiple features.

Despite the ability to obtain IETS spectra from MOSFETs with non-degenerate semiconductor substrates discussed above, there are limitations; IETS spectra can be obtained when the MOSFET is biased in inversion, but not in accumulation due to the freeze-out of majority carriers at 4.2 K. As a result, it is not possible to estimate the physical locations, energy levels, and densities of the traps in the gate dielectric of a MOSFET because these calculations require IETS data for both voltage polarities. A possible solution is to use a special structure with both an $n$+ source and drain and a $p+$ source and drain so that good electrical contact is made to the channel for both inversion and accumulation. With such a structure, IETS spectra for both polarities can be measured, thus allowing determination of the physical locations, energy levels, and densities of the traps in a MOSFET without a degenerate semiconductor substrate.

### 7. Conclusions

The development of MOSFETs that meet the requirements of continued scaling will require insights from a variety of experimental probes and techniques. IETS is particularly well suited to providing crucial information about potential high-k gate stacks, such as HfO$_2$/Y$_2$O$_3$ bilayer MOS device after 400, 600, and 800°C N$_2$ anneals, respectively.[21] A number of trap levels first appear after a 400°C N$_2$ anneal and become more prominent after a 600°C N$_2$ anneal, as can be seen in Figure 3b, where these trap levels are numbered.

Quantitative analysis of the IETS data indicates that these trap levels are located at the HfO$_2$/Y$_2$O$_3$ interface. Qualitatively, this can be inferred from Figure 3b by noting that the trap features are nearly symmetric about 0 V. Applying Equation 6, where $V_f = -V_i$, the model predicts a trap approximately in the middle of the structure. These trap levels are likely caused by valence and strain mismatches between HfO$_2$ and Y$_2$O$_3$. The weakening of trap features at 800°C is attributed to the reduction of strain at the interface due to diffusion and intermixing.[23]

The IETS results presented above are from MOS capacitors with degenerate Si substrates, which are used to avoid freeze-out of carriers at the liquid helium temperature required for the measurements. A MOSFET device structure without a degenerate semiconductor substrate can also be measured by IETS techniques at liquid helium temperatures by biasing the MOSFET in inversion. The advantage of such an approach is that the effects of electrical stress on transistor performance can be correlated with IETS features on the same device. In one such experiment, an $n$-MOSFET device with a HfSiON dielectric was measured by IETS before and after constant gate dc voltage stress of various durations.[12] The gate voltage stress causes significant changes in the $I_f–V_f$ characteristic; a shift toward more positive $V_f$ as the stress time increases is observed, along with an overall decrease of the drain current. Both of these phenomena are consistent with electron trapping, which is expected to shift the threshold voltage and reduced both free electron density electron mobility for a given gate voltage. An increased gate leakage current as the dc gate voltage stress continues is also observed. These results are consistent with the stress induced leakage current (SILC) mechanism for thin gate dielectrics,[22] suggesting that trap-assisted conduction mechanisms are enabled by stress-induced electronic traps in the gate oxide.

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