



## Science Letters:

# A Robust Polysilicon-Assisted SCR in ESD Protection Application\*

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**Abstract:** A Novel polysilicon-assisted SCR is presented and analyzed in this paper, which is fabricated in HHNEC's 0.18 $\mu$ m EEPROM process. The polysilicon-assisted SCR's take advantage of polysilicon layer to help bypassing ESD current without occupying extra layout area. TLP I-V measurement results show that given the same layout areas, robustness performance of polysilicon-assisted SCR's can be improved to the 3 times of conventional MLSCR's. Moreover, one-finger such polysilicon-assisted SCR's, which occupy only 947 $\mu$ m<sup>2</sup> layout area, can undergo 7-kV HBM ESD stress. Results further demonstrate that the S-type current-voltage (I-V) characteristics of polysilicon-assisted SCR's are adjustable to different operating conditions by changing the device dimensions. Compared with traditional SCR, this new SCR can bypass more ESD currents and consumes smaller IC area.

**Key words:** Electro-static discharge (ESD), Silicon-controlled rectifier (SCR), Robustness performance, Polysilicon-assisted, Human body model (HBM)

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ESD (Electro-Static Discharge) is one of the most important issues on IC reliability. As the technology is scaled down constantly, the demand for high performance ESD protection devices is becoming more and more urgent (Wang 2004; Wang, Hai-gang et al., 2005; Chang and Ker, 2007; Chun-Yu and Ming-Dou, 2007; Si Moussa, El Kaamouchi et al., 2007). ESD protection in ICs is established by involving integration of the input/output (I/O) protection, and the supply clamp. These protection components are typically implemented with diodes, MOSFETs, bipolar junction transistors, and sometimes SCR's. Robustness performance is one of the most important concerns that should be taken into account when designing such ESD protection devices (Salcedo, Liou et al., 2005; Liou, Salcedo et al., 2007). Although MLSCR, one of the conventional SCR's, has better robustness performance than other

traditional devices in double-well submicron technology, the robustness requirements can be obtained only by multiplying the MLSCR's fingers. In general, multiple-finger devices consume much more area than one-finger ones. Facing the challenge of robustness performance and over-sized IC area, novel polysilicon-assisted SCR's are developed and analyzed in this paper.

## STRUCTURES AND TERMINAL CONNECTION

The conventional SCR-based ESD protection device's structure, named as MLSCR, is demonstrated in Fig. 1. An N<sup>+</sup> region is located above the boundary region of NWELL and PWELL. One of the novel SCR-based ESD protection devices' structures, named as FDSCR (Forward Diode Silicon Controlled Rectifier), is depicted in Fig. 2, from which we can observe that the device is built with two

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parts, substrate silicon part and polysilicon part. The two parts are paralleled, thus the device can bypass more current under ESD without extra layout areas. Polysilicon part actually consists of paralleled diodes (Fig. 2b). Every diode is formed with P-type polysilicon, intrinsic polysilicon and N-type polysilicon. The holes in the polysilicon layer ensure that N+ implant can go through to form N+ region bestraddling NWELL and PWELL. There is one STI region surrounding one N+ region in every hole. Substrate silicon part is quite like the conventional MLSCR depicted in Fig. 1, except that the N+ region is separated and discontinuous in FDSCR while N+ region is continuous in MLSCR. These devices have been designed in the process of HHNEC's EE180 G. Another SCR-based ESD protection devices' structure, named as RDSCR (Reverse Diode Silicon Controlled Rectifier), is presented in Fig. 3. In RDSCR, N-type polysilicon is connected to the anode terminal and P-type polysilicon to the cathode terminal, and this is the only different point from FDSCR. All the SCRs in this paper, no matter MLSCRs, FDSCRs, or RDSCRs, occupy the same layout area (Fig. 4, and Table 1). Dimensions of "W" and "D" are the same in all the SCRs. Detailed dimensions of "D" (D1, D2, D3, D4 and D5 in Fig. 1, 2, 3) are also fixed (Table 1). The value of "L" is changeable in FDSCRs and RDSCRs.

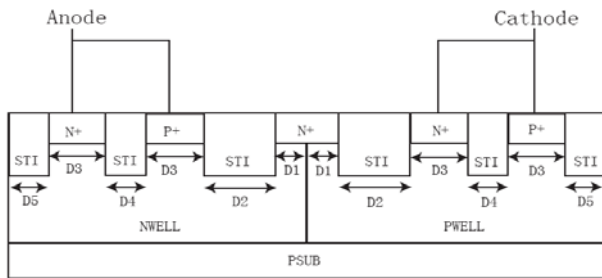


Fig. 1 Cross section of conventional MLSCR

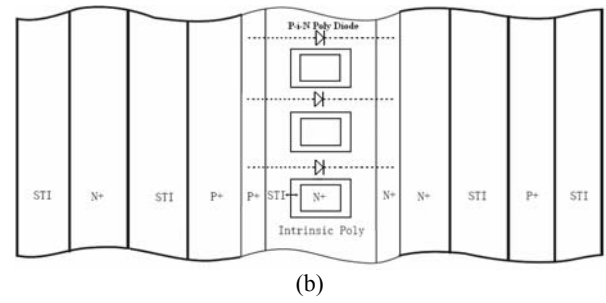
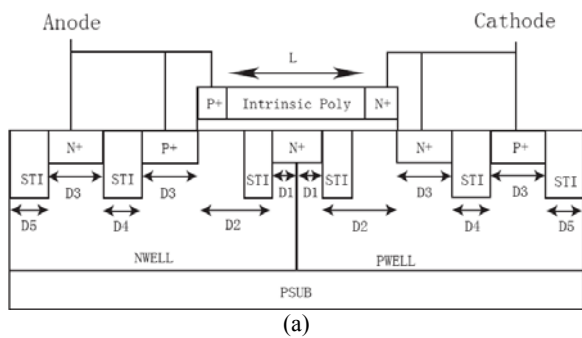


Fig. 2 Structure of FDSCR  
(a) Cross section of FDSCR (b) Planform of FDSCR

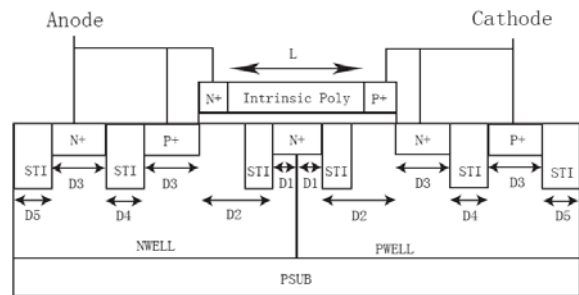


Fig. 3 Cross section of RDSCR

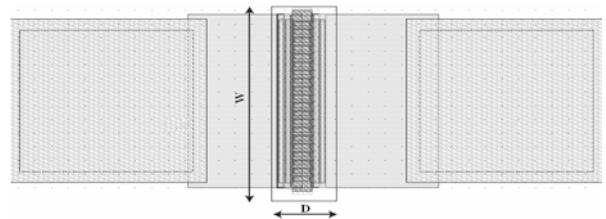


Fig. 4 Overall layout of MLSCRs, FDSCRs, and RDSCRs

Table 1 Dimensions of MLSCRs, FDSCRs, and RDSCRs

D1	D2	D3	D4	D5	D	W
( $\mu\text{m}$ )	( $\mu\text{m}$ )	( $\mu\text{m}$ )	( $\mu\text{m}$ )	( $\mu\text{m}$ )	( $\mu\text{m}$ )	( $\mu\text{m}$ )
2.14	1.36	1.5	0.5	0.36	14.7	65

## MEASUREMENT RESULTS OF ROBUSTNESS PERFORMANCE

Fig. 5 is the measured TLP I-V characteristics of MLSCR, FDSCR and RDSCR. At DP\_ML\_1, the leakage current of MLSCR is increased by three orders, and this device fails at DP\_ML\_2. At DP\_FD and DP\_RD, the leakage currents are suddenly increased by six orders to failure. In Table 2, area-considered robustness performance is evaluated by " $I_{ESD}/\mu\text{m}$ " and " $V_{ESD}/\mu\text{m}^2$ " (1) (2). The leakage current of MLSCR is firstly increased to the orders of  $10^{-6}\sim 10^{-5}$ , and then reaches  $10^{-3}\sim 10^{-2}$ , which shows the latent vulnerability of MLSCR's robustness. In

contrast, leakage currents of FDSCR and RDSCR are increased abruptly from the order of  $10^{-9} \sim 10^{-8}$  to the order of  $10^{-3} \sim 10^{-2}$ . The results show that, robustness performance of FDSCR and RDSCR can be increased by 80 percent, and if latent robustness problems taken into account, robustness performance of RDSCR and RDSCR is at least 3 times of that of MLSCR.

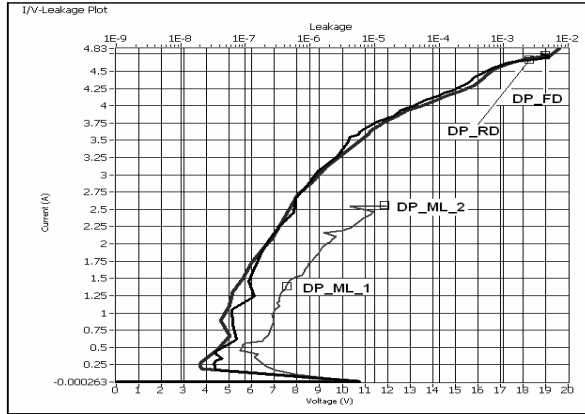


Fig. 5 Characteristics of MLSCR, FDSCR and RDSCR

Table 2 Comparing robustness performance (a) Leakage currents of the three devices (b) Latent robustness problem ignored. (c) Latent robustness problem considered.

(a)

Devices	Order of Leakage Currents		
	$10^{-9} \sim 10^{-8}$	$10^{-6} \sim 10^{-5}$	$10^{-3} \sim 10^{-2}$
MLSCR	$0 < I < 1.37$	$1.37 < I < 2.6$	$I > 2.60$
FDSCR	$0 < I < 4.68$	-	$I > 4.68$
RDSCR	$0 < I < 4.66$	-	$I > 4.66$

(b)

Devices	$I_{t2}$ (A)	$I_{ESD}/\mu m$ (mA/ $\mu m$ )	$V_{ESD}/\mu m^2$ (V/ $\mu m^2$ )
MLSCR	2.60	40.0	4.08
FDSCR	4.68	72.0	7.41
RDSCR	4.66	71.7	7.38

(c)

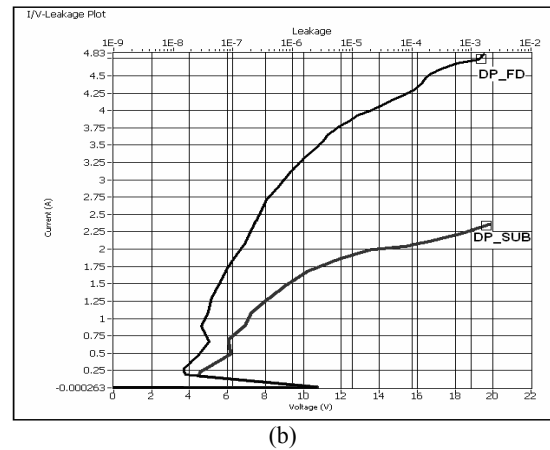
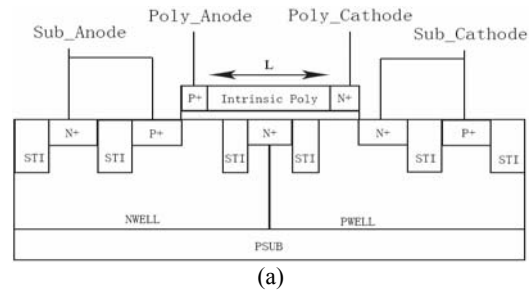
Devices	$I_{t2}$ (A)	$I_{ESD}/\mu m$ (mA/ $\mu m$ )	$V_{ESD}/\mu m^2$ (V/ $\mu m^2$ )
MLSCR	1.37	21.1	2.15
FDSCR	4.68	72.0	7.41
RDSCR	4.66	71.7	7.38

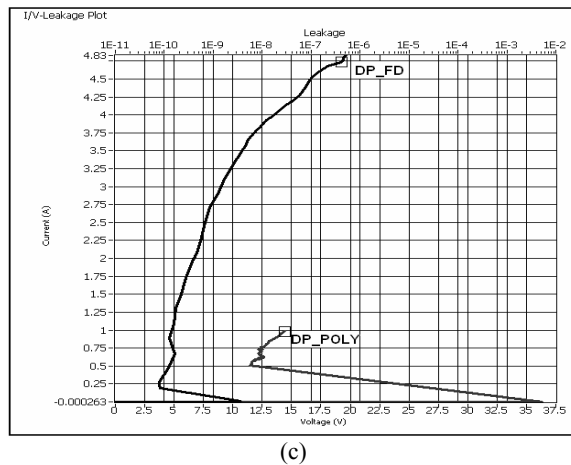
$$I_{ESD} / \mu m = \frac{I_{t2}}{W} \quad (1)$$

$$V_{ESD} / \mu m^2 = \frac{I_{t2} \times R_{HBM}}{W \times D} \quad (2)$$

ROBUSTNESS ANALYSIS AND CHARACTERIZATIONS OF POLYSILICON-ASSISTED SCRS

A four-terminal device is presented in Fig. 6a, where FDSCR is separated into two parts. Poly\_Anode and Poly\_Cathode are two terminals of polysilicon part, with Sub\_Anode and Sub\_Cathode being the substrate silicon part. Results of substrate silicon part's and FDSCR's TLP I-V characteristics are presented in Fig. 6b, and polysilicon part's and FDSCR's characteristics in Fig. 6c. The polysilicon part of FDSCR actually is not completely triggered in the ESD event, considering the 36V trigger voltage shown (Fig. 6c). and the FDSCR's  $I_{t2}$  exceeds the sum of substrate silicon part's  $I_{t2}$  and polysilicon part's  $I_{t2}$ . In other words, the robustness performance of polysilicon-assisted SCR exceeds the sum of polysilicon part's robustness and substrate part's. The explanation is that the polysilicon part covered above the substrate silicon part induces a high electric field, which can reach the substrate part surface to form a high-conductance carriers layer in ESD event. The temporary high-conductance will improve the bypassing situation of polysilicon-assisted SCRs remarkably.





**Fig. 6 Analysis of FDSCR's robustness**

a) Four-terminal device b) Robustness of FDSCR and substrate silicon part c) Robustness of FDSCR and polysilicon part

Relation between dimension of FDSCRs (RDSCRs) and TLP characteristics is given in Table 3. Trigger voltages of FDSCR and RDSCR are quite the same, and not sensitive to the length "L". This is because triggering of RDSCR and RDSCR is fulfilled by substrate silicon part, and all the substrate SCR's are just the same. Holding voltages of RDSCR are higher than FDSCR by about 1 V. Larger lengths of "L" will induce larger values of holding voltages. In practice, larger holding voltages provide better immunities against latch up (Tremouilles, Bafleur et al., 2004; Ker and Hsu, 2006). Therefore, connection ways of polysilicon part and different lengths of "L" can be utilized to adjust to various operation circuits without inducing latch up damage. Finally, measurements show that larger intrinsic polysilicon's lengths will induce higher second breakdown currents ( $I_{I2}$ ). This is because larger values of polysilicon's lengths ("L") mean larger area of substrate silicon part in polysilicon-assisted SCR's influenced by high electric field in ESD event. And, the induced electric field plays a critical role in improving the robustness performance in the polysilicon-assisted SCR's in ESD protection application.

**Table 3 Characterizations of FDSCRs and RDSCRs**

Devices	L ( $\mu\text{m}$ )	$V_{t1}$ (V)	$V_h$ (V)	$I_{I2}$ (V)
FDSCR1	2.5	11.63	3.51	4.22
FDSCR2	5.9	11.69	3.63	4.68
RDSCR1	1.0	11.57	4.45	3.26
RDSCR2	2.5	11.62	4.53	4.34
RDSCR3	5.9	11.69	4.62	4.55

## CONCLUSION

Two polysilicon-assisted SCR's have been designed, fabricated and characterized. Measurement results show that given the same layout areas, robustness performance of polysilicon-assisted SCR's can be improved to the 3 times of conventional MLSCR's, and one-finger such polysilicon-assisted SCR's, which occupy only  $947\mu\text{m}^2$  layout area, can undergo 7-kV HBM ESD stress. Results further demonstrate that the S-type current-voltage (I-V) characteristics of polysilicon-assisted SCR's are adjustable to different operating conditions by changing the device dimensions.

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