BGA Package Integration of Electrical, Optical, and Capacitive Interconnects

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Abstract:
We present a novel optically-enabled ball grid array (OBGA) package that integrates conventional electrical I/O, proximity communication (PxC), and optical communication in one industry-compatible BGA package for the first time. The key enabling technologies for such a packaging solution, including the precision alignment needed to combine multiple CMOS chips and compact opto-electronic (OE) subassemblies, are detailed here. We designed and fabricated a 45 mm x 45 mm x 5.2 mm organic cavity-down BGA package with up to 600 solder balls for electrical I/O. Its cavity holds three CMOS chips, with PxC interfaces and optical driver/receiver circuits, as well as two multi-channel optical subassemblies with standard optical fiber connections. We report preliminary testing results.

Introduction

Overall computer system performance is increasingly throttled by limited off-chip communication bandwidth. To combat this, designers are pushing the capabilities of high-speed electronic links and off-chip optics, and researching new chip-to-chip communication technologies, such as capacitive “proximity” coupling [1].

Recent work in proximity communication (PxC) shows significant power, latency, and area savings over traditional solder, but only for chips within a module placed in very close physical proximity to one another [2]. In contrast, electrical links are well-suited to medium-range communication, such as between chips on a board; and optical links efficiently transmit data over long distances, from backplanes to wide-area networks. Systems that combine all three technologies can benefit from using the most efficient communication method for different data streams.

Prior work focused on integrating all three types of communication interfaces on a single CMOS chip routing data at multi-Gb/s rates [3,4]. In that system, a CMOS chip, optical detectors, and vertical cavity surface emitting lasers (VCSELs) were all bonded chip-on-board-style to a printed circuit board (PCB). Two such PCB assemblies placed with their CMOS chips face-to-face enabled sending data across each possible interface, such as optical into one chip, across the proximity communication gap, and then electrically out of the other chip. However, such a system would not be easily compatible with mainstream or low-cost packaging.

In this work we combine these disparate technologies into a single ball grid array (BGA) package solution suitable for integration into a standard PCB manufacturing flow. We integrate multiple chips with proximity communication interfaces into the same package, enabling very high bandwidth density and low power data transfers within the package. In addition to its regular high-speed electrical I/Os, optical I/Os are built directly onto the OBGA package with subassemblies that integrate fiber arrays, VCSELs, or photo detector arrays, enabling efficient communications between packages using optical networks. In the following context, the architecture of such an OBGA package will be presented and details of the Light Out Proximity In (LOPI) test chip, optical sub-assembly (OSA), package design and integration, and an innovative alignment technique with ball and etch-pits will be discussed. Experimental results from a prototype package will also be reported.

OBGA package architecture and design details

PxC enables seamless integration of many chips for enhanced performance within a package without suffering from inter-chip bandwidth bottlenecks. High performance electrical systems, however, require balanced communications throughout the whole interconnect hierarchy. Traditional electrical I/O through the package is already the bottleneck for interconnects between modules [2]. Integrating optical I/O directly onto the package adds bandwidth orthogonal to
electrical I/O, and can alleviate this bandwidth bottleneck. Figure 1 shows the concept of an OBGA package that integrates three interconnect technologies into one package as a basic building block for systems with balanced interconnects. It is a 45 mm x 45 mm x 5.2 mm organic cavity-down BGA package with its cavity holding two electronic chips furnished with PxC interfaces and optical driver/receiver circuits. The optical I/O interface built into the BGA package has electrical access to the on-chip transmitter driver and receiver circuits on chip via wire bonding, and reaches the off-package optical interface via MT fiber ribbon connectors.

The OBGA package is designed based on the 90nm CMOS LOPI test chip as previously reported [3,4]. Fig. 2a shows the test chip’s floor plan. In addition to the PxC and optical I/O interfaces, the chip also has an electrical I/O interface for testing. Each interface is 4 channels wide. Three sets of “where” blocks, used for checking the alignment of the chips, surround the proximity communication channels. The electrical I/O uses differential current mode logic (CML), allowing us to simply AC-couple the CML input buffer to a pattern generator, and eliminate the difficulty of insuring a proper input common-mode. The CML output buffer circuits can drive 5 Gbps data off-chip.

The PxC interface contains transmitter plates and receiver plates for both data path and chip alignment. Data to/from the optical or electrical I/O interfaces can be steered from/to the PxC interface using scan chain control.

The optical circuits for the LOPI chip consist of a 4-channel, 5 Gbps per channel VCSEL driver (TX) and a 4-channel, 5 Gbps per channel optical receiver (RX). The optical TX, which converts a CML electrical signal into a current that can drive a VCSEL load at high speeds, can be configured by the user for optimization of various VCSEL and package configurations.

The three different I/O interfaces interconnect via a network of multiplexer (MUX) and de-multiplexer (DeMUX) circuits, allowing all pair-wise I/O configurations to be exercised. Fig. 2b shows the test chip functional block diagram. As indicated by the arrowed lines in the figure, data paths can be configured to loop back at the same I/O interface or between any two I/O interfaces by the on-chip MUX/DeMUXs. Transmission of data across all interfaces at rates faster than 2.5Gbps has been demonstrated with a 6-axis alignment station [3,4].

The electrical I/O is configured for operation with Differential Current Mode Logic (CML), which is a low power technology suitable for high-speed serial data transmission. The CML interface uses two wires for each data channel: one for the data signal and one for the common-mode signal.

The optical I/O is configured for operation with VCSELs (Vertical-Cavity Surface-Emitting Lasers). VCSELs are compact, low-cost, and efficient optical sources that are well-suited for high-speed data transmission. The optical I/O interface uses a parallel fiber ribbon connector to connect to the optical sub-assemblies.

The optical sub-assemblies are integrated into the OBGA package using a parallel optical sub-assembly technology. The sub-assembly consists of an array of optical elements (VCSELs or photodetectors) mounted on a ceramic substrate, with fibers bonded onto the substrate. The fibers are aligned to the optical elements using a 45° angle reflector, which couples light into or out of the sub-assembly.

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Figure 3 Reflex Photonics LightABLE™ parallel optical sub-assembly for optical I/O in OBGA package.

The optical interface to the OBGA package is enabled by Reflex Photonics LightABLE™ parallel optical sub-assembly technology. Figure 3 shows an OE device array mounted and wire-bonded onto a ceramic substrate. A fiber array in v-grooves with pitch matching the OE device array (VCSELs or photo detectors) is polished at a 45° angle. The polished fiber array is placed directly on top of the substrate with the end surface of the fibers aligned to the OE device apertures. The polished fiber end-surface serves as reflector for coupling of light from/to opto-electronic devices to/from fibers. This optical subassembly achieves a very compact 90° optical turn for surface normal OE devices, making it possible for its integration into regular BGA package.

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A heat sink plate machined for the OBGA package forms a housing for both the CMOS chips and OSAs, as depicted in Figure 4. A 0.5 mm thick chip locator plate is constructed.
from 0.01” electrical discharge machined (EDM) wire and epoxied into the package. This plate aligns and supports multiple chips to a tolerance of +/- 10 microns, allowing them to communicate through proximity communication.

Integrated into the sides of this BGA package are a pair of optical modules supporting direct optical fiber insertion and alignment, and also containing VCSELs and photodiodes. These modules can be either wire bonded or flip-chip bonded to the central CMOS chips for optical communication. Four-channel optical fiber ribbons attach to these modules using standard MT connectors. Finally, an organic substrate with standard BGA interface, and an opening in the center is attached to the heat sink plate to complete the cavity-down BGA package as shown in Figure 1. This substrate also routes eight power supplies, ranging from 1.1V to 3.3V, plus ground, as well as all the high-speed electrical traces with well-controlled impedances. The OBGA package supports in excess of 600 solder balls for connection to a printed circuit board.

Figure 5 shows the close view of the CMOS chips assembled in an OBGA package. To assemble the CMOS chips into the package, one PxC bridge chip (LOPI chip 1) is flip-chip bonded to a system chip first. This two-chip assembly can then be connected and aligned to an E-to-O chip with PxC interface (LOPI chip 2) with epoxy, and use a coarse proximity communication circuit that tolerates moderate in-plane misalignment before being placed into the package. Alternately, they can be placed into the cavity, guided by the coarse alignment provided by the chip locator plate to engage the inverted pyramidal etch pits of two chips and the sapphire balls. They are then pressed together with a spring pressure clip to lock the two chips into alignment through the etch pits and ball kinematical mechanism, as the conceptual cartoon shown in Figure 6. The CMOS chips are then bonded directly to the package for traditional electrical communication.

We fabricate the precision inverted pyramidal etch pits on silicon chip by micro-machining features in the silicon substrate with an anisotropic wet etch to create (111) facets that form an inter-planar angle of 54.7 degrees with the (100) surface of the silicon chip [5,6]. The pit opening is calculated and precisely controlled by lithography for achieving zero-gap between two chips using 400 µm diameter sapphire balls. The auto-centered mating of the ball in the inverse pyramidal etch pit establishes the precise relative position between two chips. In addition, the forming of the inverted pyramids is self-terminating and is defined by the wet etch process in silicon. The depth of the pit is defined solely by the pit opening. With uniform size precision balls, the gap between the two chips can also be accurately controlled and maintained in a range of less than 1 micron to over 100 microns. The higher precision of the etch pit and ball alignment technique enables use of much finer proximity communication circuits with reduced power and area.

Figure 6 Precision chip alignment concept using inversed pyramidal etch pits and sapphire balls.

Package prototype and preliminary results

A couple of OBGA packages, and a test mother board were fabricated for this demonstration. Figure 7 shows the top and bottom view of a OBGA package flip-chip bonded on the test board, with a close view of the OBGA cavity showing one integrated LOPI chip.

High speed data transmission is tested using this demonstration system. The input electrical data signal goes through the traces on the test board, BGA interface and traces on package, wire bonds to the LOPI chip, and finally into the CML input circuit. The data is then steered to the VCSEL driver on the LOPI chip to drive the lasers in the transmitter OSA. Optical output from the OBGA package is sent over 100 meters of fiber, and then looped back to the receiver OSA of the package through the MT fiber ribbon connectors of the OSAs. The data is converted back to the electrical domain by the receiver circuits on the chip, sent through the CML output on chip, OBGA package, the test board, and then finally to the output SMA terminals on the test board. Due to the parasitics and impedance mismatch from extra bonding wires, traces on the OSA ceramic substrate, the organic board of the package, and the test board, the loop back link is limited to 2.5 Gbps data rate, as shown by the “eye” diagram in Figure 8.
Given the small size of the LOPI chips, which is only $4 \times 6$ mm, it was very challenging to fabricate precision etch pits lithographically. Currently we are still working on an improved etch-pit process on small CMOS dies so that we could demonstrate the 3-chip OBGA package with working PxC interconnects between chips.

With a focus on prototyping, and due to limited channels on the LOPI chip, only two OSAs are designed into this demonstration OBGA package. With the Reflex compact OSA technology, more optical I/Os running at a higher data rate can be integrated into a common size BGA package, supporting potentially up to Terabits/s of optical I/O bandwidth [7].

Conclusions

We presented the OBGA package that can potentially integrate regular electrical I/O, PxC, and optical communications in one industry compatible BGA package. In addition to conventional electrical I/O bandwidth offered by normal BGA package, extra optical bandwidth potentially up to tera-bits per second can be provided by the package, enabling networking for systems that consist of multiple packages. Further more, a direct optical interface to the chip package eliminates the need for optical transceivers in and out of the "box," enabling lower cost systems.

The etch pits and balls alignment technique combines the two exacting natural shapes of a sapphire sphere and an inverted (111) pyramidal pit in (100) silicon, eliminating five of the six degrees of chip misalignment; the last degree, chip separation, can be precisely controlled by the sapphire ball size. This accomplishment enables multi-chip packages with 3D integration and interconnected by high performance PxC. The high-bandwidth, low-power, and low-area inter-chip proximity communication is ideal for chips normally co-located in a single module, such as processors and caches, or several processors in a "fat node" configuration. It also enables chip replacement, and solves known good die, issues for building highly functional chip packages such as are reported here.

In summary, the OBGA package offers a promising packaging solution for improved single package performance by integrating multi-CMOS-chip assembly in one package. High performance inter-chip communications are enabled by PxC with no need to escape the second level packaging. In addition, off-package communication bandwidth is enhanced with better reach by the optical I/Os built into the OBGA package. Systems employ many packages and many nodes can potentially benefit from this packaging solution for much more balanced interconnect hierarchy, yielding better performance at lower cost.
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References


