A Novel Design and Modeling Paradigm for Memristor-based Crossbar Circuits

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Abstract—Over 30 years ago Leon Chua proposed the existence of a new class of passive circuit elements, which he called memristors and memristive devices. The unique electrical characteristics associated with them, along with the advantages of crossbar structures, have the potential to revolutionize computing architectures. A well defined and effective memristor model for circuit design combined with a design paradigm based on well understood underlying logic design principles would certainly accelerate research on nanoscale circuits and systems. Towards this goal, we propose a memristor crossbar circuit design paradigm in which memristors are modeled using the quantum mechanical phenomenon of tunneling. We use this circuit model to design and simulate various logic circuit designs capable of universal computation. Finally, we develop and present a new design paradigm for memristor-based crossbar circuits.

Index Terms—Crossbar, digital logic design, memristor, quantum tunneling

I. INTRODUCTION

Memristor was originally proposed in 1971 by the nonlinear circuit theorist Leon Chua [1]. The memristor is a fourth class of electrical circuit element, joining the resistor, the capacitor, and the inductor and exhibits its unique properties primarily at the nanoscale [2], [3].

Currently, Hewlett Packard’s (HP) version of the Titanium Dioxide (TiO$ _2$) substrate memristor [3] is the most generally recognized memristor type. It is based on two thin-layer TiO$ _2$ films. The bottom layer acts as an insulator whereas the top film layer acts as a conductor via oxygen vacancies in the titanium dioxide (TiO$ _2$ changes its resistance in the presence of oxygen). Voltage increment moves the oxygen vacancies from the top layer towards the bottom layer, thus changing its resistance. As an ac voltage is applied to the terminals of the device, the I-V curve shows a pinched hysteresis loop that passes through the origin. Around the origin the device acts as a traditional resistor (linear region). Nevertheless, until nowadays there has been no direct connection between a model and the memristor physical properties, except for a simple physical model proposed by Strukov et al. [3]. An appropriate descriptive model will not only lead to a better understanding of its behavior, but will also result to a better exploitation of its unique properties.

To access the memristive properties, memristors are placed at the intersection of nanowires (crossbars) so that a charge can be passed through them [2]. Many proposed architectures for nanoscale electronics have focused on the crossbar architecture because of its fabrication simplicity and of the inherent redundancy which supports defect tolerance [3], [4], [5]. The crossbar architecture can be used to compute logic functions based on the placement of specific device switches at the wire junctions and on their state. Currently, known disadvantages of crossbar-based designs compared to CMOS technology are mainly due to the device choice used to implement the switches. Configurable nanoscale memristors in a crossbar [6], [7], [8], where memristors are simply used as two-state switches, would provide a more powerful foundation for nanoelectronic computation. It would also offer considerable flexibility to system architects and would enhance the toolkit of circuit designers.

In this paper we focus on the architectural perspectives that arise from crossbars with configurable memristors. Towards this goal we propose a novel CMOS-like [5] circuit design paradigm and support it with a proper memristor circuit model which is based on the effective tunneling distance modulation [9]. Finally, based on the proposed memristor model, we built a crossbar circuit simulator using the Java programming language [10], and used it to simulate the equivalent circuits of the universal digital logic gates set (NOT, NAND, NOR) as well as more complex circuits (AND-OR-INVERT function, Half Adder), which altogether make possible the design and implementation of any digital logic circuit.

II. APPLICATION POTENTIAL OF MEMRISTOR-BASED CIRCUITS

In this section, the potential of memristor-based crossbar circuits is discussed. A series of technical specifications regarding performance metrics found in the literature are summarized and presented. Such experimental information forms a ground basis for future establishment and practical use of emerging nanotechnologies, verifying their potentiality and also further motivating the study of new design paradigms and future applications.

In their work, Stan et al. [11] point out that molecular electronics have a lot of potential to enable electronic functionality to continue scaling beyond the end of CMOS. Specifically, in Table I of their work, potential moletronic circuit approaches are compared with predictions made in the ITRS [12] for the end of the CMOS roadmap, in terms of speed, power, and density. The table compares footprint,
energy/transient, delay, power density, and compute density, taking into account only high-performance CMOS. It can be seen that crossbar-based circuits show clear potential for superiority in area, as well as in energy consumption, but not yet in performance. Furthermore, as long as the cost of building CMOS chips continues to follow an exponential law with time, it is pointed out that it is reasonable to expect that molecular chips will be less expensive to build, since chemical self-assembly is used to build the devices, rather than many, very precise lithography steps.

Moreover, Jo et al. [13] investigate two terminal amorphous-Silicon (a-Si) based resistive switches. These devices are found to exhibit a number of desirable performance metrics in terms of speed (<50 ns programming time), and endurance (>10⁸ cycles), which make them suitable for high-performance memory and logic applications based on conventional or emerging hybrid nano/CMOS architectures. Kim et al. in [14] demonstrate a high-density, fully-operational hybrid crossbar/CMOS system which utilizes a memristor-based crossbar array. The structure of the studied device consists of an a-Si layer acting as the switching medium. A 50 nm half pitch was achieved through electron beam lithography and yielded an equivalent data storage density of 10 Gbits/cm² when storing one bit per memory cell. In addition, Lu et al. in [15] review the recent progress on the development of two terminal resistive devices and report on a number of promising performance metrics shown by devices based on solid state electrolytes like a-Si. Specifically, resistance switching speed of < 10 ns and endurance of > 10⁸ cycles are mentioned, whereas data retention of >10 years at 85 °C and nominal energy consumption per operation in the subpicojoule range have also been reported [16-19]. Some of the recent advances of binary metal–oxide resistive switching devices reported in the literature are summarized in Table 4 of [20].

Also, Ebong and Mazumder [21] analyze the feasibility of memristor memories and introduce an adaptive read, write, and erase method. The power metrics are compared to flash memory technology, and the memristor-based memory exhibits an energy per bit consumption about one tenth of that of flash when programming, comparable to flash when erasing, and about one fourth of flash when reading. The aforementioned results are summarized in Table I of [21]. Also, Eshraghian et al. in [22] provide a new approach towards the design and modeling of memristor-based content addressable memory (CAM). Emerging memory devices and technologies are discussed, and a range of performance parameters and salient features of characteristic emerging technologies for memories can be found in Table II of [22]. The memristor-based crossbar architecture is shown to be highly scalable [23] and promising for ultra-high density memories [24]. It is worth to mention that a memristor with minimum feature sizes of 10 and 3 nm yields 250 Gb/cm² and 2.5Tb/cm², respectively.

It is worth to mention that in 2010, almost two years after their first memristor announcement (their device comprised a 50 nm titanium dioxide film and exhibited ion mobility of 10⁻¹⁰ cm²/(Vs)), HP Labs also declared that they had practical memristors working at 1 ns (~1 GHz) switching times and 3 nm by 3 nm sizes, with an impressive electron/hole mobility of 1 m/s [25]. These statistics foreshow well for the future of the technology and memristors could easily rival the current sub-25 nm flash memory technology.

III. MEMRISTOR DEVICE MODELING

A. Related Work

The HP Laboratories group in their first memristor implementation announcement [3], along with experimental device examples, suggested a coupled variable-resistor model for memristors. Ever since, this model was improved by Jokic and Wolf [26], whereas several papers by HP [27], [28] report on further developments of resistance switching theory for TiO₂ devices. Di Ventra et al. [29] suggested a simple threshold-type model of memristive systems [30] and employed it in programmable analog circuits [31], [32]. Liu et al. [33] proposed a material-oriented methodology to control resistance switching behavior of oxide-based resistive switches, based on a unified physical model [34] where formation of conducting filaments (CFs) is due to the generation of new oxygen vacancies by ionizing oxygen ions from the lattice under voltage bias. Furthermore, approximated SPICE memristor models have been proposed and tested with promising simulation results [35]. However, little work has been done towards memristor modeling, whereas various implementation paradigms are continually being proposed combining nano/CMOS [7], reconfigurable architectures and memristors [36], [37], resulting in hybrid implementations [38], [39], that could have a profound effect on integrated circuit performance.

B. A Novel Memristor Circuit Model

We propose an alternative solution for modeling memristors, explaining the devices memristive behavior by investigating the occurrence of quantum tunneling [9]. The equivalent circuit of the proposed model is depicted in Fig. 1. It is a threshold-type switching model of a two-terminal voltage-controlled electrical device that exhibits memristive behavior [30], and it is described by the following expressions:

\[ I(t) = G(L,t)V_M(t) \]  \hspace{1cm} (1)

\[ L = f(V_M,t) \]  \hspace{1cm} (2)

*Fig. 1. Equivalent circuit of the coupled ohmic-tunneling variable-resistor model; L is the width of undoped dioxide layer (tunnel barrier width).*
Schiff [9], here as voltage-dependent tunneling transmission coefficient, denoted variable-resistor equivalent circuit of Fig. 1, where we consider an ohmic due to the applied voltage bias. The time derivative of the state variable in (2) is interpreted as the speed of movement of the barrier between the two layers, whereas the undoped layer is a pure insulator. The doped layer acts as a conductor, whereas the undoped layer is a pure insulator. There is therefore a significant difference between the actual values of their resistances, with $R_t \gg R$, which is the reason why our proposed model concentrates mainly on the $R_t$.

Tunneling resistance $R_t$ is expected to be proportional to the tunnel barrier width $L$, given the fact that the larger the barrier width, the higher the resulting resistance should be. Also, its value is anticipated to change according to the movement of the boundary between the two materials because of the transport of oxygen deficiencies under positive or negative sinusoidal voltage. Thus, any mathematical formulation for $R_t$ could include at least a fitting parameter which would bound the effect of the device’s varying geometry on the actual concentration of the oxygen vacancies in either of the sides (doped/undoped) of the TiO$_2$ film. Furthermore, according to Schiff [9], $R_t$ is inversely proportional to the product of the voltage-dependent tunneling transmission coefficient, denoted here as $T_0$, and the electron effective density of states, defined here as $N_{eff}$, whereas it is exponentially proportional to the tunnel barrier width $L$. Therefore, its particular mathematical formulation is:

$$R_t(V_{M\, t}) = \frac{1}{N_{eff}} \cdot e^{\frac{2V_{M\, t}}{T_0 V_a}}. \quad (3)$$

The voltage dependence of (3), due to the presence of the voltage-dependent parameters $T_0$ and $k$, can be translated into a corresponding variation of the tunnel barrier width $L$; therefore it can be passed to a new voltage-dependent parameter $L_{V_{M\, t}}$ with no significant error implication. In our model, we defined $R_t$ to be described by the following equation, whose graphical representation is demonstrated in Fig. 2(d):

$$R_t(L_{V_{M\, t}}) = f_0 \cdot e^{\frac{2V_{M\, t}}{L_{V_{M\, t}}}}. \quad (4)$$

Equation (4) gives the devices resistance (memristance) for a certain restricted range of the state variable $L$. All unknown material-specific and geometrical issues are contained into the model-fitting constant parameter $f_0$ whose value has been determined by comparison with experimental results [3]. The qualitative agreement of (3) and (4) verifies our assumption for the exponential dependence of the tunneling resistance on the tunnel barrier width.

In addition, the tunnel barrier width is expected to vary within a restricted valid range, based on the assumption that the switching rate of $L$ is small (fast) below (above) a threshold voltage $V_{th}$. A heuristic equation $L(V_{M\, t})$ that qualitatively gives the expected response of the tunnel barrier width as a function of time $t$ and applied voltage $V_{M\, t}$ is given below, whereas the corresponding graph is shown in Fig. 2(c):

$$L(V_{M\, t}) = L_0 \cdot \left(1 - \frac{m}{r(V_{M\, t})}\right). \quad (5)$$

$L_0$ is the maximum value that $L$ can attain. The term in parenthesis of (5), which contains a voltage-dependent function $r(V_{th\, t})$ and a fitting constant parameter $m$, determines the boundaries of the barrier width. The function $r(V_{th\, t})$ incorporates the assumption for the expected different switching rate of $L$ based on the applied voltage bias discussed above. Particularly, the time derivative of $r(V_{th\, t})$ is given by the following equation:

$$\dot{r}(V_{M\, t}) = \begin{cases} a \cdot \frac{V_{M\, t} + V_{th}}{c + V_{M\, t} + V_{th}}, & V_{M\, t} \in [-V_{th} - V_{th}] \\ b \cdot V_{M\, t} + V_{th}, & V_{M\, t} \in [-V_{th} + V_{th}] \\ c + V_{M\, t} - V_{th}, & V_{M\, t} \in [V_{th} + V_{th}] \end{cases}. \quad (6)$$

Equation (6) comprises one-parameter sigmoid functions for
the regions above \( V_{th} \) (first and last leg), whereas a linear relation of the applied voltage is used for the region below \( V_{th} \). \( a \), \( b \), and \( c \) are fitting constants that define the slope and the magnitude of \( (6) \), with \( a>b \) and \( 0<c<1 \). A different set of values for the parameters \( \{a, b, c, f_0, m\} \) defines a different set of boundaries for the tunnel barrier width in \( (5) \). The graphical representation of \( (6) \) is shown in Fig. 2(b), where the two sigmoid functions were also included separately to facilitate visual correspondence. It is obvious that in the region \( \{V_0, V_{th}\} \) the graph (black line) follows the green sigmoid graph, whereas in the region \( \{V_{th}, V_0\} \) follows the red graph. Equations \( (5) \) and \( (6) \) bound the fundamental switching dynamics in TiO\(_2\)-based memristive devices, correlating the tunnel barrier width \( L \) with the applied voltage \( V_{M} \).

**C. Verification of the Proposed Model**

Fig. 2(a) demonstrates a comparison of the normalized I-V hysteretic curves obtained from a memristor under ac voltage bias, between our model and two published device models [26], [29]. The results of our model exhibit the expected “bow tie” shape, and apparently correspond qualitatively to the other models’ simulation results, as well as to the experimental I-V curve shown in [3]. In order to illustrate the versatility of our model, we present in Fig. 3 the I-V and M-V (M-Memristance) characteristics as calculated by the presented here model and the model proposed by Joglekar and Wolf [26] This model is an extension of the linear ionic drift as described by HP [3], where a particular window function is incorporated to illustrate nonlinearities in ionic transport. In order to obtain a fairer comparison, where we use the same parameters for both models. In specific, we use an 8V peak-to-peak triangular voltage pulse of period \( T_1=2.6 \) s and \( T_2=5.5 \) s to simulate memristors with total width \( L_{0,1} = 3\) nm and \( L_{0,2} = 5\) nm, respectively. We consider a \( R_{off} / R_{on} \) ratio of ~10, a dopant mobility of \( 3\times10^{10} \) m\(^2\)/Vs and we set the exponent variable of the corresponding window function \( p=2 \) [26]. Fig. 3 summarizes the simulation results for both the first \((a, b)\) and the second \((c, d)\) memristor. In each simulation we set our model’s parameters \( \{a, b, c, f_0, m, |V_{th}|\} \) to the values \{1000, 50, 0.1, 86.49, 56.06, 1.7V\} and \{350, 20, 0.1, 2.67, 29.97, 1.5V\}, respectively. In both cases our model delivers satisfying quantitative results which coincide with the results from the published model. The small difference in the maximum observed currents is attributed to the slightly different moments when the maximum memristance is achieved, particularly shown in Fig. 3 b, d.

Moreover, Pickett et al. in [40] report on experimental results from the application of a dynamical testing protocol applied to a set of TiO\(_2\)-based memristive devices. Through analysis of the switching dynamics that arise from ionic motion in the devices, it is concluded that electronic conduction in these devices is dominated by an effective tunneling barrier width that varies with time under the applied voltage. Thus, the switching effect is primarily attributed to an effective tunneling distance modulation, which supports our initial assumptions. Therefore, although the switching behavior is definitely complex, it has been showed that it is well represented in our model. Compared to other published models, like the HP’s model [3], our proposed model provides intuition into these strongly nonlinear dynamical systems, comprising simple and well understood equations and avoiding the use of restrictive material-specific parameters [3], [40]. Different value-sets for all fitting parameters, namely \( \{a, b, c, f_0, m\} \), provide the capability of simulating TiO\(_2\)-based memristive devices with different physical structures and geometries. In addition, our model offers the option for different threshold voltages to be applied to the ON and OFF switching cases respectively, in order to simulate asymmetric dynamical behavior during each case. Although symmetric behavior is presented here as the default option, various tunneling distance change rates could be attributed to the interaction of the external applied field, the internal field of the concentrated vacancies, and the diffusion, all acting in the same or in the opposite directions according to the applied voltage bias [40].

**IV. CIRCUIT DESIGN PARADIGM**

**A. Implementation of the Universal Digital Logic Gates**

In this section we propose a novel design paradigm for circuits with memristors, which is based on well-known logic design principles for the CMOS Very Large Scale Integration (VLSI) technology. We present the implementation of the equivalent circuit of the universal digital logic gate set. According to CMOS VLSI design theory, for every logic function \( F(x) \) implementation there is a specific formation for the Field Effect Transistors (FETs) circuit. In particular, p-type FETs are located in the upper part of the design plane, implementing the \( F(x') \), whereas the n-type FETs are located in the lower part,
implementing the $F'(x)$, with the circuit output always taken from between these two parts. Fig. 4 depicts the above description and also shows that appropriately polarized memristors can be used to replace existing FETs, maintaining the well understood CMOS-like design methodology [5]. This equivalence is mostly based on the fact that each memristor is considered to be a two-state switch, allowing or preventing the current flow in a circuit branch. It should be mentioned that in every circuit design presented throughout this work, the memristor devices are deliberately shown as three-terminal devices to facilitate comparison with CMOS circuits. In fact, memristors are two-terminal devices and each input signal in the circuit is applied to the particular set of crossbar nanowires which form the junction where the specific memristor is located. Thus, during programming state, applying an input signal simultaneously to all the devices found in a horizontal circuit line corresponds to the application of an appropriate voltage (positive or negative) to the crossbar nanowires which will affect the internal state of the memristor devices. Moreover, we use forward polarized memristors (FPMs) in the n-MOS area and reversely polarized memristors (RPMs) in the p-MOS area. Also, for the input signals we use conventional notation; namely, we represent logic ‘1’ with positive voltage bias and logic ‘0’ with negative voltage bias on the memristor terminals. The RPMs, corresponding to p-type FETs, are initially found in the $R_{off}$ state. Thus a negative sinusoidal voltage changes its state from $R_{off}$ to $R_{on}$ whereas a positive sinusoidal voltage either restores its state from $R_{on}$ to $R_{off}$ or lets it unchanged in $R_{off}$. On the contrary, the FPMs which correspond to n-type FETs, are initially found in the $R_{on}$ state. So, a negative sinusoidal voltage changes its state from $R_{on}$ to $R_{off}$, though a positive sinusoidal voltage either restores its state from $R_{off}$ to $R_{on}$ or lets it unchanged in $R_{on}$ correspondingly.

For every logic function, the final circuit consists of an equivalent ohmic resistance for the upper and another one for the lower part of the CMOS-like implementation respectively. Therefore the output voltage $V_{out}$ is always a fraction of the $V_{dd}$ (voltage divider), with voltage values close to $V_{dd}$ corresponding to logic ‘1’ and values close to zero ($G_{nd}$) corresponding to logic ‘0’. Fig. 5 demonstrates the actual circuit implementation of the universal digital logic gates with memristors, whose functionality we explain taking for example the INVERTER (NOT gate). At its initial state, before any applied input, it is $V_{out} = V_{dd} R_{on}/(R_{on} + R_{off}) \ll V_{dd}$. After positive sinusoidal input (logic ‘1’) the memristor’s previous state is changed, so we have $V_{out} = V_{dd} R_{off} (R_{on} + R_{off}) \approx V_{dd}$. Afterwards, every time a positive sinusoidal input is applied to the gate following the application of a negative one, the memristor’s state is restored to their initial state. Consequently, $V_{out}$ changes as expected for any input variation. Likewise, the proposed paradigm works correctly for the rest of the universal digital logic gates, making the design of every digital logic circuit possible.

B. Crossbar circuit simulator

In order to effectively simulate circuits with memristors on crossbar architectures [4], [5], we built a crossbar circuit simulator which utilizes the memristor device model proposed earlier in this work, using the Java programming language [10]. The simulator has been properly constructed in order to facilitate the circuit design following the proposed design paradigm, which is based on the CMOS VLSI theory. Snider et al. in [5] presented an approach to building nanoscale computing elements on mosaics of crossbars of configurable FETs and switches, which comprise a set of complementary arrays, i.e. pairs of nFET and pFET arrays supporting a CMOS-like design methodology. Inspired from their particular work and their concept of a fundamental crossbar-based building block, we adopted the basic geometrical features of the proposed logic block, which we then extensively transformed, proposing here our approach to building nanoscale compute fabrics out of configurable memristor switches. Particularly, we maintained the sharp geometry of the array-based architecture and considered appropriately polarized memristor devices to replace nFETs and pFETs.

More specifically, our simulator incorporates a practical user friendly interface, which comprises a basic logic block (LB) that facilitates the creation of logic with the use of memristor arrays, shown in Fig. 6. The horizontal and vertical lines
represents nanowires, with the horizontal lines in one plane and the vertical wires in another. The nanowires are divided into different quadrants of adjustable dimensions, each quadrant possessing different electrical properties due to the nature of the nanowire types in the quadrant and the chemical properties of the interlayer used in that region. The dark gray rectangles at the top represent structures that supply power and ground to the array. The small circles represent connections between the structures in the two different planes. The leftmost vertical wires are electrically connected to the \( V_{dd} \) power supply whereas the rightmost vertical wires are electrically connected to the ground. The quadrants at the bottom of the LB represent configurable routing switches; i.e. each junction is normally open, but can be electrically configured to be closed (a low impedance path). In the pink quadrant each junction can be configured to be an RPM, with the configuration input implemented with the horizontal wire and the poles of the device implemented with the vertical wire. In the same way, each of the blue quadrant junctions can be configured to be an FPM.

Every logic function can be implemented in a straightforward manner by decomposing it into two sets of minterms (one set for the RPMs and another for the FPMs), and by selective configuration of junctions in each of the quadrants. For sum-of-products function representations, each product term is implemented with a single vertical chain of memristors and the final sum is created by wired-ORing the existing products. A particular input signal may be brought in on any of the horizontal nanowires in the top main two quadrants and it applies to all of the configured memristors found in the same horizontal line. Correspondingly, an output signal may be driven out on any of the horizontal nanowires in the bottom quadrants, on either side of the array, limited only by the ability to allocate junctions within the array to implement the computation function.

![Fig. 6. Basic logic block of the crossbar simulator for circuits with memristors. It comprises two horizontal metal wires for power supply \( (V_{dd} \) and \( G_{ns} \), \( p \) (\( q \)) horizontal metal wires for inputs (outputs), and \( n=n_1+n_2 \) vertical nanowires. On the right, the most compact implementation for the set of universal digital logic gates is presented, where yellow dots denote currently configured memristors and routing switches.](image)

![Fig. 7. Output response of a NAND (middle graph) and a NOR (lower graph) digital logic gate implemented with memristors, for all possible input variations (upper graph) of signals \( A \) (red) and \( B \) (green), with \( V_{dd}=2V \).](image)

### C. Simulation of memristor-based crossbar circuits

In this section we demonstrate the results of the simulations conducted using our simulator environment, which utilizes the coupled ohmic-tunneling variable-resistor circuit model for memristors described earlier in Section III. We have successfully simulated the universal digital logic gates, as well as a half adder (HA) and an AND-OR-INVERT function implementation, which are powerful enough to implement universal computation. In our simulations we defined the value margin of \( L \) between 1 and 4 nm, and also used a 4V ac voltage amplitude, getting a satisfactory \( R_{on}/R_{off} \) ratio of approximately two orders of magnitude. All differential equations are numerically solved using a 4th order Runge-Kutta integration method, as it is implemented in [10].

Fig. 7 shows the output response of a NAND and a NOR logic gate for the corresponding input signals, both implemented with memristors under the CMOS-like design paradigm proposed earlier in Section IV. All possible input combinations are presented, starting with the pair \((A,B)=(0,0)\) and finishing with the same signal values. This is done on purpose in order to demonstrate that the circuit always returns to its initial state. The output voltages should be considered after an input signal completes its transition; i.e. in the deliberately left wide time gap between consecutive input signal variations.

Fig. 8 shows the LB configuration and the circuit design diagram of a HA, under the proposed design paradigm. On the LB figure, red color is used to distinguish the circuit part which corresponds to the Carry and green for the part of the Sum circuit respectively, with the inverted signals driven from the outside. Also, the output response for Sum and Carry, which proves the correct functionality of the circuit, is also presented. The simulation begins with the combination \((A,B)=(0,0)\) and finishes also with the same signal values. This time attention should be paid to the output graph after each inverted signal completes its transition. Furthermore, Fig. 9 demonstrates the circuit diagram for the implementation of an
AND-OR-INVERT function, namely \( F=(AB+CD)^\prime \), along with the output response for all of the sixteen different input signal combinations. The output graph is successfully confirmed by the function’s truth table, also given in Fig. 9.

### D. Performance evaluation of memristor-based circuits

Nanowire crossbar is considered one of the most promising circuit solutions for nanoelectronics having many favorable properties, including its periodic geometry and the very compact definition of devices and interconnects, facilitating large scale fabrication and ultra high device density. We next analyze how logic circuits implemented in memristor-based crossbars will perform especially in comparison with MOSFET logic circuits. Evaluation is done with three basic circuit properties, namely area, operation frequency (delay) and energy. Ultra high cross-point density is the major advantage of nanowire crossbar. The generic memristor-based crossbar considered here consists of two horizontal metal wires for power supply (\( V_{dd} \) and \( G_{nd} \)), \( p \) (\( q \)) horizontal metal wires for inputs (outputs), and \( n=n_1+n_2 \) vertical nanowires, where \( n_1 \) and \( n_2 \) is the number of nanowires in each of the orthogonal arrays where RPMs and FPMs are located. If \( f \) is the half pitch (minimum feature size) of the process technology, the area of a memristor at a cross-point is estimated as small as \( 4f^2 \) [41]. Considering all pitches equal for simplicity reasons, i.e. horizontal power line pitch, input/output line pitch and nanowire pitch, the area of any circuit is calculated as follows:

\[
\text{Area} (p, q, n_1, n_2) = (p + q + 1) \cdot (n_1 + n_2) \cdot 4 f^2. \tag{7}
\]

For example, the set of parameters \( \{p, q, n_1, n_2\} \) for the crossbar implementation of NAND and NOR universal logic gates shown in Fig. 6 is \( \{2, 1, 2, 1\} \) and \( \{2, 1, 1, 2\} \), respectively. Thus, the corresponding area for both of the logic gates is \( 48f^2 \), which is only the 16\% of a four-transistor MOSFET gate’s area of \( 300f^2 \) [42].

In order to estimate the operating frequency of the presented here memristor-based circuits, we need the time required to change the state of a memristor (write) from 0 to 1 and 1 to 0, which is directly connected to a voltage source. This time \( (T_w) \) was previously derived in [43] and is given by the following equation:

\[
T_w = \frac{L_0^2 \beta}{2 \mu_v V_m}. \tag{8}
\]

\( \beta \) is the achieved resistance ratio of \( R_{off}/R_{on}, L_0 \) is the thickness of a memristor, \( V_m \) is the magnitude of the applied voltage and \( \mu_v \) is the mobility of oxygen vacancy dopants. According to this equation, the write time of a memristor is a function of physical parameters of the device and increases with increase in \( L_0 \) and \( \beta \) and decreases with increase in the applied voltage. The time required to read the state of a single memristor is not needed for our logic circuits. Introducing in (8) the set of parameters’ values considered in our simulations for the presented circuits, utilizing a dopant mobility value also used in [22], namely the set \( \{L_0, \beta, V_m, \mu_v\} = \{5nm, 100, 4V, 3\times10^{-8} m^2/(Vs)\} \), results in a memristor access time \( T_w \) of 10.4ns. Such a delay is relevant with measured values for switching speed reported in the literature, although higher (lower) dopant mobility can lead to lower (higher) delays respectively. The instantaneous current of the memristor \( i(t) \) while writing one or zero depends on the memristor resistance at that instance of
time ($R_t$) and on the applied voltage ($V_m$). The energy dissipated during access time in each cross-point device can therefore be calculated as:

$$E_w = \int_0^{t_r} V_m i(t) \, dt. \quad (9)$$

According to data reported in recent literature listed earlier in section II, measured values for switching speed and energy dissipation per operation for memristors can reach <10ns and <0.6J, respectively. Thus, in terms of area and energy consumption, memristor-based circuits are very competitive, delivering also comparable speed with conventional MOSFET-based circuits.

V. CONCLUSION

This paper underlines the architectural perspectives that arise from crossbars of configurable memristors. More specifically, a novel circuit model for memristors, which explains the devices memristive behavior by investigating the occurrence of quantum tunneling, and a CMOS-like circuit design paradigm for circuits with memristors were proposed. We proved the fine application of both by demonstrating the results of various simulations conducted with a properly built crossbar circuit simulator. This work applies well to nowadays technology trends on nanoscale circuits and systems and motivates for further experimental investigation on issues concerning power consumption, operating speed and circuit reliability. Detailed study related to application of this work to memory circuits will be also part of our future investigation.

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REFERENCES


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