Toward a Low Cost and Single Chip Holter: SoC-Holter

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Abstract—In spite of the rapid development of medicine, cardiovascular diseases are still the number one killer in the world. In France every year more than 50,000 people die suddenly due to cardiac arrhythmias. Identification of high risk sudden death patient is still a challenge. To detect the cardiac arrhythmias, currently Holter is generally used to record 1~3 leads ECG (electrocardiogram) signals during 24h to 72h. However the use of Holter is limited among the population due to its form factor (not user-friendly) and cost. In this paper, we propose an integrated single chip wearable Holter named SoC-Holter, which enables to record 1~4 leads ECG. This single chip SoC-Holter is relied on adequation algorithm architecture design methodology. To minimize energy consumption, CMOS technology (0.35µm) is used to prototype the first implementation and test. The SoC-Holter has the following functions: signal conditioner and preamplifier, amplifier and filters, analog to digital converter, and Nano-controller. The low-pass filter is composed of current division, degeneration and common-mode feedback circuits added to fulfill the required performance. The analog circuits are implemented, tested and validated. The digital bloc is simulated, implemented and tested. It seems that an integrated, low cost, and user-friendly single chip Holter is feasible. Consequently large number of high risk populations such as heavy smoker and obese may be monitored. This SoC-Holter consumes less than 10mW while the device is operating.

Index Terms—cardiac arrhythmias, Nano-controller, CMOS, ECG, Holter, SoC-Holter

I. INTRODUCTION

In spite of the rapid development of medicine, cardiovascular diseases are still the number one killer in the world. Most cardiac arrests occur following myocardial infarction and 90% of them are due essentially to cardiac arrhythmias. 20% of sudden cardiac arrhythmias deaths are caused by heart block or pause (bradycardia) and 80% are caused by ventricular fibrillation (VF), frequently initiated by ventricular tachycardia (VT). Cardiovascular disease is not one condition. It is not possible to provide all symptoms, because each condition has many different symptoms. There are many symptoms affecting the heart that include chest pain or discomfort, shortness of breath, or faster heartbeats etc. If these abnormal symptoms can be early detected and diagnosed, time is saved to prevent the occurrence of heart attack or to provide an efficient treatment in time. Reducing the number of disabilities and deaths caused by heart attack, it is necessary to have an effective method for early detection and early treatment.

In fact, if the cardiac arrhythmias is detect early, the implantable cardioverter-defibrillator (ICD) may be used to prevent sudden cardiac death due to ventricular fibrillation. However, to implant an ICD a major surgery is need and it is not free of potential complication. Moreover, the implantation of ICD is expensive. Why it
is important to develop a new technique, which enables to detect efficiently and early the cardiac arrhythmias. Currently to detect cardiac arrhythmias, generally a Holter monitor is a portable device used to record 1–3 leads ECG signal during 24h to 72h. However it seems that the current available preventive techniques are not efficient due to its cost. When the patient is equipped with a Holter he fills not easy due to its form factor.

Therefore, it is necessary to develop a new cardiac monitoring device (SoC-Holter), which enables to identify precisely the high risk sudden death patients. To achieve this objective, the new device should be user-friendly, cost-effective, risk-free and easy to use in everyday life for a large number of populations.

This paper gives an overview of our previous work on cardiac monitoring system, and specifies some interesting technical details. In section 2 the state-of-the-art of cardiac monitoring devices is presented. Section 3 resumes our previous work, and obtained results on cardiac arrhythmias tele-assistance and monitoring platform. Section 4 details the techniques adopted for the implementation of SoC-Holter functions. In section 5, an assessment of the SoC-Holter prototype and the ongoing work are presented.

II. STATE OF THE ART

Nowadays, to detect cardiac arrhythmias, three simple and non-invasive cardiac surveillance techniques based on ECG monitoring are available: Holter, loop recorder and RTEST. Currently Holter is the most popular, and it enables to record 1–3 leads ECG signals during 24h to 72h. With Holter monitoring system, the recorded ECG signals are processed by specific software (off-line) and then a diagnostic report will be created to help cardiologists for further analysis. However, Holter is proved largely insufficient for a long-term prediction because the critical cardiac arrhythmias do not necessarily occur during these 72h [1] and [2].

A loop recorder is a portable device enables to record ECG signals continuously for an extended period of time. Unlike Holter, all the ECG signal are not recorded, only a sequence of ECG signal will be saved when the patient notes an arrhythmia symptom. The information may be sent to the cardiologist or saved locally. Loop recorder is implantable for long monitoring period (18 months) [3].

The RTEST is a one lead ECG monitoring device. Like loop recorder, the patient can manually record a sequence of ECG signals, when he notes an arrhythmia symptom. Furthermore, RTEST may be configured to record automatically cardiac arrhythmia up to 8 days. The recorded ECG signals would be sent through modem/Email communication to a remote server to be analyzed and diagnosed either by a cardiac technician or by a cardiologist [2].

Note that loop recorder and RTEST enable to monitor an extended period of time and the patient can manually save the ECG signals, but the cardiac arrhythmias are often asymptomatic.

III. SYSTEM ARCHITECTURE

In fact, in our previous work, we have implemented a platform dedicated to real-time cardiac arrhythmias tele-assistance and monitoring. The system is composed of 4 main configurable elements: wireless ECG sensor (WES), local access unit, remote centre server and remote surveillance terminal [2], [4] and [5]. The platform is used to evaluate 30 patients of the cardiology department at the CHRU of Gabriel Montpied’s hospital (Clermont-Ferrand, France). Each patient is equipped with the WES and with the HP’s telemetry device. In real-time our platform provides the same results as the HP’s telemetry device ones. Note that the quality of the ECG signal of our platform is better than the HP’s telemetry device because the sample frequency of the WES is higher (1 KHz) [2]. Moreover, note that the WES electrical features respond to the last AHA (American Heart Association) recommendations [6].

There are several application modes and operation modes of the WES. It is configured merely as an ECG surveillance equipment to monitor the heart status of patient. The recorded ECG signals are stored into the
internal memory on WES. The patients must periodically go to the hospital to submit the ECG records. The cardiologists analyze and diagnose these ECG signals on WES, which works like the Holter [7]. In another application mode, the patients and the cardiologists are in the local area and share the local network infrastructure. The ECG signals acquired by the WES will be compressed and sent via local wireless mediums. Because the diagnostic procedure is not implemented on WES but on local or remote server, according to reduce the cost of WES. In this mode, our system works as a telemetry arrhythmia recording system, as shown in the Agilent telemetry system [8]. If the patient is far from the cardiologist, the connection is established via the existent network infrastructure, for example the wide wireless technology.

The telemedicine system offers three operation modes over the different application mode but can be changed by the cardiologist in order to evaluate the patient’s heart status. The first also the highest alarm mode provides the real-time continuous ECG signals for on-line diagnosing by the cardiologist. This operation mode has some limitations due to the restricted network bandwidth, system resources and human resources. In the second operation mode, the system stores and send only a sequence of ECG signal, which consist of the two side data of cardiac arrhythmias events. This mode avoids generating huge data and network traffics caused. This operation mode is suitable for lower-risk heart disease population, who are needed to fewer data for monitoring the presence of heart disease. In the third mode, a short emergency message is sent to the cardiologist including the symptom of the cardiac arrhythmia.

Thanks to our previous work and experiment results, we think that one of the key issues to prevent sudden death is to develop an effective device such as SoC-Holter for early detection and early treatment, which also decreases power consumption. Integrated Nano-controller means that SoC-Holter allows signal processing in chip and increases performance of system. The entire system also becomes more flexible, the ECG signal can be transmitter immediately for real-time application or saved in memory for off-line mode. The latter mode avoids wasting energy on sending large volume of raw data, suitable for the patients without serious illness. The technical features of SoC-Holter are:

(i) Gain: 500; (ii) CMMR(min): 110dB; (iii) 3 dB Bandwidth: 140Hz; (iv) Programmable sampling frequency superior to 500Hz; (v) Analogue to digital converter: 12 bits; (vi) Leakage current: 10µA.

The following sections present the different functional blocks of SoC-Holter:

A. Signal conditioner and pre-amplifier

The output of ECG lead is noisy and the amplitude of chess lead V5 derivation ECG signal is about 1mV. In fact to be able to extract the ECG signal from noise, it is necessary to implement an appropriate signal conditioner and preamplifier stage having at least 110dB of CMRR.

This block is composed of a preamplifier having the gain value of 500. The preamplifier contains three identical amplifiers with different negative feedback factor. The circuit diagram is shown in Fig. 3.

\[
Gain = \frac{V_{out}}{V_{in}} = -\frac{R_F}{R_S} \tag{1}
\]

Where \( R_F \) is the feedback resistor and \( R_S \) is the source resistor, the value of feedback loop is settled by the ratio of two resistors. The resistor of feedback \( R_S \) is set 500 KΩ, so the gain can be adjusted by changing the source resistor \( R_2 \) and \( R_3 \) according to the upper formula.

The first amplifier offers the gain of 55 by setting \( R_2 \) to 9 KΩ, and the last two amplifiers supply the same gain of 3 by setting \( R_3 \) to 166 KΩ, then the final gain is obtained up to 500, achieving a 110dB CMRR with low power supply (±2.5V, 5V peak to peak).
Fig. 4 shows the schematic of a differential input stage with current mirror load, followed by a common emitter configuration with active load that provides most of the voltage gain. Furthermore, the rail to rail configuration makes the input stage gain independent of the signal amplitude and achieves a high CMRR. This topology is chosen in Fig. 4 because it provides a high voltage gain meeting the design requirements. In addition, this topology provides a good linearity due to the current mirror circuit connected. The resistive common mode feedback connecting to output stage prevents the amplifier operating point shifting with a full symmetrical design. The feedback loop consists of the resistor and the capacitor. The resistor allows the amplifier to be matched over a bandwidth because its input impedance is largely dependent on it.

The circuit achieves high gain and CMRR rail to rail operation with lower power consumption. Note that the useful input signal bandwidth is about 0.1Hz to 40Hz.

The upper plot in Fig. 5 shows a sinusoidal voltage waveform at a frequency of 20Hz, this is the input signal waveform. The amplitude of input signal is 4 mV. The lower let plot shows the waveform of amplified signal with the amplitude of 2V. The measured gain is about 500 to achieve our design requirements. Fig. 5 also shows the measured AC gain versus the sweep frequency range. The AC gain is adjustable with the increasing frequency. By keeping the voltage fixed, the relationship between the AC gain and the frequency is measured. The AC gain is at its maximum at the lower frequency band, and drops to a minimum at the end of the band. These results satisfy the requirement and ensure the input signal of the mixer from the amplifier to be not overloaded.

B. Low/high pass filter and amplifier

The recommendation cut-off frequency of band-pass filter for ECG signals is a 0.05 to 100Hz [4]. Classical bi-quad filter with passive RC components needs large die size. Numerous techniques have been developed in order to save die size in case of large time constant circuit such as switched capacitor and continuous time [8]. In this paper a band-pass filter built on a low-pass and a high-pass filter based on the OTA (Operational Transconductance Amplifier), as presented in Fig. 6. Differential design is chosen to improve the signal noise ratio as well as good voltage swing.

OTA is consisted of three parts as CDB (Current-Divider Block), degeneration block and Common Mode Feedback. The CDB is composed of 10 transistors in order to minimize the transconductance gain [10]. The transconductance of the amplifier is then divided by factor 10, $G_m = \frac{G_{m_0}}{\text{Factor}(10)}$ where $G_{m_0}$ is the original transconductance of the amplifier without CDB. $G_{m_0}$ is dependent on the size of transistor and the bias current. Thus it is necessary to properly select the ratio between width ($W$) and length ($L$) of transistors to maintain them in the saturation region with the bias current as low as possible and also to minimize die space.
The degeneration part increases linearity and reduces the transconductance of OTA. The final part, CMFB stabilizes the output [11]. The architecture of the low-pass filter is given in Fig. 7a, and the high-pass filter is given in Fig. 7b [12].

The cut off frequency of the filter is given by the formula: 

$$f_{\text{cutoff}} = \frac{G_m}{2C},$$

where $G_m$ is the transconductance of OTA, and $C$ is the value of the capacitor located between OTAs. Fig. 8 shows the voltage waveform of the signal passing through the filter and the final result. The plots obviously display signals through the filter with the voltage loss. From the AC response of the filtered signal, the same conclusion is obtained. The voltage gain declines sharply at the frequency beyond the area of 100Hz and decreases 3 dB at the frequency of 140 Hz.

**C. 12-Bits ADC**

The ECG frequency signal is low (<10Hz), and for a high resolution ECG signal the sampling frequency is 1KHz. Note that generally, the ECG signal is sampled at 250Hz. Thus, in our design we implement a single slope ADC, having the conversion time 40µs (sample frequency 125 KHz max), which is largely enough to sample the ECG signal at 1 KHz as shown in Fig. 9. The ADC is composed of 4 parts: T/H (track and hold), rampe generator, comparator and 12-bit serial register [13].

The rampe generator provides the linear voltage to the comparator, by means of two current generators made of two transistors (P and N MOS). These transistors are charged by the two capacitors with a constant current. Subsequently, this slope is compared with the front-end input signal.

The comparator consists of three blocks: input, amplifier and latch. The input part is a differential amplifier. The second block is a positive feedback amplifier and the last stage is latch which converts the output into a digital signal. The complete circuit of comparator is shown in Fig. 10.

Fig. 11 illustrates the transient analysis result of the ADC. The amplitude of the analog input signal of the ADC varies from 250 µV o 1 V.
D. Oscillator

The schematic of the high frequency oscillator is shown in Fig. 12. This oscillator uses a CMOS differential amplifier composing of transistors [14]. The current mirror circuit is used to provide the bias voltage of the transistor at VDD/2 to maximize the voltage swing and reduce the current needed for oscillation by half.

Fig. 13 shows a plot of AC response and output waveform of the oscillator. The measured zero to peak output voltage swing is 1.8v with a 3.5v supply. The oscillator is self biased for sustained oscillation at 2.46 GHz. From the output waveform of the oscillator, the startup process is clearly shown. When the transistors charged to the bias voltage, the oscillator begins to power up. A shorter time of this process increases loading and power consumption. Once the oscillation point is reached, the differential amplifier offers sufficient voltage gain and makes the oscillation amplitude stabilized. Faster amplitude growth time can be achieved at the expense of a higher current consumption. Finally, the transistors turn into the triode region and the oscillator reaches steady state.

E. Mixer

Our design requirement of mixer allows a frequency translation between a high RF frequency to 2.458GHz and a lower Intermediate Frequency (IF) to 88MHz. The topology of mixer has a differential interface as depicted in Fig. 15. The transistors in the mixer behave as switch and LO signal drives the gate of the transistors to start work.

Fig. 14 shows FFT of transient output in the simulation, which has to obtain the greatest power gain at 2.5GHz. The nearest spurious tone measurement appears at 5 GHz away from the center frequency. Within longer frequency range, the spurious tones are found at the points which are at integer multiples away from the center frequency. The nearest spurious tone is -40 dBc and the location being away from the center frequency makes the impression of the spurious tone on RF system minimal. In our design of system, the filter attenuates signals that are outside of the received bandwidth. Therefore, the spurious tones far beyond the bandwidth are attenuated substantially.

Fig. 16 shows the result of multiplying the RF and LO signals. A low frequency waveform is clearly visible. It can be seen as a replica of the RF signal translated to the IF frequency. This method provides a qualitative analysis of how the mixer operates, however it is not adequate to deduce the prediction. In addition, the mixer has additional losses due to square wave multiplication. In order to predict accurately the mixer’s performance, large signal simulation must be made.
The integrated circuit of SoC-Holter is shown in Fig. 17. The preamplifier with large gain consumes 5.2mW which contributes a large portion of the energy consumption. The filter consumes 680µW. The proposed ADC permits fully integration, with a power consumption of 2.3mW with including power of digital parts. And the total power consumption of the mixer with oscillator is 1.66mW. The total power consumption of SoC-Holter is about 9.84mW while the device is in fully working condition.

**Nano-controller**

Note that the existing low power microcontrollers such as MSP430x (16-bit RISC core) [9] and ATMega128 (8-bit RISC) [15], on one hand, they do not have enough on chip resource (e.g. Flash memory to record 4 leads ECG signal continuously during 48h; and on the other hand they have more peripheral devices (UART, PC, USB) than need. Thus, to minimize die size and energy consumption, we implemented a simple 8-bit RISC dedicated to sample the ECG signal and save directly into the flash memory or to process and send it through ZigBee wireless access medium which is connected to an UART or to record the sample data into a Flash memory through SPI interface. Note that, the recorded ECG signal may be read by dedicated software (offline) through SPI interface.

To minimize energy consumption a Nano-controller based on 8-bit RISC processor concept is implemented. The Nano-controller key features are (Fig. 18):  
- Firmware dedicated to RS232 connection with commercial wireless access medium such as Bluetooth and ZigBee (IEEE802.15.4),  
- Firmware dedicated to SPI interface for flash memory.

**V. CONCLUSION**

In this paper a SoC-Holter dedicated to monitor cardiac arrhythmia is presented, and particularly the wearable single chip ECG sensor is investigated.

A prototype based on commercial off-the-shelf components are implemented and tested but it form factor and energy consumption are still important for long time wearable ECG monitoring. Thus in this paper, we show that it is possible to implement a single chip wearable Holter: SoC-Holter.

The analog circuits such as signal conditioner and preamplifier, band-pass filter and ADC are implemented as shown in Fig. 17 and tested. The obtained results corresponded to expect performance. The Nano-controller is simulated and validated and we are starting to implement a single chip SoC-Holter which enables to record 1~4 leads ECG. Note that the current SoC-Holter may be use also to implement a wireless ECG node by connecting a ZigBee module through RS232 interface. Moreover to increase the lifetime of SoC-Holter, we will develop an embedded firmware within the Nano-controller which enables to classify normal and abnormal ECG signals.

Fig. 19 presents the acquisition of data issues from the output of the ADC, and the digital data is sent to the RS232 interface in binary format (2 characters of 8-bit). Note that, with the dedicated Nano-controller only 6 Nano-instructions (8-bit) are necessary and the clock of the different blocks is activated only when need. Thus, the Nano-controller minimizes significantly the energy consumption of the SoC-Holter.
ECG signal. Consequently only the abnormal ECG signal will be recorded to be analyzed (offline). Finally we believe that with SoC-Holter a large number of high risk population may be user-friendly monitored to prevent efficiently sudden death.

REFERENCES


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