Data Acquisition System for the Angra Project

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Abstract

The design of a Data Acquisition System (DAQ) for the Angra Neutrino project is presented. The DAQ is divided in two main sub-systems - *neutrino* and *veto*. The neutrino sub-system receives as input pulses from the photomultiplier tubes that cover the active volume for the neutrino detection. The veto sub-sytem is responsible for processing the veto information generated by muons crossing platic scintillators covering the whole detector. Both sub-systems are custom electronics mainly based on VME standard. The electronics design uses off-the-shelf devices from worldwide semiconductor companies. A software framework for the DAQ is developed for Linux platforms by using standard scientific tools and languages like Root and C++. This note focuses on the descritpion of the neutrino DAQ architecture and its hardware implementation. Other notes will present the veto sub-system as well as the software implementation for both DAQ channels.

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1 Introduction

The Angra Neutrino experiment [1] is composed of two basic detectors: the central detector and the veto system. The former is expected to be a cubic volume filled with pure water, surrounded by 8-inches Photomultiplier Tubes (PMTs). Two main branches of the front-end electronics [2] are considered for the central detector. One branch delivers the analog signal from the anodes already shaped and amplified, while the second path provides a digital pulse obtained from leading-edge discriminators. Both signals feed the neutrino DAQ sub-suystem for data acquisition, digital processing and further transmission and storage. The neutrino DAQ is supposed to receive both the analog and the trigger pulse from the front-end electronics.

The veto system consists of plastic scintillators pads surrounding the central detector on the bottom and on the top lids of the volume. Signals from the scintillators are driven through optic fibers to 64-pixel photomultiplier units. The anode signals from these PMTs should feed fast pre-amplifiers followed by leading-edge discriminators. The discriminated pulses are logically combined by the veto electronics to create an event-discard flag, since a muon can potentially mimic a neutrino event. These muons comprise a natural background difficult to avoid, or even reduce, with any kind of shielding, due to the high energy of the particles.

In summary, the Data Acquisition System for the Angra Neutrino detector is responsible for all the processing stages from the output of the front-end electronics to permanent data storage of monitoring and physics events. An overview of the signal paths from the detectors to the DAQ is shown in Figure 1.

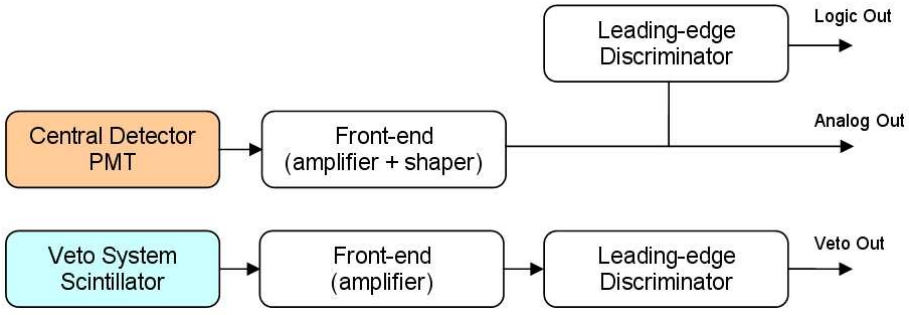

Figure 1: The signal path from the detectors to the Data acquisition System.

2 DAQ Architecture

The two DAQ subsystems - neutrino and veto - consist of custom electronics based on the VME64 standard, and dedicated software developed for Linux operating systems. As a first estimate, a single VME 6U crate (up to 21 modules) will contain all the neutrino DAQ electronics. On the other hand, even in the case of insuficient room in one crate, another crate may be added without any technical difficulty. A single-board computer installed in the crate will be connected through ethernet to a DAQ network, so that, any module in the crate can be accessed by allowed remote machines. In case of more than one crate operating in the DAQ framework, each crate will appear as a different IP machine in the DAQ network. A first conceptual view of the neutrino DAQ is shown in Figure 2. It should be noted that the veto system, in principle, only send flags to the neutrino DAQ concerning muon

events in the central detector. These flags may indicate a muon crossing the detector and the x and y coordinates in each scintillator plan. In the event of a veto, which means a muon crossing the central detector inside a pre-defined time window after a positron detection, information on that event will be packed and filled into buffers for further data readout. All the operations in the DAQ hardware will be controlled by a set of small applications, mainly in C language. In a hierarchical approach, all these applications will be running under the control of a high-level software framework being executed in the DAQ server of the experiment.

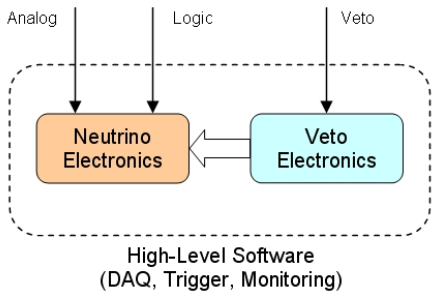

Figure 2: Conceptual view of the Data Acquisition System.

The High-Level Software (HLS) is the top framework for the management of all the elements in the data acquisition of the experiment. It is a fully object-oriented software based on C++ and Root [3]. The HLS has total access and control over the Neutrino and the Veto electronic modules through ethernet connection. The HLS should perform the following tasks:

- control the DAQ operation during either data taking or calibration runs
- online readout and display of physics and monitoring data
- execute high-level trigger algorithms to filter out ordinary-physics events
- control the data flow from the VME electronics to the permanent data storage system
- buildup and organization of physics and monitoring data in the data storage media

This is a first overview of the tasks foreseen for the HLS. Each item above will be carefully sub-divided and organized in functional blocks to a modular and complete hierarchical design. Other tasks can be assigned to the HLS during project development. Figure 3 illustrates a general overview of the Neutrino Angra DAQ, including each sub-system.

3 Neutrino channel

A block diagram of the neutrino DAQ channel is shown in Figure 4. This diagram illustrates only the main processing elements in the data flow for one channel, that is, one PMT in the central detector.

As already depicted in Figure 4, before the DAQ electronics, the PMT signals are first processed by a sensitive front-end electronics. The PMT current pulse is pre-amplified so that a voltage pulse is produced with a peak amplitude proportional to the charge deposited in the PMT. Amplification and filtering follows to expand the amplitude range and to shape the original pulse in such a way that it can be reasonably represented in the digital domain.

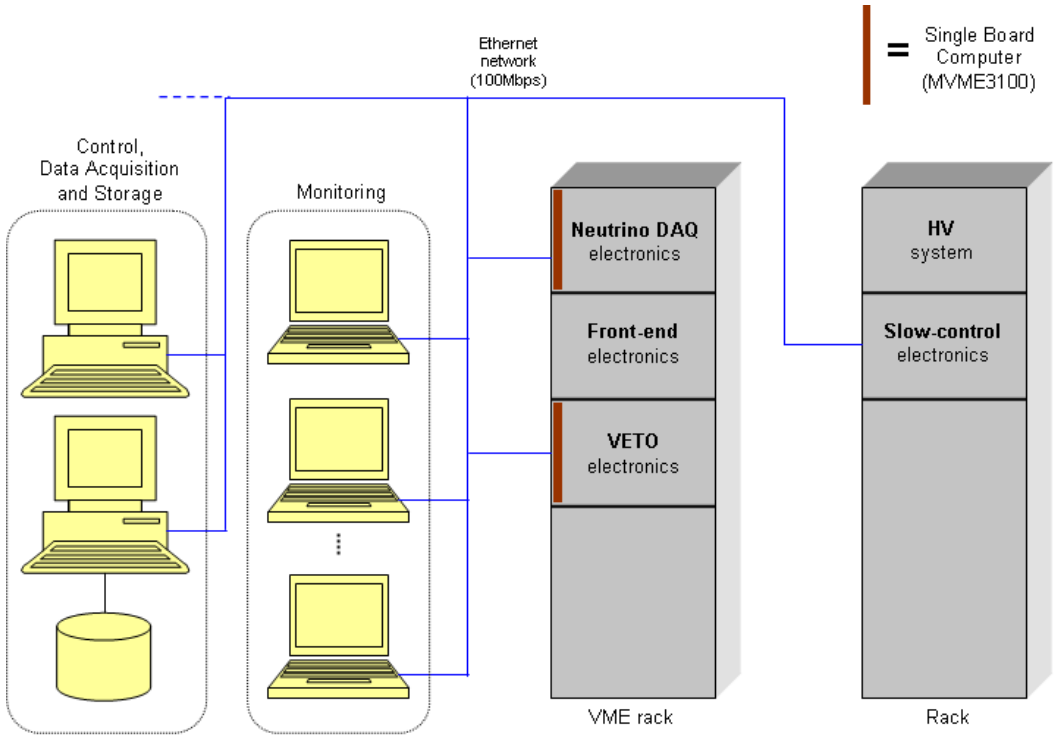

Figure 3: Overview of the Neutrino Angra DAQ.

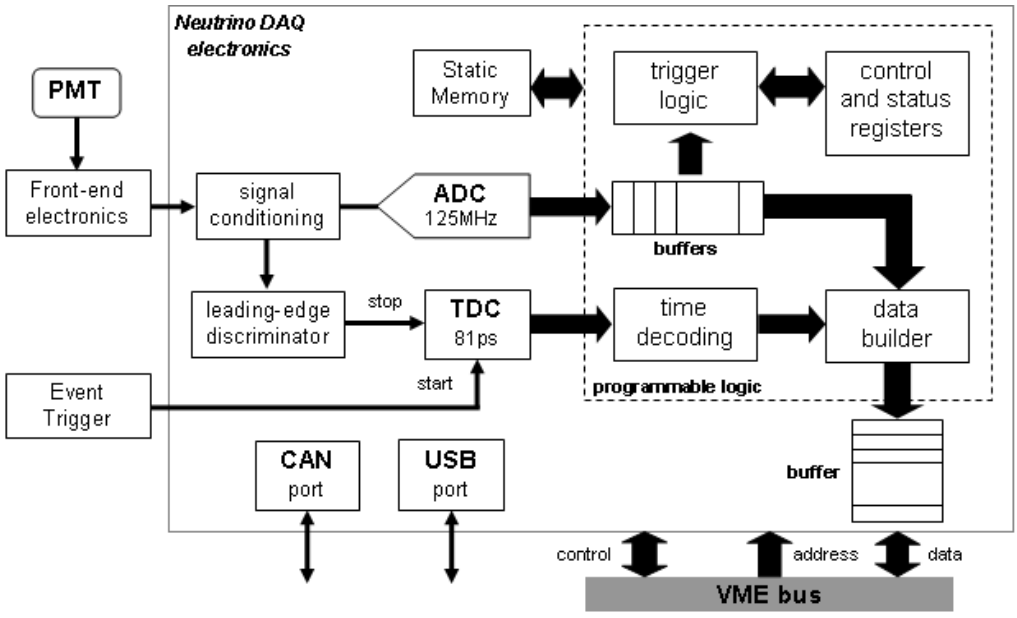

Figure 4: Basic processing blocks of the Neutrino-DAQ (one channel).

After the front-end circuitry, the pulse is sent through two distinct paths. By means of $50\,\Omega$ coaxial cables (RG174), one path takes the signal directly to the analog-to-digital conversion channel in the DAQ module (custom VME standard card). The second branch takes the signal to a leading-edge discriminator that will provide a trigger pulse (Start) to the DAQ. One crucial requirement in the design of the front-end and discrimination circuits is the maximization of the signal-to-noise ratio,

aiming to optimize the analog-to-digital conversion and to extract timing information, by means of a time-to-digital converter.

Therefore, concerning physics data, for each PMT in the central detector, the neutrino DAQ modules receive one analog pulse, proportional in amplitude to the charge deposited by photons in the PMT, and one digital pulse, which gives the instant of the first hit in a group of eight PMTs. Any delay introduced by cables, or propagation delay between and within integrated circuits, will be taken into account in the DAQ digital processing.

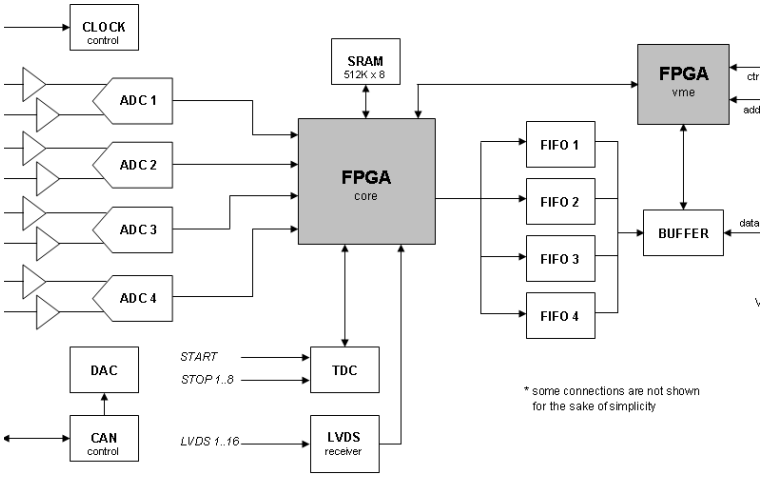

Figure 5: Neutrino DAQ module diagram

3.1 Amplitude measurements (analog-to-digital conversion channels)

A more complete block diagram of the Neutrino DAQ module is presented in Figure 5. The module features 8 analog input channels for digitization at $125\ MHz$ or 4 channels at $250\ MHz$. Each analog-to-digital conversion channel in the module is implemented by using a 12-bit multi-stage pipeline ADC able to sample the input signal at $125\ MHz$. This sample frequency has been selected based on the following reasons: adequate representation of the PMT pulse in time, lower possibility of signal integrity problems, like EMI and crosstalk, lower power consumption of the electronic devices and current status of CMOS technology. By choosing a resolution of $10\ bits$ and a dynamic range of $2\ Vpp$, voltage resolution around $2\ mV$ is achieved. This resolution is expected to cover the required energy resolution (considering $4\ mV$ per photo-electron, see [4]). The analog-to-digital conversion of the input signals is performed in free-running mode, where the signal is sampled and converted at periodic instants, equal to one cycle of the ADC clock frequency. The digitized sample is delivered to a Field Programmable Gate Array (FPGA) with latency of 5 clock cycles, which means $40\ ns$ later. This delay does not impose any limitation to the data acquisition flow since data will be continuously stored by internal buffers within the FPGA, and finally in external FIFOs (First-In-First-Out) memories. A flexibility implemented in the hardware design allows the use of four ADC channels sampling at twice the frequency, that is, $250\ MHz$. This feature may be configured at laboratory by mounting $0\ \Omega$ resistors in the positions indicated by SW1, SW2, SW3 and SW4 in Figure 6, and configuring a clock distribution chip to adjust the phase on two clock signals to 180^o. In this operation mode, only the inputs AIN1, AIN2, AIN5 and AIN6 are used.

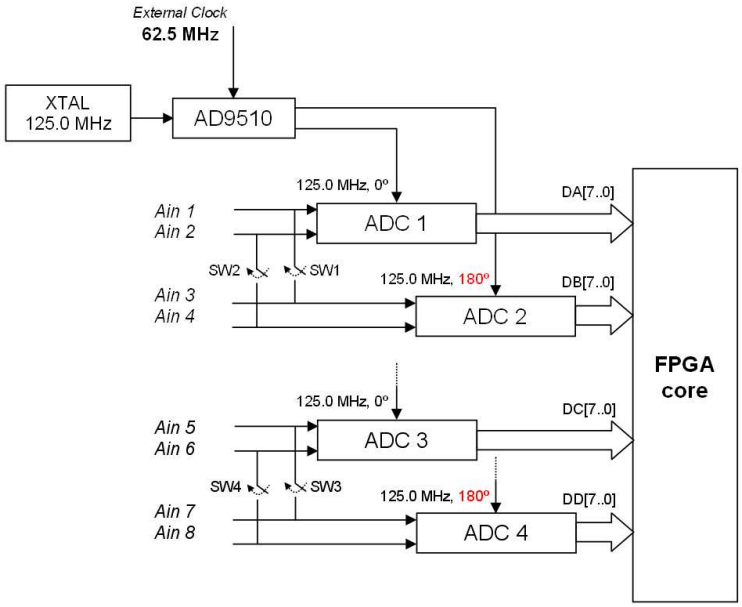

Figure 6: Analog-to-Digital Conversion scheme for 250 *MHz* sampling.

The four data buses from the ADCs feed a digital processing circuit implemented in a single FPGA. Within the FPGA every incoming data word is written into a two-layer buffer scheme (two FIFOs in series) that stores the information during the time needed for a trigger decision. This buffer structure reduces the overall deadtime in the acquisition process and allows the readout of samples before the trigger point. Another layer of buffering (external to the FPGA) stores data already filtered in order to reduce deadtime due to the VME bandwidth and the control software. This last buffer is implemented with high-density CMOS FIFOs. These memories present independent write and read control circuits operating at different clock speeds, which is needed to match the write rate (data coming from the FPGA) with the read rate (limited by VME bandwidth and software processing speed).

3.2 Discrimination and Trigger Logic

Concurrently to the digitization of the analog input signals, eight on-board leading-edge discriminators produce on-board trigger pulses to start the readout of each PMT pulse. Each discriminator receives the output of the amplifier stage and an adjustable threshold, configured through an $8-channel$ DAC configured via CAN port. Discriminator output feeds a combinational logic, inside the FPGA. This logic implements a programmable trigger menu in order to define valid events. The first condition taken into account by the trigger logic is the ocurrence of the PMT pulses inside a pre-defined time window started by an external trigger signal. This coincidence window corresponds to the time interval from the positron detection (prompt) to the neutron capture, which is estimated to be in between $50\ \mu s$ and $150\ \mu s$. Other trigger conditions will be related to pulse amplitude and multiplicity of fired PMTs. The events not selected by the initial trigger conditions will be discarded, which means flushed out of the second buffer layer.

3.3 Time measurements (time-to-digital conversion channels)

For high-precison measurement of time between pulses an 8-channel Time-to-Digital Converter (TDC) chip has been selected. It features one START and eight STOP inputs operating in a common start mode. The TDC provides a digital representation of the time interval between a pulse in the START input and a pulse in the STOP input. Operating in I-mode, the TDC provides resolution of $81\ ps$, dynamic range up to $9.8\ \mu s$ and a continuous acquisition rate per channel of $10\ MHz$. The TDC outputs feed directly the FPGA core, as the ADC outputs do, which allows for amplitude and time measurements in a correlated way in quasi real-time.

3.4 Control (FPGA vme)

The control block, implemented in the FPGA vme (see Figure 7), is responsible for:

- VME protocol decoding
- readout of status registers inside both FPGAs
- configuration of control registers inside both FPGAs
- control of the readout process of the physics and monitoring data

3.5 Neutrino module implementation

The Neutrino DAQ module (NDAQ) is designed as a VME 6U standard module, which means that it follows the VME64 standard in terms of mechanical specifications, electrical specifications and communication protocol. The board features 6 copper layers, being one ground plane, two power planes and three signal layers, as it is shown in Figure 7. In the TOP layer there are both microstrip single-ended and microstrip differential lines (dedicated for clock and data from the ADCs). There are two internal layers dedicated for sriplines carrying high-speed clock signals. The module is designed to be used as a VME standard card or in standalone mode. As a VME card, it receives power from the VME bus and communicates with the outside world through the VME backplane. In the standalone mode it may be used without a VME crate, being powered through an on-board power connector ($+5\ V$) and communicating through an USB port. In principle, all the functionalities available in the VME mode should be present in the standalone mode but it is worth noting that the communication bandwidth is estimated to be much smaller in the standalone case. By using block transfers in the VME bus, a theoretical value of $40\ MB/s$ is achieved, while the USB port is designed to support maximum transfer rate of $1\ MB/s$. Figures 8 and 9 illustrate screen shots of the TOP and BOTTOM layers close to be finished.

4 Conclusions

This document presented the design and current status of the Neutrino DAQ for the Angra experiment, focusing on its hardware implementation. The module under development makes use of state-of-the-art technologies currently available. The complete DAQ, including front-end electronics, VETO system, Slow-Control electronics, High-Voltage system and the high-level control software are not presented. At the time of this document edition, the schematics are complete and the layout desing of the first prototype is under development.

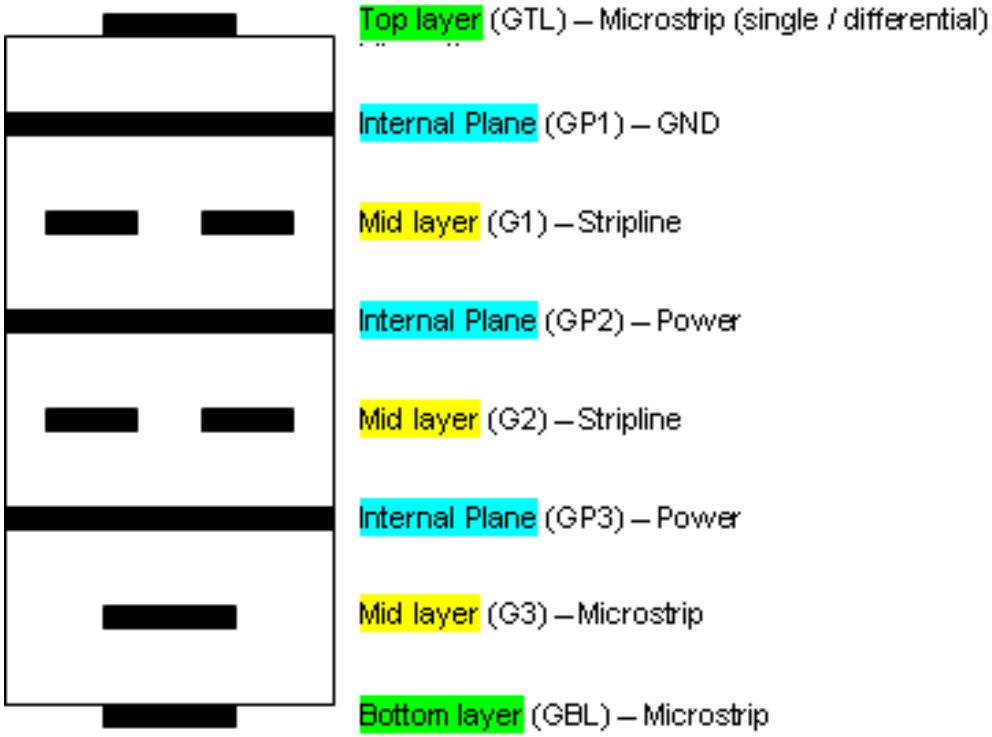

Figure 7: Layer stack of the NDAQ module.

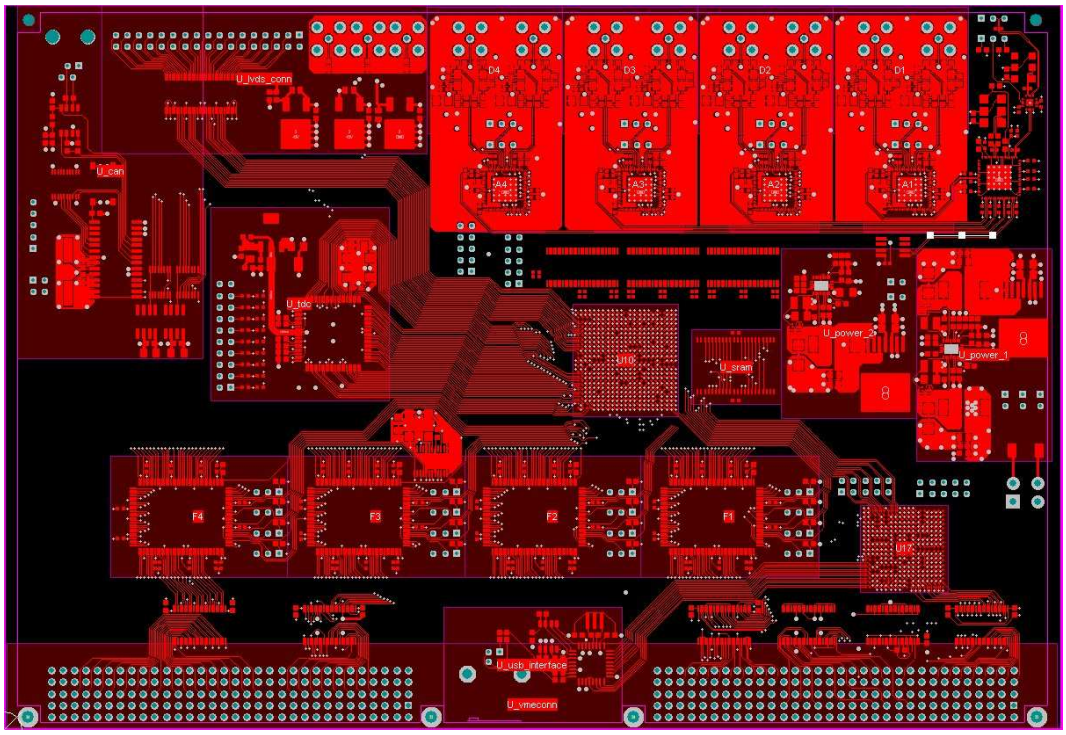

Figure 8: Top layer of the Neutrino DAQ printed circuit board.

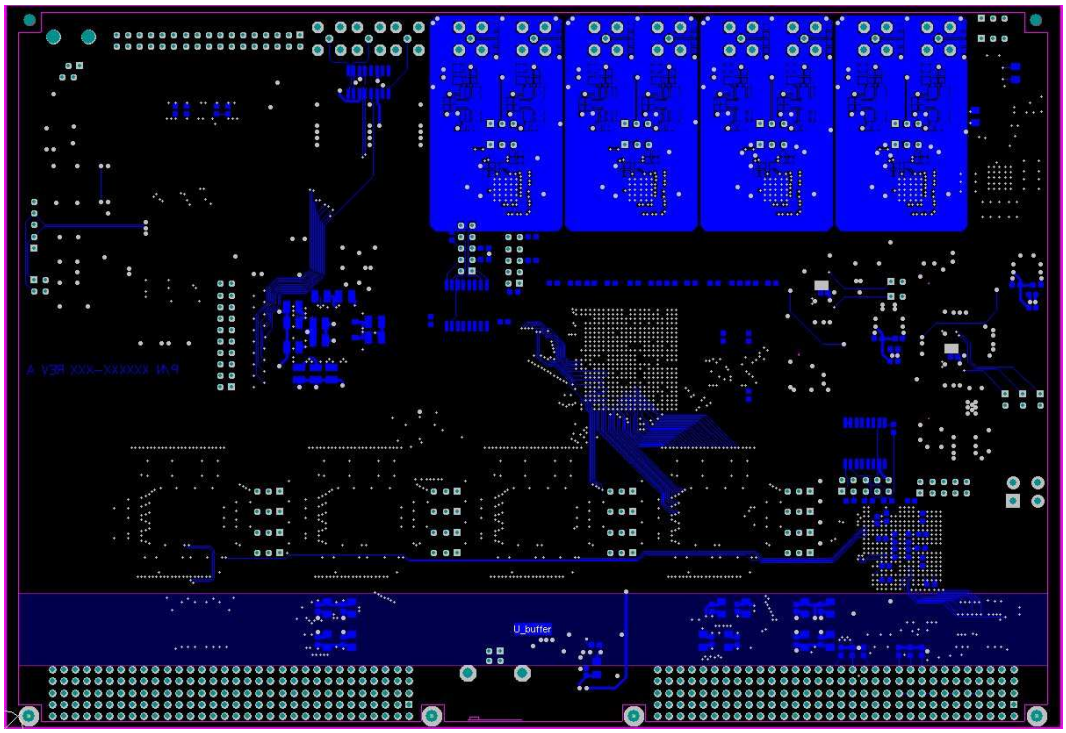

Figure 9: Figure 9: Bottom layer of the Neutrino DAQ printed circuit board.

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[3] ROOT - A Data Analysis Framework, http://root.cern.ch

[4] A. F. Barbosa, *Preliminary simulation study of the front-end electronics for the central detector PMTs*, AngraNote **001-2007**, 2007.