Technology Requirements for Chip-On-Chip Packaging Solutions

M. Töpper, Th. Fritzsch, V. Glaw, R. Jordan, Ch. Lopper, J. Röder, L. Dietrich, M. Lutz,
H. Oppermann, O. Ehrmann, Herbert Reichl
Fraunhofer IZM Berlin / Technical University of Berlin
Gustav-Meyer-Allee 25, D-13355 Berlin, Germany
Phone (+49)-30-46403-603
email: toepper@izm.fhg.de

Abstract

The trend towards smaller, lighter and thinner products requires a steady miniaturization which has brought-up the concept of Chip Scale Packaging (CSP). The next step to reduce packaging cost was the chip packaging directly on the wafer. Wafer Level Packaging (WLP) enables the FC assembly on PWB without interposers. New and improved microelectronic systems require significant more complex devices which could limit the performance due to the wiring of the subsystems on the board. 3-D packaging using the existing WLP infrastructure is one of the most promising approaches. Stacking of chips for chip-on-chip packages can be done by wafer-to-wafer stacking or by chip-to-wafer stacking which is preferable for yield and die size considerations. This chip-on-chip packaging requires a base die with redistribution traces to match the I/O layout of both dice. This allows the combination of the performance advantage of flip chip with the options of WLP. To avoid the flip chip bonding process the thin chip integration (TCI) concept can be used. Key elements of this approach are extremely thin ICs (down to 20 µm thickness) which are incorporated into the redistribution. This technology offers excellent electrical properties of the whole microelectronic system. The focus of this paper will be the technology requirements for the realization of different kinds of chip-on-chip packages.

Key Words: Chip-on-Chip Packaging, Wafer Level Packaging, 3-D Packaging, System in Package (SiP)

1. Introduction

Ball Grid Array (BGA) and later Chip Size Packaging (CSP) have been the most popular single chip packages since the last twenty years. Economic considerations and the transition to 300mm wafer technology have been driving packaging technologies towards the concept of Wafer Level Packaging (WLP) to finalize and test the package for each die before singulation. WLP became an economic solution for a wide variety of applications from low pin count passives, EEPROM, flash and DRAM to ASICs and microprocessors [1]. Area array for the finial bump interconnect is further necessary to match the I/O pitch of the IC to the routing density of the printed circuit board (PCB) which is necessary to combine the different components or modules for microelectronic systems. Redistribution technology established by Sandia and Fraunhofer IZM / Technical University of Berlin (TUB) to reroute peripheral pads into an area array is therefore an essential process step for WLP [2-5]. The similarity in technology and equipment of wafer bumping and wafer level packaging has the advantage for foundries to offer both in high volume.

The trend to higher complexity of semiconductors is represented by the ever increasing number of pin counts and chip performance which is forecasted by the ITRS [6]. Electronic products are grouped together by standardized categories. These groups are: *Low-cost/Hand-held (*<$500), *Cost-performance (*<$3,000), *High-performance (*>$3,000) and *Harsh*. The package pin count forecast for the different electronic application as proposed by ITRS is given in table 1:

Year / Application	Low-cost/ Hand-held	Cost-performance	High-performance	Harsh
2005	134 –550	550 - 1760	3400	550
2012	249 – 932	932 - 3388	4810	812
2015	325 – 1213	1216 4339	6402	933
2018	421 - 1576	1581 - 5642	8450	1235

Table 1: ITRS forecast 2003 of pin counts for different applications [6]

These application areas cover the majority of the product development of the semiconductor industry. The technology addressed in the roadmap provides at least 80% of the revenue in each application area.

Pin count will continue to increase in all segments while die sizes are expected to remain constant. This will drive a continuing need for finer off-chip and off-package pitch. The off-chip digital frequency has been increased to match on-chip in some high-speed communications applications, which will drive the need for improved package signal integrity. This requires significantly more complex packaging approaches which should not limit the performance due to the wiring of the subsystems on the board [7]. One solution is 3-D packaging while stacking of individual plastic packages does not only have the disadvantages of high cost, but at the same time does not offer efficient means to minimize overall package size and to integrate passive components like resistors, capacitors, inductors and filters. 3-D system integration provides a technology to overcome these drawbacks [8]. This vertical stacking using flip chip requires a base die with redistribution traces to match the I/O layout of both dice. This allows combining the performance advantage of flip chip with the option of integrating passive components into the redistribution layer. The technology requirements for chip-on-chip will be discussed using two case examples:

2. Examples for Chip-On-Chip Packaging:

2.1. Emulation Device for Microcontroller Chips

The goal of this project was the technology built-up for an emulation device for a microcontroller. A schematic drawing is given in figure 1:

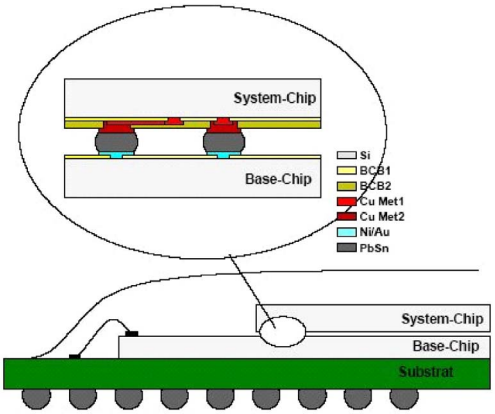

Figure 1: Schematic drawing of the built-up for the microcontroller emulation device

The microcontroller chip is flip-chip bonded on a base chip. This base chip is wire-bonded to a substrate ending with a glop topping process step to encapsulate the stacked dice. At the end all I/Os of the microcontroller chip are connected to the BGA balls on the back-side of an interposer substrate. The geometry of the different components is summarized in figure 2:

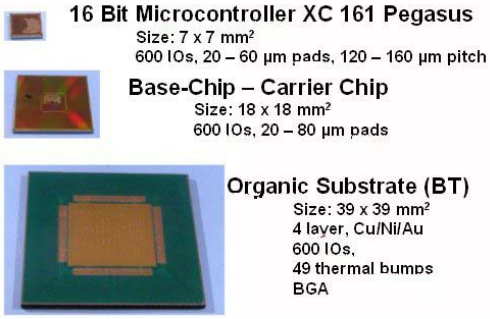

Figure 2: Components of the microcontroller emulation device

This built-up structure allows the teaching and programming of the microcontroller. The microcontroller chip has peripheral and area array I/O configuration with different pad sizes. For standard applications only the peripheral I/Os are in use. For the emulation device all 600 I/Os have to be connected. Therefore a redistribution of the microcontroller is necessary to yield uniform pad sizes of 80 µm with a pitch of 160 µm. Besides data processing and controlling the task of the base chip is to distribute these I/Os to its periphery. The size of the base chip (18 mm to 18 mm) is pad limited. It has two kinds of pads: FC pads in the centre of the die and wire bond pads on the periphery of the chip for the wire bonding process to the interposer. A high reliable FC contact in addition to a wire bondable metal surface requires a well-defined surface metallization of Ni/Au. Figure 3 shows the chip-on-chip with the flip chip mounted microcontroller on carrier chip with redistributed IC-pads. The interconnection from the base chip to the WL-CSP substrate is done using wire-bonding.

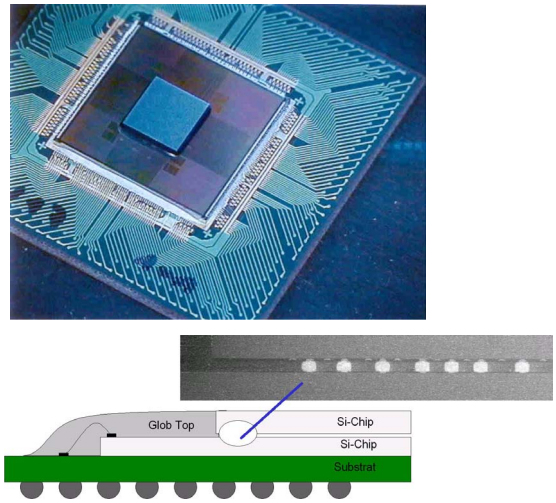

Figure 3: Chip-on-Chip integration using FC-bonding (courtesy of Fraunhofer IZM and Infineon): Top: Chip-Stack bonded to interposer; Bottom: Schematic drawing and SEM

In this 3-D approach a functional base chip on wafer level is used as an active substrate for flip chip bonding of a second die. The electrical and mechanical interconnection is done using eutectic or lead-free solder balls which are deposited by electroplating. The base chip is redistributed to an area array of a solderable UBM. The redistribution consists of electroplated copper traces to achieve a low electrical resistivity. The dielectric isolation is achieved using low-k Photo-BCB. The process is summarized as follows:

1.) Redistribution and Bumping of System Chip
2.) Modification of Carrier Chip for FC and WB
3.) FC Bonding (µC to Base Chip)
4.) Underfilling
5.) Wire Bonding (US) Carrier Chip to Interposer
6.) Encapsulation
7.) BGA Deposition

Fraunhofer IZM is producing these modules in low quantity for prototyping.

2.2. High-Density Multi-Chip Module for a Pixel Detector System (ATLAS Consortium)

This multi-chip module concept is a prototype for a pixel detector system for the Large Hadron Collider LHC at CERN, Geneva. The project is part of the ATLAS experiment [9, 10]. The ATLAS experiment is being constructed by 1700 collaborators in 144 institutes around the world. The main purpose of this detector are the search for the Higgs Boson, the last undiscovered particle in the Standard Model of elementary particles and their interactions and the study of the decays of the top quark, which was discovered 1994, with high statistics.

For the pixel detector a modular system is needed which can be put together to build this large detector system. While the diode-pixel-arrays have an active area of about 10cm^2 the read-out chips are one order of magnitude smaller because of their higher complexity. In general, the diode-pixel-arrays and

the read out chips can be fabricated in wafer size dimensions. Each module is an excellent example showing highest density FC assembly with a 50µm pitch (figure 4).

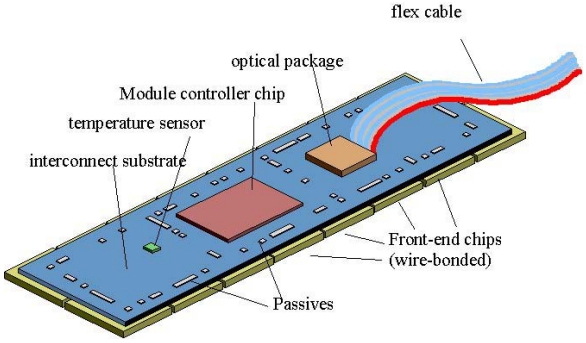

Figure 4: Chip-on-Chip concept for the ATLAS module

A module consists of a sensor tile with an active area of $16.4\text{mm} \times 60.4\text{mm}$ and 16 read out chips, each serving 24×160 pixel unit cells. The sensor wafer is 4" with a thickness of 250µm. 288 electronic chips are on one 200mm wafer. The sensor substrate is smaller than the front-end (FE) read-out chips. On the detector substrate the UBM TiW/Cu is deposited.

3. Technology Requirements

3.1. Thin Film Materials

Fraunhofer IZM / TU-Berlin have developed a redistribution technology for different front-end technologies. It has been proven for a wide range of applications [11, 12]. First a dielectric layer is deposited on the wafer to enhance the passivation layer of the die. Thin film polymers have proven to be an integral material basis for many different types of advanced electronic applications like IC stress buffer layers, MCMs and WLP. The main requirements for the selection of a given polymer are: High decomposition or glass temperature for the high temperature processes in packaging like solder reflow, high adhesion, high mechanical and chemical strength, excellent electrical properties, low water up-take, photo-sensitivity and high yield manufacturability. Mostly thermosets are therefore the polymer class for high-end packaging applications. In addition, the selection of the optimal polymer for a given application depends not only on its physical and chemical properties and processability, but also on its intrinsic interfacial characteristics. The polymer layer under the rewiring metallization acts also as a stress buffer layer for the bumping and assembly processes. Using photosensitive polymers requires fewer processing steps for thin film wiring than non-photosensitive materials that have to be dry etched. PI (Polyimide), BCB (Benzocylo-butene) and PBO (Polybenzoxazole) are common re-passivation materials and are used as insulation for redistribution layers or integrated passives (copper coils) as well. Fraunhofer IZM/TU Berlin use Photo-BCB (Cyclotene from Dow Chemical) [13]. Compared to other polymers BCB has a low dielectric constant and dielectric loss, minimal moisture uptake during and after processing, very good planarization and a low curing temperature.

The rewiring metallization consists of electroplated copper traces to achieve a low electrical resistivity. The plating process for the redistribution can be extended to the bumping process. The same set of equipment can be used without any modifications. A sputtered layer of Ti:W-Cu (200/300nm) serves as a diffusion barrier to Al and as a plating base. A positive acting photo resist is used to create the plating mask. After metal deposition the plating base is removed by a combination of wet and dry etching. A second Photo-BCB layer is deposited to protect the copper and to serve as a solder mask. BCB can be deposited directly over the copper metallization without any additional diffusion barriers. Electroplated Ni/Au is used for the final metallization.

3.2. Interconnet

The major advantage of flip chip assembly is the self alignment function. Chips can be misregistered as much as 50% off the pad center and the surface tension of the molten solder will align the pads of the chip to the substrate metallization. The disadvantage of flip chip assembled ICs is that the bumps are the only mechanical links between chip and substrate. As a consequence the stress caused by the CTE (coefficient of thermal expansion) mismatch of the semiconductor die and the substrate act only upon the bump interconnects.

A major requirement for the flip chip interconnections are modified pads on the IC. The so called UBM (Under Bump Metallization) or BLM (Ball Limiting Metallurgy) is the basis for a low-ohmic electrical, mechanical and thermal contact between chip and substrate. It has to be a reliable diffusion barrier between IC pad and bump with low film stress and it needs to be sufficiently resistant to stress caused by thermal mismatch or during die assembly. In case of PbSn bumping common UBM stacks are Cr-Cr:Cu-Cu-Au (original C4 from IBM); Ti-Cu; Ti:W-Cu; Ti-Ni:V; Cr-Cr:Cu-Cu; Al-Ni:V-Cu; Ti:W(N)-Au. Usually, these UBM stacks are subsequently deposited by sputtering.

The electroplating bumping technology can be used even for a pitch below 40µm. The pitch of the I/Os of the pixel detector for example is 50µm and redistribution to a larger pitch was not possible. Therefore, PbSn bumps were plated for the flip chip assembly of the chip-on-chip stack. A layer of 200nm Ti:W is sputtered on the whole wafer as an adhesion layer and diffusion barrier, followed by a second layer of 300nm copper which is used as the plating base. High viscous photoresist is used to produce resist layers with a thickness of 5µm up to nearly 100µm by spin coating and patterning process with a yield close to 100%. Before the plating base is etched, the photoresist has to be removed without any residues. Essential for a wet etching process is that the etchant should erode the thin film plating base uniformly and completely, but avoiding under etching. The ohmic resistance of the electroplated PbSn bumps is 2mΩ for 100x100µm bumps [14].

The assembly was done by pick and place using the FC-Bonder FC 150 from SüssMicrotec. In the case of PbSn bumps deposited onto a copper based UBM intermetallics compounds (IMCs) between Sn and Cu are formed by the reflow process providing the required adhesion of the bump to the chip pad (figure 5 and 6).

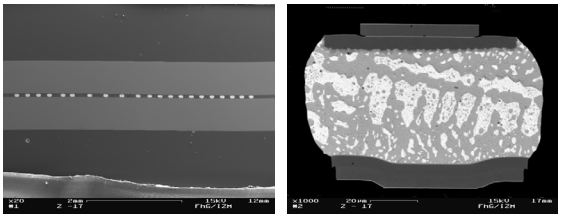

Figure 5: Left: Cross Cut of FC bonded µC emulation stack; Right: Detail

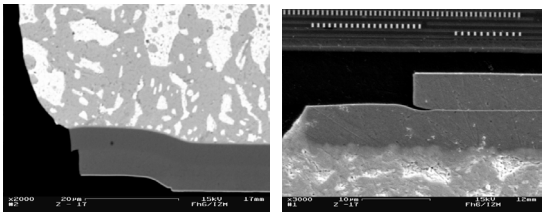

Figure 6: Details of Carrier (left) and µC (right)

IMCs are brittle in nature due to the ordered crystal structure which is in contrast to the solid solutions like the PbSn. These compounds are based on Hume Rothery type with electron valence bonding. The crystal structure is controlled by the number of electrons in the bonding. For example the Cu_3Sn and the Cu_6Sn_5 phases are found for intermetallics of Cu and Sn and Ni_3Sn_4 and Ni_3Sn phases are formed between Ni and Sn. The growth rate depends on temperature, the different activation energies of compound forming and diffusion processes. Ni is preferred due to the slower growth rate of the intermetallics.

3.3. Chip Thickness

Failure analyses of the pixel detectors have shown that thinning of the FC-bonded dice is limited by the FC interconnection. In the case of the pixel detector project the dice have a size of 11 mm by 7 mm. The metallization consists of 6 metal layers and nearly 3000 bumps with a diameter of 25 µm. The thickness of the Si was varied by the grinding process after bumping. The failures were high ohmic contacts or open connections mostly detected at the edges of the chips. The influence of the die thickness was proven by an analysis of the mechanical deformation during the assembly process. The mechanical deformation of the chips during reflow process was detected by laser leveling measurements at discrete temperatures. To avoid errors from moving the gauging head a laser leveling with a beam splitter and a beam divider was used. The difference distant measurements were done between the die below the interferometer and a temperate polished silicon wafer piece on top. The temperature was applied with an infrared heated thermode and an equilibration time of 5 min was given. Figure 7 to figure 9 shows the bowing of the chip depending on thickness and temperature. The three measurement points were located at the upper left corner (point 1), center (point 2) and lower right corner (point 3). It is obvious that the temperature depending bowing is significant correlated with the thickness of the dice. For the chip with a thickness of 180 µm the center is about 10 µm lower than the level of the chip edges at soldering temperature (figure 7). This deformation increases for chips with 160 µm thickness to 14 µm (figure 8) and to 17 µm if they are thinned to 130 µm (figure 9).

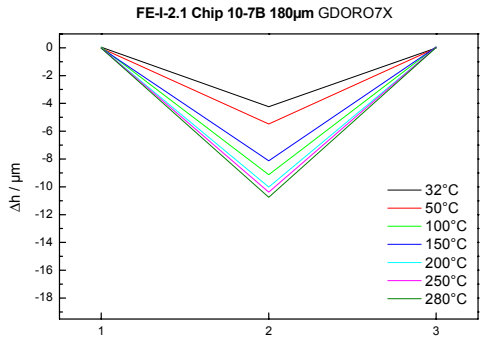

Figure 7: Chip with 180 µm thickness

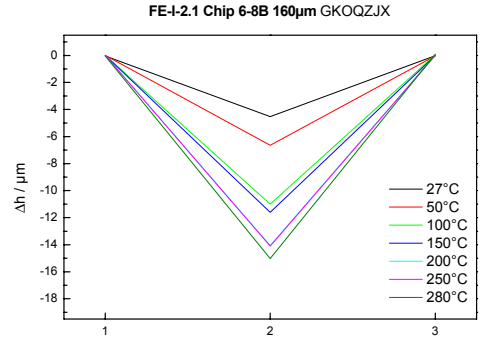

Figure 8: Chip with 160 µm thickness

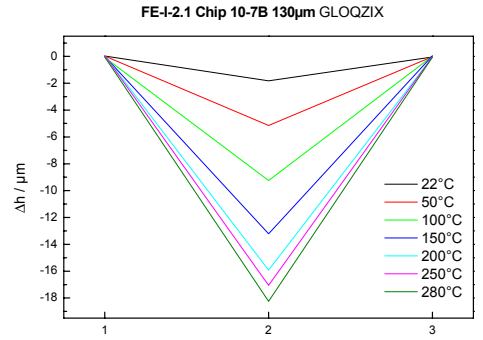

Figure 9: Chip with 130 µm thickness

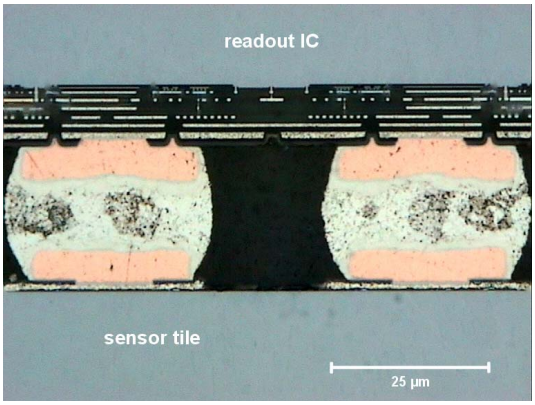

Figure 10: Cross section of assembled sensor

The bowing is caused by the CTE of the metals used for the intra wiring of the bottom chip which is about 4 times higher than pure Si.

During the beginning of the reflow the bumps in the center of the chip build a 10 µm thick liquid phase (Figure 10).

Therefore the outer area of the chips should not be higher than 12 µm above the carrier Si to allow a good wetting of the pads on the substrate. Therefore the suggestion is given to use at least 180 µm thick chips, better 200 µm for the given example.

3.4. Yield and KGD

An important factor of such complex module is the importance of KGD (Known Good Die) and the possibility of repair. In figure 11 the yield of pixel detector modules is calculated versus the chip yield:

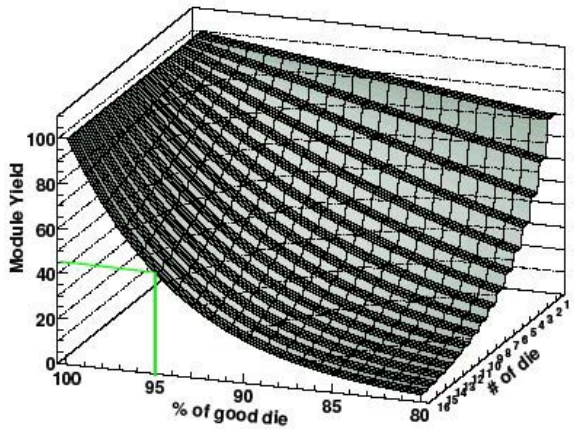

Figure 11: Module yield as a function of KGD and number of dice for the pixel detector system[15]

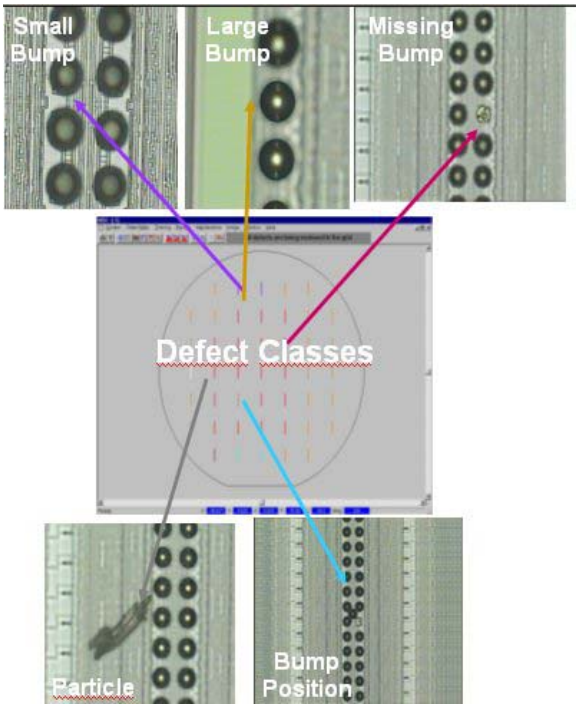

Figure 12: Defect control of bumped electronic wafers (Pixel Detector Module)

A total module yield of only 44% can be achieved if the chip yield is 95% for this 16 chip module. Therefore an extensive test and inspection procedure was established. Examples of the automatic optical tests are show in figure 12.

In general the process flow was optimized to maximum process yield. The different steps for the pixel detector are summarized below:

1.) Sensor wafers: Electrical test, cleaning, optical inspection, UBM deposition by sputtering, lithography and plating, dicing, cleaning, end inspection.

2.) Electronic wafers: Electrical test, cleaning, optical inspection, UBM and bump deposition by sputtering, lithography and plating, inspection, thinning and dicing, sorting, cleaning, single chip inspection, FC, x-ray, electrical module testing, (repair)

A repair by de-attach of single chips has been successfully demonstrated. Therefore a yield of over 98 % has been achieved for the first 280 modules (16 electronic chips on a sensor).

4. Reliability

The reliability was checked by thermal cycling (AATC -55°C to 125°C). Cross cuts of the microcontroller emulation stack after 3000 cycles are given in figures 13 and 14:

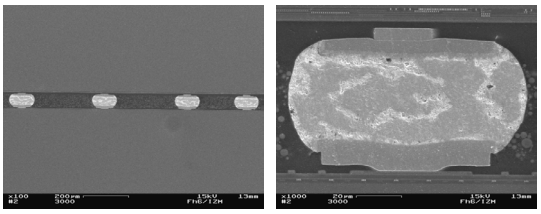

Figure 13: Left: Cross Cut after 3000 cycles (-55°C / +125°C) of bonded µC emulation stack; Right: Detail

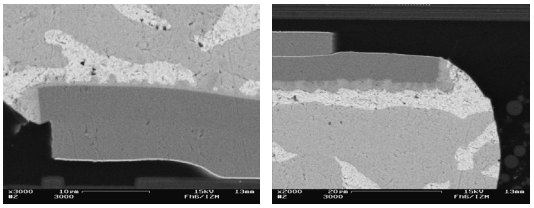

Figure 14: Details of Carrier (left) and µC (right)

No Delamination of the redistribution or the UBM could be detected. A stable growth of the intermetallic Hume Rothery phases is visible. No cracks occurred.

5. Potential for Higher Integration

5.1. From 3-D WLP to SiP

The potential of integrating passives into 3-D packages is obvious if one consider the change in electronics going from single transistors to the concept of IC. Moore`s law was the result of the constant developments in on-wafer technologies. The main difference is that the passives cannot be scaled down to sub-microns due to physical limits. In addition there is a limitation in reducing footprint for integrated passives. The integration of resistors, capacitors and inductors using thin film techniques on top of the wafers are adding further functionality on finished devices wafers. Smart combinations of these elements can be used to build filters etc. [16].

Higher integration will bring 3-D to SiP. The definition of SiP is still not well established across the literature [17]. It is basically a synergy between the semiconductor industry, system designers and the different packaging concepts. Motivation is the fact that Moore`s law is more and more restricted by packaging and substrate technology than by front-end technology. SiP will strongly benefit from all different kinds of technology developments in microelectronics. The strongest contribution will be coming from Wafer Level Packaging including Thin Film substrates and FC bonding, Integrated Passives and 3-D stacking (figure 15):

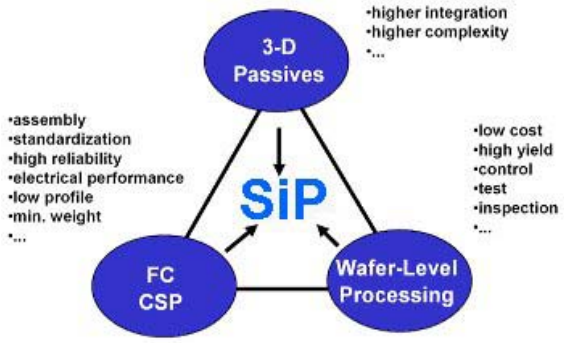

Figure 15: The advantages of FC/CSP, 3-D integration, integrated passives, and the economics of wafer processing are combined in SiP technology

Fraunhofer IZM has developed a novel multi-chip Wafer-Level 3-D package with a "Thin Chip Integration" concept (TCI) to handle the necessity for enhanced functionality.

5.2. Thin Chip Integration (TCI)

Key elements of the TCI approach are extremely thin completely processed wafers and chips (figure 16) [18].

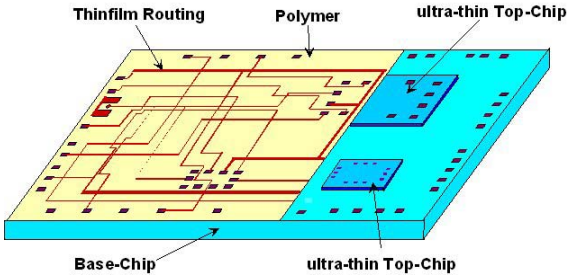

Fig. 16: Principal of TCI

In contrast to existing packaging techniques the TCI concept uses 20 µm thin chips mounted to a base chip by a conventional adhesive. This technology replaces the conventional substrate. Application of bonding or soldering techniques which might limit the reliability is avoided. In addition this offers excellent electrical properties of the wiring system and the interconnection of the active and passive devices. The signal transmission time for high speed memory modules will be reduced compared to single chip packages. The design for the electrical wiring within the chip arrangement can be selected by the customer. The following metallization processes are done at wafer level as well as the final standard wafer level CSP process. Process flow for TCI modules starts up with one type of bottom-wafer carrying large base chips. The completely processed device wafers for the top-IC have to be mounted on a carrier substrate by a reversible adhesive bond and undergo a backside thinning process until the thinned wafers show a remaining thickness of approx. 20 µm. The bottom wafer is coated with a thin epoxy film and the thinned top-chips are placed and mounted into this adhesive layer. Now the photo-sensitive low k dielectric BCB polymer is deposited onto the surface to planarize the 20 µm topography of the mounted thin chips. A high degree of planarization (DOP) which is one of the advantages of Photo-BCB is very important for this first polymer layer in order to overcome the step between the surface of the bottom chip and the thinned chips. The standard redistribution of Fraunhofer IZM / TUB can now be used for the interconnection. A final CSP process, using a solderable metal layer and solder bump deposition completes manufacturing of the TCI module. Figure 17 shows a cross section of an ultra-thin Top-Chip on bottom wafer planarized by a 30 µm thick Photo-BCB layer and with an additional Cu-layer redistributed wafer with the UBM.

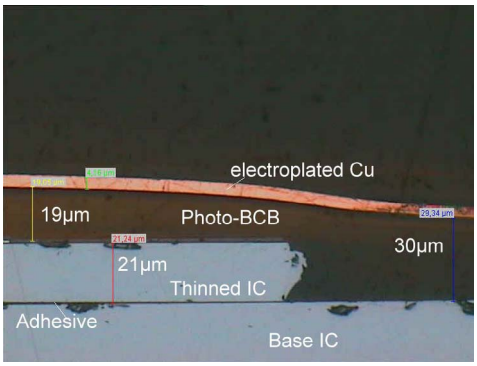

Figure 17: A thinned chip planarized with a thick BCB-layer and an additional Cu routing for TCI (cross section).

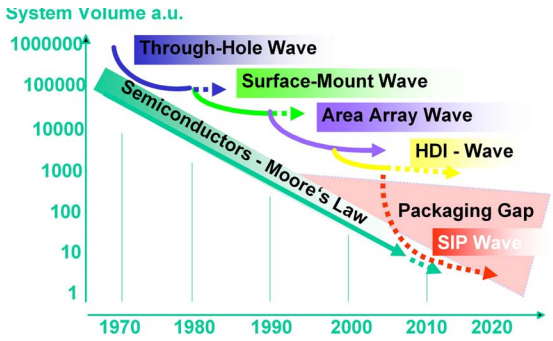

Figure 18: The increasing role of packaging for microelectronic systems

The reliability of the TCI was approved by AATC (-55°C / +125°C). No cracks or delami-nation were detected after 1000 cycles.

6. Conclusion

The company Philips [19] brought it to the point that there is "More than Moore" emphasizing the need of cooperation

between semiconductor, inter-connection, integrated passives, substrate and system design. The increasing role of packaging for microelectronic systems is schematically shown in figure 18:

Even though the SMT and Area Array technology were major developments in the electronic industry the gap between semiconductor technology and packaging has been increasing. System in Package will be the packaging wave for the next ten year to keep the Moore`s law growing although for higher system performance. 3-D packaging approaches like the chip-on-chip technology and TCI will play a mayor role due to the existing production infrastructure.

7. Summary

WL-CSP/WLP has been established as one of the key packaging technologies of today. The reliability and the economics have been proven in numerous applications. 3-D integration using chip-on-chip stacking can adopt the reliable WLP concepts with the need of less board space in conjunction with reduced interconnection length providing less parasitic effects for high frequency applications. The concept was proven by two examples. Highest interconnect pitch has been achieved for a pixel detector and a microcontroller emulation device. There are no basic requirements which are in contrast to industrial production. Mostly standard processing equipment can be used which is already in production for wafer bumping or WLP.

Integrated passive components [16] and TCI technology will further push WLP. As a consequence WLP will move to SiP. The industry-wide adoption of WLP and SiP will benefit from the flip chip and wafer bumping infrastructure which is currently created at a breathtaking pace because process technology, process equipment and materials and general mode of thinking bear many similarities.

WLP has to change into more complex system integration like chip-to-chip stacking to face the rapid developments in semiconductors and to satisfy the increasing functionality asked by the consumers.

8. Literature

[1] Phil Garrou “Wafer-Level Packaging Has Arrived” Semiconductor Int. Ocober 2000, p. 119

[2] R. Chanchani, K. Treece, P. Dressendorfer. “mBGA Technology“ Int. Journal of Microcircuits and Electronic Packag., Vol. 18, no.3, 1995

[3] J. Simon, M. Töpper, G. Chmiel, H. Reichl. “A Comparison of FC Technology with CSP” Proceedings of the IEPS 1995

[4] M. Töpper, J. Simon, H. Reichl “Redistribution Technology for CSP using Photo-BCB” Future Fab Int. 1996

[5] M. Töpper, M. Schaldach, S. Fehlberg, C. Karduck, C. Meinherz, K. Heinricht, V. Bader, L. Hoster, P. Coskina, A. Kloeser, O. Ehrmann, H. Reichl „Chip Size Package - The Option of Choice for Miniaturized Medical Devices“ Proceedings IMAPS Conference San Diego, USA 1998

[6] http://public.itrs.net/

[7] M. Töpper, P. Garrou “The Wafer-Level Packaging Evolution” Semiconductor Packaging October 2004, p 5P-20

[8] Y. Degani, T.D. Dudderar, R.C. Frye, K.L. Tai, M. Y. Lau, B. Han “Microinterconnect Technology” in Flip Chip Technologies edited by John Lau, McGraw Hill, 1995, pp. 181 - 222

[9] K.-H. Becks et al, “A Multi-Chip Module, the Basic Building Block for Large Area Pixel Detectors”, Proceedings of IEEE MCM Conf. (1996)]

[10] M. Töpper, P. Gerlach, L. Dietrich, S. Fehlberg, C. Karduck, C. Meinherz, J. Wolf, O. Ehrmann, K.-H. Becks, H. Reichl, ”Fabrication of a High-Density MCM-D for a Pixel Detector System using a BCB/Cu/PbSn Technology“, The International Journal of Microcircuits & Electronic Packaging Issue 4, Vol. 22, No.4, 1999, pp 305 -311

[11] M. Töpper, M. Schaldach, S. Fehlberg, C. Karduck, C. Meinherz, K. Heinricht, V. Bader, L. Hoster, P. Coskina, A. Kloeser, O. Ehrmann, H. Reichl “Chip Size Package - The Option of Choice for Miniaturized Medical Devices”, Proceedings IMAPS Conference San Diego, USA 1998

[12] M. Schaldach, M. Töpper, J. Müller, M. Starke, T. Tessier, O. Ehrmann, H. Reichl, “State-of the Art Technology Development for Medical Implantable Systems”, Proceedings IMAPS 98, San Diego, USA, Oct. 1998

[13] M. Töpper, A. Achen, H. Reichl, “Interfacial Adhesion Analysis of BCB / TiW / Cu / PbSn Technology in Wafer Level Packaging”, Proceedings ECTC 2003, New Orleans, May 2003

[14] L. Dietrich, J. Wolf, O. Ehrmann, H. Reichl “Wafer Bumping Technologies Using Electroplating for High-Dense Chip Packaging”, Proceedings Third International Symposium on Electronic Packaging Technology (ISPT’98), Beijing (China), Aug. 17 – 20, 1998

[15] Ch. Grah, “Das Atlas Experiment und Fraunhofer IZM”, AVT Workshop TU Berlin, Germany, April 2004

[16] K. Zoschke, J. Wolf, M. Töpper, O.Ehrmann, Th. Fritzsch, K. Scherpinski, F.-J. Schmückle, H.Reichl “Thin Film Integration of Passives - Single Components, Filters, Integrated Passive Devices” Proceedings of the ECTC Conference, 2004, Las Vegas, May 2004

[17] M. Töpper, E. Jung, K.-F. Becker, V. Glaw, K. Zoschke, Th. Fritzsch, O. Ehrmann R. Aschen-brenner, H. Reichl “Evolution of WLP: From Redistribution to 3-D Packaging and MEMS Packaging“ IWLPC Conference October 2004, San José, California, USA

[18] M. Töpper, K. Scherpinski, H.-P. Spörle, C. Landesberger, O. Ehrmann, H. Reichl, „Thin Chip Integration (TCI-Modules) – A Novel Technique for Manufacturing Three Dimensional IC-Packages”, Proceedings IMAPS 2000, Boston, USA, September 2000

[19] van Roosmalen, “There is More Than Moore”, 5th Int. Con. on Mech. Sim. and Exp. in Microelectronics and MST, EuroSim2004