DESIGN AND IMPLEMENTATION OF ONLINE MODE SWITCHING ON HYBRID SOFTWARE RADIO PLATFORMS

Yahia Tachwali (ytachwali@ou.edu), Fadi Basma (fadi.basma@ou.edu), Mustafa Chmeiseh (mustafa.chmeiseh@ou.edu), Hazem H. Refai (hazem@ou.edu)
The University of Oklahoma, Department of Electrical and Computer Engineering, Tulsa, OK. 74135

ABSTRACT
This paper demonstrates the design and implementation of a configurable mode transceiver using software radio platform. The work implements a radio transceiver in which its communication modulation and frequency carrier can be altered while maintaining operation. The designed transceiver switches between amplitude modulation (analog) and differential binary phase shift keying (digital) upon a user request. While it is capable of automatically switching its frequency carrier upon an increase in bit error rate due to degradation of its wireless channel. The transceiver combines the signal processing modules to perform a configurable multimode radio. The design of the transceiver is implemented using a small form factor software defined radio (SDR).

INTRODUCTION
A myriad of wireless standards have emerged in recent decades. While these standards support many applications with different quality of service requirements over different geographic scales, they are not necessarily incompatible. Therefore, it becomes desirable to have multi-band multi-mode (MBMM) wireless platforms that interoperate with different wireless standards. SDR is becoming a promising solution to bridge the interoperability gap between these standards. However, software radio relies on the advancement of many enabling technologies [1]. Configurable computing platforms are considered the core enabling technology for SDR since it provides the flexibility required to maneuver between different wireless communication bands and operation modes, and the computational power required to support a wide range of bandwidths.

In order to design and implement a configurable MBMM software radio platform, two important design decisions needed to be taken. First decision is the architecture of the configurable MBMM radio that features sufficient flexibility and hardware efficiency. The second decision is to determine an appropriate online mode switching mechanisms to obtain seamless and error-free mode transitions.

This paper reports the design and implementation of MBMM software radio. The paper discusses the two design decisions mentioned earlier in the process of the design; namely, the architecture and mode switching mechanism. The main contributions of this work are as follows:

- It provides a systematic approach to build a configurable multimode radio based on hardware reuse.
- It proposes a mode switching control architecture.
- It underscores software and cognitive radio design concepts, namely, configurability and adaptability, where configurability is discussed in terms of signal processing backbone reuse by variant communication modes and defined as the ability to switch between the modes. Adaptability in cognitive radios enables an automatic communication mode selection based on wireless channel conditions.

The paper is arranged as follows: First, we will provide a background represented by reporting the efforts of research community in building configurable radio platforms. Next, we will take a high level look at the SDR platform used for building our configurable radio. Then, we will describe the capabilities of our proposed configurable radio. We will also discuss design procedures in two folds; the architecture and switching mechanism designs. Finally, we will conclude by summarizing the main design elements presented in this work. Also, we will highlight the limitations realized and what is going to be addressed in future work.

BACKGROUND
SDR is an important element of wireless technology and fast becoming a hot topic in the telecommunication field. It provides a flexible radio architecture that enables the radio behavior to change according to performance requirements. Consequently determining the digital hardware composition of a software radio constitutes a fundamental design step. Configurable computing platforms used for software radio contains one or more processing engines such as general purpose processors, digital signal processors and field programmable gate arrays. One viable solution for SDR implementation is the hybrid GPP/DSP/FPGA architecture. This mixture of processing elements facilitates a balance in cost, power, performance, flexibility, and reliability [2].

Many studies have reported the implementation of a wireless waveform using this architecture [3]. However,
the focus of these studies is to illustrate porting the implementation of these waveforms from waveform dependant architecture to generic hybrid SDR architecture. In the context of MBMM radios, the configurability and mechanism of switching becomes a design challenge especially in FPGAs. The field programmable gate arrays have attracted many software radio researchers due to their unique capability in performing parallel computations [4]. However, it suffers from a number of limitations which have been addressed in many studies such as design portability [5-6], dynamic configurability [7] and interoperability [8] with other processing engines in hybrid SDR platforms. These limitations did not prevent FPGAs from being an active element in software radios that is mainly used to perform computationally intensive signal processing functions such as up/down conversions, coding/decoding and error corrections algorithms. The dynamic configurability in FPGA transceiver designs are achieved by choosing an appropriate flexible architecture that requires reasonable hardware resources and reconfiguration time [7]. Based on the work of [7], the partial dynamic reconfiguration architecture is suggested. This architecture is implemented by exploiting the signal processing commonalities between supported air interfaces to formulate the common digital processing backbone. The main common functionalities of digital radios are sample rate conversion and channelization [9]. The main benefit of this architecture is the hardware reuse obtained by sharing the common signal processing backbone between supported modes. This architecture is adopted in our configurable multi-mode radio. However, we are going to explain in more details the design considerations to develop the common signal processing backbone and to build a partial configurable signal processing chain. In addition, a switching control architecture is added to insure seam-less transition.

THE SOFTWARE RADIO PLATFORM

The configurable wireless transceiver is implemented using a modular small form factor (SFF) SDR platform produced by Lyrtech. Figure 1 shows a simplified hardware block diagram of the SDR platform which consists of three modules: digital signal processing module, data conversion module and RF module. The digital transceiver design is implemented in the digital signal processing module. The other two modules are configurable through a number of control signals generated from the digital signal processing module. The digital signal processing module uses a Virtex-4 FPGA and DM6446 DMP. The DMP chip features an advanced Very Long Instruction Word (VLIW) DSP portion which is responsible for some signal processing tasks in the transceiver design, and a Reduced Instruction Set Computer (RISC) ARM9 core which is used for running a real-time operating system RTOS. The data conversion module is equipped with a 125 MSPS, 14-bit dual channel ADC and a 500 MSPS 16-bit dual channel interpolating DAC. It is equipped also with programmable gains at the input and output of the ADC and DAC respectively. This enables the implementation of automatic gain control AGC and transmission power control. The RF module is configured to have either 5 or 20 MHz bandwidth with transmission frequency range of 200-930 MHz and receiving frequency range of 30-928 MHz. The digital transceiver implementation in this paper is centered at 400 MHz which is within the optimum operation range of the available platform antennas. Interfacing between DSP and FPGA is achieved using different connections. The main bridge between the two processing engines is the Video Processing Sub-system (VPSS) data port, i.e. a DM6446 DSP 16-bit synchronous video data transfer port. The VPSS is composed of the video processing front end (VPFE) and the video processing back end (VPBE), where the VPFE is used as an input interface to the DSP and the VPBE as an output interface from the DSP. The VPSS was adapted to be used on the digital processing module of the SDR platform as an interface to transfer data other than video between DSP and FPGA. In order to emulate video signals, Vsync and Hsync signals are generated by the VPFE of FPGA interface. The FPGA VPBE uses the Vsync and Hsync signals generated by the DSP to synchronize the incoming data transfer. Also, another interfacing method is achieved by custom registers. These registers are shared memory blocks of eight 32-bit words between DSP and FPGA On-Chip Peripheral Bus (OPB). Additional information about the hardware specification can be found in [2].
CONFIGURABLE TRANSCEIVER DESIGN

The configurable transceiver is based on GPP/DSP/FPGA software radio architecture. It is composed of four subsystems:

- **Digital modulation**: differential binary phase shift keying (DBPSK)
  The digital modulation transceiver is based on differential binary phase shift modulation. It supports a data rate of 244.14 kbps (signals sampled at 24.414 kHz with 10 bits for each sample).

- **Analog modulation**: amplitude modulation with double/single sideband (AM-DSB/SSB)
  The analog modulation transceiver is based on double side-band amplitude modulation with optional single side-band mode. The analog modulation mode is also capable of transmitting a signal sampled at 24.414 kHz, where the modulation mode is chosen manually by the user.

- **Manual modulation mode switching mechanism**
  In order to achieve efficient hardware utilization, the common structure between the two modulation modes is highlighted and used to implement an efficient multimode wireless transceiver with online mode switching capability. Switching between modulation types is performed by configuring the modulation specific blocks. This switching is manual; triggered by the user.

- **Automatic frequency switching mechanism**
  The automatic frequency switching mechanism is effective in digital modulation mode. It enables the transceiver to automatically switch on-the-fly between two communication channels upon detecting wireless channel quality degradation.

The design and implementation of the first and second subsystems are discussed in more details in [2], [10-12]. The focus of this paper is on the building the third and fourth subsystems.

BUILDING THE COMMON SIGNAL PROCESSING STRUCTURE

The exploitation of commonalities of different communications modes proves a challenge when designing a configurable digital transceiver for a software radio terminal. This is especially true if the modes are dissimilar, i.e. analog and digital modulation modes. The proposed software radio design aims to maximize the reuse of digital signal processing blocks. This section details the approach of determining the common structure between AM and DBPSK transceivers, suggesting how to avoid implementing two independent transceivers in the software radio platform. This approach is performed in two stages.
Figure 3: Hybrid AM/DBPSK Transmitter Structure

extract the original signal and pass it to DSP through VPSS bus. Note the possible need for synchronization and carrier recovery stages at the receiver when using coherent receiver structures. Further details on building configurable symbol synchronizers are found in [3], [13]. By inspecting the high-level view of the signal processing chain, we realize that many stages can be reused. However, the modulation stage and sampling rate conversion should be carefully designed to increase the hardware reuse and support both modulation techniques. This is addressed at the next stage of the design.

The second stage is the bit-level AM/DBPSK transceiver structure design. The following design elements are considered:

- The transmitted signal characteristics (bandwidth)
  One of the most important design considerations is the bandwidth of the transmitted signal. By having a sampling rate of 24.414 kHz, it is possible to have two kinds of signals: 1) the analog modulated signal, which is limited to 12 kHz bandwidth approximately; and 2) the digital modulated signal which is limited to \( 24.414 \times 10 \text{ bits} = 244.14 \text{ kbps} \). Upon using an excess bandwidth factor of 0.5 in the pulse shaping stage, the occupied bandwidth used by the digital modulated signal is 366.21 kHz. This baseband signal bandwidth is the largest among all the possible baseband signals that may pass through the signal processing chain. Therefore, it identifies the Nyquist boundaries required for sampling rate conversion stages.

- The sample rates conversions

Figure 4: Hybrid AM/DBPSK Receiver Structure

There is a design trade-off between transceiver supported data rates and energy consumption. Software radio design utilizes multi-rate signal processing techniques in order to manipulate this trade-off and to achieve a balance between performance and energy consumption. Regarding the design of a multirate system, it is important to comply with anti-aliasing constraints. The common structure is conservatively designed for the widest possible bandwidth, i.e. 366.21 kHz. Designing for this scenario provides the chance of reusing a portion of the signal processing blocks for alternate communication modes, which run at less bandwidth, i.e. the AM signal.

- The resolution (bit size) used at different stages of the digital portion of the transceiver

The digital portion of the wireless transceiver is composed of various digital components, including DSP, FPGA, and ADC/DAC, each with different capacities and resolutions. DSP is a 32-bit digital component and is connected to FPGA through a 16 bits VPSS bus (interested reader can find the buffering and communication mechanism of VPSS bus in [2]). Due to its flexible structure, FPGA can manage a variety of bit-sizes. DAC has a 16 resolution while ADC has 14 bits only. Most wireless communication waveforms utilize 10 to 12 bits resolution in their baseband processing level. The configurable transceiver in this work uses 10 bits resolution based on ADC SNR limitations.

The hybrid transmitter design is illustrated in figure 3 and the hybrid receiver design is shown in figure 4.
Common transceiver signal-processing blocks include the signal generation and display, up/down conversion, DAC, ADC, and RF board. Bit conversion stages are omitted for simplification.

The signal generation stage samples the signal to be transmitted, where the sampling rate is the main constraint and must fulfill the Nyquist requirements for all communication modes.

The up/down conversion stage is comprised of up/down-sampling and mixing subsystems. In order to share the up/down-sampling subsystem, determining the up/down-sampling ratio is required for each communication mode. This up/down ratio is calculated by finding maximum common divider of total up/down sampling ratio for each communication mode. In our configurable transceiver, the AM transmitter requires a total up/down-sampling ratio of 5120, while the DBPSK transmitter requires 64. Therefore, the common up/down-sampling subsystem is 64, which is the maximum common divider of 5120 and 64. The mixing stage is defined by the IF frequency choice, which is selected based on hardware limitations, namely, the ADC and the RF board.

The DAC, ADC, and up/down conversion stages are mutually dependant. The sampling rate of the ADC and DAC determines one boundary of the total sampling rate conversion ratio. In the configurable transceiver, the sampling rates of the ADC and DAC are identical and fixed (125 MHz).

An RF board can be designed to achieve a certain selectivity and sensitivity for all communication modes. It must support the maximum possible signal bandwidth of any communication mode.

**AUTOMATIC CHANNEL SWITCHING MECHANISM**

The automatic channel switching mechanism platform is capable of changing its communication channel upon degradation in the wireless channel quality. Wireless channel quality is defined as the suitability of a wireless channel to carry the transmitted signals with an acceptable received error rate. There are direct and indirect techniques that can be used to estimate the wireless channel condition. Direct techniques, such as measuring the error rate, can identify channel quality degradation. This requires the availability of the original transmitted signal at the receiver—a phenomenon that is not possible in practice. However, a periodic known pattern (preamble) can be injected at the beginning of each frame and is then used to perform many receiver adaptation tasks, including synchronization, channel equalization, AGC, and channel estimation. While this may appear useful for bursty traffic, it is definitely not efficient for continuous communication due to the overhead occupied by the preamble.

Indirect techniques use statistical parameters to estimate the SNR of the received signal, which proves as a good parameter to measure channel quality. Other methods are based on time diversity techniques (sending each sample twice) and comparing the two received samples. This trivial technique is adopted for this configurable transceiver because of its implementation simplicity with minor changes in the design. Although this technique suffers from a considerable overhead, it is considered as a simple example of circuit that monitors the wireless channel degradation and triggers the channel switching control system.

The decision to switch channels is made upon detecting N1 corrupted samples in row. The sample is considered corrupted when n bit errors are detected in a sample. Regardless, it is still possible to experience continuous switching between two channels. This may occur due to the fact that after switching channels, the receiver might experience a number of bit errors depending on the circuit transient state behavior. To avoid limit cycle behavior in the control circuit, two switching thresholds (high and low) are used, where the high threshold is equal to N1 and activates the channel switching task. This switching is performed just once and does not allow a switch back to the original channel with the exception of two cases:

- The error rate is below N2
- Reset manual switching button

The parameters N1, N2 and n are determined manually based on the sensitivity required for the channel quality monitor. In our configurable transceiver, n=2 bits, N1=6 and N2=3. The limitation of this channel switching controller is the lack of channel sensing system to recommend a vacant channel. Therefore, the channel switching circuit is limited to two predefined channels. The extreme case occurs upon switching to a noisy channel. Manual switching provides the ability to go back to the previous channel. However, it should be noted that this simple circuit is implemented to validate the channel switching mechanism. Reliable spectrum sensing is still an open problem and it is beyond the scope of this paper.

Figure 5 illustrates a simplified block diagram of the switching control circuit. Error detection is performed using an XOR gate between the two copies of the received samples, which are extracted from the serial-to-parallel converter. The number of bit errors is counted by passing XOR output serially to a counter. The bit error counter resets every 10 cycles (1 sample) and is synchronized with the serial-to-parallel stage. If the output is larger than n, the sample error counter stage increases. The symbol error counter output is captured every N1 samples, or 10xN1 cycles. The symbol counter resets upon receiving a correct sample. The output of the sample error counter is forwarded to a hysteresis relay with two thresholds. The...
relay is set when the number of sample errors is above \(N_1\). The relay is reset when the number of sample errors is lower than \(N_2\) or upon pressing the reset button. The relay output is passed to a toggle flip flop T-FF which switches between 1 and 0 on the rising edge of the relay output. T-FF controls a multiplexer which passes one of two carrier frequency values to the radio board controller.

**SWITCHING CONTROL DESIGN**

Online switching presents a challenge for software radio. In the proposed configurable transceiver, two modes of switching are presented; namely, manual switching between analog and digital modulation, and automatic switching between different communication channels. These challenges are listed as follows:

**Data Integrity During Switching Operation**

It is important to design a switching mechanism that protects the transmitted signal from loss or corruption during switching. This is achieved by buffering the data during the switching interval. Transmitter and receiver circular buffers are used to maintain data integrity during mode switching. The design of data buffering is shown in figure 6.

At the transmitter side, the circular buffer is placed after the VPSS port. The VPSS port provides a “ready” control signal subsequent to passing a new data word from DSP. This signal is connected to a write-enable port of the buffer. The switching control circuit provides a read-enable control signal when the switching operation is idle, and the buffer is not empty. If the buffer is full, a “full” control signal is passed from the buffer to shared memories (absent in figure 6) to notify the DSP that the transmitter is unable to transmit more data.

At the receiver side, the circular buffer is placed after the ADC. Similarly, the data converter provides a “ready” control signal subsequent to passing a new digitized sample (14 bits) from the analog domain. This signal is connected to a write-enable port of the buffer. The switching control circuit provides a read-enable control signal when the switching operation is idle, and the buffer is not empty. If the buffer is full, the received sample is dropped.

The switching control circuit regulates the switching mechanisms, whether switching between digital and analog or switching between different wireless RF frequencies. For the former, the command is received manually through a push button connected to a shared memory. Upon receiving the switching command, the switching control block passes inter-connection signals to the transmitter and receiver to connect the appropriate filters and signal processing stage to perform the digital or analog modulation. For the second switching mechanism, the circular buffer reading operation is ceased for a sufficient period of time to perform the switching operation. The buffer size is determined by the switching settling time.

**Synchronization**

Another challenge caused by switching is the loss of synchronization between the two communicating wireless nodes. This justifies choosing differential coding for digital modulators and single side band AM analog modulators. The SSB-AM demodulator is less sensitive to phase shifts in the analog modulation receiver than the coherent AM demodulator.

For coherent digital demodulators, there are two types of synchronization to be maintained: 1) phase/frequency synchronization; 2) symbol synchronization. The differential coding in DBPSK eliminates the need for phase synchronization at the expense of SNR degradation of 3 dB. Symbol synchronization can be replaced by a high oversampling ratio at the pulse shaping stage (8 samples).
Hence, the averaging mechanism using the “integrate and dump circuit” compensates a portion of performance degradation at the benefit of reducing the hardware complexity.

**Wireless Channel and Antenna Characteristics**

Automatic channel frequency switching, i.e. the frequency response of the wireless channel and antennas, serves as an additional design complexity. Wireless channels are band-limited, and their response varies among different RF frequencies. Propagation loss and multi-path characteristics are wireless channels properties dependant on carrier frequency. Operating over a wide range of frequencies requires the utilization of wide range antennas. SDR platform used is equipped with antennas that are optimized at the range of 450-490 MHz. Therefore, the two operating channels used for the current design fall within this range. In order to perform wider range operation, static gain scheduling, or AGC, is needed to control the signal level at the input of the analog-to-digital converter and to compensate the degradation in the antenna sensitivity outside its optimized operation range.

**CONCLUSION**

We have presented a configurable multimode transceiver using a hybrid software radio platform. A number of assumptions have been made throughout the design and implementation process. These include: the stability of the received level of the wireless signal so AGC implementation can be omitted; the consideration of the bit error rate as a sufficient wireless channel condition indicator, upon which a channel switching decision is made; and also perfect frame synchronization. While these assumptions are not necessarily typical, they were valid in order to build a proof-of-concept configurable wireless transceiver model.

The highlighted challenges in designing the mode switching control call for more complex system that is beyond the scope of pure physical-layer implementation. An important conclusion to note is the need of utilizing cross-layer design techniques to address problems that physical layers cannot overcome, including spectrum sensing and communication session negotiations, as well as channel condition evaluation. In future work, a cognitive element, which executes different operation management tasks (i.e. power management, spectrum sensing), will be applied to this configurable design. Hence, it is possible to build a cognitive radio that is capable of switching between different operation modes depending on battery power condition or channel traffic.

**REFERENCES**