A Novel Compression Method for Wireless Image Sensor Node

Xinkai Chen\textsuperscript{1}, Hanjun Jiang\textsuperscript{2}, XiaoWen Li\textsuperscript{1}, Zhihua Wang\textsuperscript{2}

\textsuperscript{1}Department of Electronic Engineering, Tsinghua University, Beijing, China
\textsuperscript{2}Institute of Microelectronics, Tsinghua University, Beijing, China

Abstract—This paper presents the design of a novel compression method for wireless image sensor node. In order to meet the requirement of the wireless image sensor node, a dedicated filtering procedure is developed for raw Bayer CFA pattern. JPEG-LS encoder follows the filtering procedure to compress the data. The parallel and pipeline structure are chosen for the purpose of high throughput and real-time operation. The compression method is implemented using UMC 0.18um technology. The test results shown that the image with VGA (640x480) resolution and frame rate 15 fps can be achieved with the same clock frequency with the CMOS image sensor.

I. INTRODUCTION

Distributed wireless sensor networks are expected to have widespread application within the coming age, ranging from military reconnaissance, environmental monitoring, object tracking and medical treatment assistant. Usually, the sensor nodes are deployed to sense the interesting physical phenomena with low data amount, such as temperature, humidity, pressure, vibration. These sensor nodes are of low data rate, low transmit bandwidth. However, recent advances in wireless communication, sensor and battery technology have made it possible to implement low-cost, low-power wireless image sensor node [1][2][3][4].

In general, a wireless image sensor node contains a CMOS image sensor, processing unit, wireless communication unit and power supply unit. It is usually deployed to capture images of the environment and transmit to the central. The characteristics and requirements of the wireless image sensor node are different from those sensor nodes that only need to sense simple physical phenomena [2].

- Due to the large amount of image data, high communication bandwidth is needed. But image sensor node has limited communication bandwidth. In order to reduce the requirement of high communication bandwidth, image compression need to be implemented at the node.
- The size of memory has to be considered. For example, if a frame of image has to be buffered for transmission, a 640x480 resolution Bayer pattern image with 8bits/pixel needs 300KB memory while an RGB mode image after interpolation needs 900KB memory. The requirement of large amount of memory is conflict with low-cost, small die size requirements. In order to reduce memory, image compression is necessary. However, the extra memory cost by compression has to be considered.
- Real-time operation is a requirement for image sensor network. For example, when intruder enters the monitoring area, image sensor node must real-time gather the image, fast process and transmit it. So, high speed image acquisition and processing is needed. In order to reduce the requirement of high communication bandwidth, image compression and partial image analysis need to be implemented at the node.
- Power consumption is a critical issue. Due to high transmission bandwidth, radio communication will constitute a significant fraction of the device’s total energy budget during active operation [2]. So the reduction of power of RF subsystem is the key issue for the low power consideration. A basic idea is using localized image compression to reduce the stream of data being generated by image sensor. The processing of image is far more complex than processing simple physical information, such as temperature and pressure. Thus, higher clock frequency is needed for the real-time image processing which cause higher power consumption. We must make sure the power consumed by the image compression is less than the saving power of radio communication.
- Medium image resolution and high image quality is needed for some applications. For example, military reconnaissance and medical treatment assistant usually acquire high quality images for monitoring physical situation. For medical application, the loss in the image quality could be a chance of missing diagnose. Thus, the detail of the medical image should be kept for some applications.

Based on the above consideration, we propose a low complexity lossless compression method. The remainder of the paper is organized as follows. In section II, we describe the algorithm of our proposed image compression method for wireless image sensor node. The detail VLSI architecture...
II. PROPOSED COMPRESSION METHOD

Our proposed compression method is dedicated developed for CMOS image sensor based on Bayer color filter array format. Bayer color filter arrays (CFA) is a popular format for the CMOS image sensor. The pattern of the color filter is shown in Figure 1. When the image sensor is read out line by line, the pixel sequence comes out GR repeatedly, and then the alternate line sequence is BG. This output is called sequential RGB.

For each single pixel, it contains only one component of three RGB color data. In order to obtain the other two components, a required image-processing step for Bayer pattern sensor is interpolation, during which the missing color components are estimated from neighboring pixel data. However, the interpolation causes the increase of the size of a frame of image in 3 times which is unacceptable in a wireless communication system. So, the raw Bayer CFA data without interpolation has been used in our proposed system and compression algorithm.

A problem with raw Bayer CFA data is a pixel and its neighboring pixel always belong to different color components, as shown in Figure 1. So the correlation between two neighboring pixels is very low and the influence of high spatial frequencies is extremely notable. Therefore, either based on prediction (DPCM) or on transformation (DWT), the lossless/near-losses algorithms suffer from a severe degradation of compression performance. In our proposed method, a dedicated filtering procedure is developed for raw Bayer CFA pattern to alleviate this problem, in which the data are firstly transformed and low-pass filtered directly in RGB space to depress the high spatial frequencies. After that, the result data are sent to JPEG-LS encoder for compression. JPEG-LS is chosen for compression not only because of its outstanding performance, but also because of its low complexity, low storage requirement which makes it ideal for a low power hardware implementation. Finally, the result data is transmitted to the base station. The recovered raw Bayer CFA data will be interpolated to generate a full image data on base station.

A. Filtering

The filtering procedure includes two kinds of operation, transformation and low-pass filtering. By transformation operation, G component and B&R components are separated into two rectangular arrays. The high spatial frequencies between neighboring pixels due to different color component belonging are greatly decreased, from which relative high compression ratio can be derived by the JPEG-LS encoder.

In our proposed method, the B and R components are treated as the same color component. If the three color components are treated and processed individually as what have been done in [5], a higher compression ratio would be obtained because the contexts modeling of JPEG-LS would be more precise and the context of B, G and R would not be able to interact. However, large amounts of on-chip storage and power are needed while processing time is inevitably increased [9]. These disadvantages are unacceptable for a high performance VLSI implementation.

![Figure 1. Example of image filter operation](image)

The low-pass filtering procedure follows a raster scan sequence. Two filtering algorithm has been evaluated which can be described as the following two equations.

Method1:
\[
\begin{align*}
G'_{(m,n)} &= G_{(m,n)} + G_{(m-1,n)} + G_{(m,n-1)} + 1 \quad \text{and} \\
R'_{(m,n)} &= R_{(m,n)} + B_{(m-1,n)} + B_{(m,n-1)} \quad \text{and} \\
B'_{(m,n)} &= B_{(m,n)} + B_{(m-1,n)} + B_{(m,n-1)} + 1
\end{align*}
\]

Method2:
\[
\begin{align*}
G'_{(m,n)} &= G_{(m,n)} + G_{(m-1,n)} + G_{(m,n-1)} + 1 \quad \text{and} \\
R'_{(m,n)} &= R_{(m,n)} + B_{(m-1,n)} + B_{(m,n-1)} + 1 \quad \text{and} \\
B'_{(m,n)} &= B_{(m,n)} + R_{(m-1,n)} + B_{(m,n-1)} + 1
\end{align*}
\]

Where \((m, n)\) indicates the position of the pixel, G, B, R stand for the values of the raw Bayer CFA data while \(G', B', R'\) stand for the filtered value of the pixel. The performance of the two methods has been evaluated based on more than 1000 samples of practical images. Method 2 has been chosen for higher compression ratio. An exception window is introduced in the algorithm to avoid the error brought by low-pass filtering. The pixels in the exception window only perform transformation operation without low-pass filtering.

B. JPEG-LS Encoder

JPEG-LS is a low complexity high performance image compression algorithm which is suitable for wireless image sensor node. Its algorithm is composed of the following parts. [5] [10]

1) Control of JPEG-LS:
It controls the acquisition and storage of input filtered raw Bayer data as well as the storage of the compressed data.

2) Context decision:
Local gradient computation, quantization, quantized gradient merging and mode selection are implemented in this part.

3) Error prediction:
It implements predicting edge detection and correction from the bias as well as computing prediction error and modulo reduction of the prediction error in the regular mode.

4) Update variables:
   The variables are updated and saved in the corresponding buffers in this module.

5) Colomb coding:
   During Colomb coding process, the mapped prediction residual is encoded and the code word length limitation procedure is performed.

6) Run scanning and run length coding:
   It implements reading the Bayer image data and determining the run length as well as encoding the valued of the length.

III. VLSI ARCHITECTURE

Software implementation can be easily accomplished in the embedded processor in high flexibility. However, image compression is a more compute intensive task. Also the real-time and low power cannot be easily satisfied by software implementation. In the long term perspective, hardware implementation is the better choice for image sensor nodes.

A. Architecture of Image Filter

As mentioned in Section I, real-time operation is a requirement for wireless image sensor node. However, proper hardware structure has to be chosen to implement real-time operation under a low clock frequency. Thus, parallel structure that benefits high throughput is used for this purpose. Two identical filtering engines are in charge of G and B&R components separately under the control of Mode controller and filter controller, as shown in Figure 2. Each engine has two half-line buffers for storing the filtered results of the neighboring pixels. The pixels in the exception window will be stored in the buffers without low-pass filtering. The output of the two engines will be combined and sent to the following JPEG-LS encoder.

The clock frequency of image filter is the same with that of CMOS image sensor.

B. Architecture of JPEG-LS Encoder

Though JPEG-LS is easier for hardware implementation compared with many other compression algorithm, the implementation of JPEG-LS for high-speed applications is difficult due to the poor parallelizability in itself. In [6], a limited parallelism is obtained only when the computations do not depend on previous ones. In [7] and [8], more on chip memory and logic gates are sacrificed to exchange for higher processing rates. However, none of the three methods can realize real time data processing, and the methods in both [7] and [8] suffer from degradation of compression ratios.

In order to implement real-time operation, a full pipelined architecture is used in our proposed JPEG-LS encoder [9], as shown in Fig 4. It is composed of 4 parts.

1) Mode decision module. It selects a work mode (Regular, Run or Interrupt) for current pixel according to the preserved data.

2) Clock controller. It is in charge of generating and shutting down the clock of the other modules.

3) Parallel pipelines. Three parallel pipelines including regular pipeline, run pipeline and interrupt pipeline can achieve high processing speed by working simultaneously. Regular pipeline is used for encoding the pixels in Regular mode. In the first stage, fixed prediction value and context of the current pixel are calculated, the second stage is used to look up the context table, calculate the parameters for Golomb-Rice encoder, and update the context table. A Golomb-Rice encoder is implemented in the third stage with two outputs generated, indicating the code and its valid length respectively. Run length is encoded in run pipeline. Interrupt pipeline is similar to the regular pipeline except registers are used for context storage instead of SRAM.

4) Two-tier data packer. It converts variable length compressed data into fixed length data stream which is 32 bits in this design.

With the architecture, a real-time compression based on VGA resolution can be performed. 18k bits on-chip SRAM is used for JPEG-LS encoder.
IV. IMPLEMENTATION RESULT

To obtain the real metric of the performance, the proposed compression method has been verified on FPGA platform and fabricated in a 0.18 μm single-poly six-metal CMOS process with 50K logic gates. 10K bits SRAM is used for image filter while 19K bits SRAM for JPEG-LS encoder. The performance is shown in the table I and the layout is shown in Figure 7.

<table>
<thead>
<tr>
<th>Technology</th>
<th>UMC 0.18 μm IP6M CMOS Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Gates</td>
<td>50K (Not include memory)</td>
</tr>
<tr>
<td>Memory</td>
<td>29k bits on-chip SRAM</td>
</tr>
<tr>
<td>Die Area</td>
<td>2 mm x 1 mm</td>
</tr>
<tr>
<td>Power consumption</td>
<td>3.5 mW @ 15fps, VGA (640 x 480)</td>
</tr>
<tr>
<td>Power Supply</td>
<td>1.8V (core) 3.3V (I/O)</td>
</tr>
<tr>
<td>Throughput</td>
<td>15 fps can be reached with resolution 640 x 480 x 8 bits if 20MHz clock is employed.</td>
</tr>
<tr>
<td>Compression Rate</td>
<td>3 ~ 4</td>
</tr>
</tbody>
</table>

A demo system including a digital CMOS image sensor, a commercial RF transceiver and the test chip has been developed. The system is able to compressed raw Bayer CFA images with VGA resolution at frame rate 15fps under 20MHz clock Frequencies which is the same with the CMOS image sensor. The average compression rate of 3 ~ 4 can be achieved. The total power consumed by the system is 40mW when image acquisition and compression are performed; 12mW when transmitting is performed, as shown in Figure 5.

In order to measure the contribution of the proposed techniques to the whole system, we use the energy consumed by the demo system for transmitting a single frame of image as a metric. The normalized result is shown in Figure 7. Compared to the situation when image compression is disabled, 46% power reduction is achieved in our proposed system because the power consumed by RF transceiver is greatly reduced by image compression technique. The compression causes only 4% increase of the power of the digital part. Real-time operation reduces the size of transmitting buffer and processing time.

V. CONCLUSION

A low complexity lossless image compression method is developed for wireless image sensor node. A dedicated image filter and JPEG-LS encoder is employed in the method. The image with VGA resolution can be compressed at 15fps using 20MHz clock frequency.

REFERENCES