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Experimental investigation of self heating effect (SHE) in multiple-fin SOI FinFETs

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Abstract
In this work, the self-heating effect (SHE) on metal gate multiple-fin SOI FinFETs is studied by adopting the ac conductance technique to extract the thermal resistance and temperature rise in both n-channel and p-channel SOI FinFETs with various geometry parameters. It is shown that the SHE degrades by over 10% of the saturation output current in the n-channel and by over 7% in the p-channel. The extracted thermal resistances $R_{th}$ increase with the scaled down gate length, reducing the number of fin and shrinking the fin width. The temperature rise caused by the SHE increases with the scaled down gate length, increasing the number of fin and shrinking the fin width under the saturated operation condition. Additionally, due to a larger power density in the n-channel SOI FinFETs under the same bias condition, the temperature in the n-channel FinFETs is higher than that in the p-channel FinFETs. Because the Si thermal conductivity decreases as the temperature increases, $R_{th}$ is larger in the n-channel FinFETs than in the p-channel FinFETs. Therefore, tradeoffs have to be made between the thermal properties and the device’s electrical performance by careful design optimizations of SOI FinFETs.

Keywords: self-heating effect (SHE), FinFETs, silicon on insulator (SOI), thermal resistance

(Some figures may appear in colour only in the online journal)

1. Introduction

FinFETs are considered one of the most promising candidates for future generation transistor technologies due to their excellent electrostatic integrity (i.e. low leakage current, improved short-channel effect), high performance (resulting from the undoped channel structure and high carrier mobility) and reduction of random dopant fluctuation [1–4]. However, the use of a silicon on insulator (SOI) wafer and the narrow fin structure make the heat dissipation more difficult compared to the bulk Si device, which leads to the severe self-heating effect (SHE) [5]. Therefore, SOI FinFET structures may present significant challenges for circuit design [6].

Self-heating is caused by high electrical current density and poor thermal conductivity of materials such as SiO$_2$ and SiGe [7]. The scaling of device dimensions decreases heat dissipation capability and increases current densities, which further exacerbates the SHE. On the other hand, the thermal conductivity of 150 nm thickness buried oxide SiO$_2$ (BOX) used in SOI wafers is 0.9 W m$^{-1}$ K$^{-1}$ (bulk SiO$_2$ is 1.5 W m$^{-1}$ K$^{-1}$) [8], which is only one percent of the thermal conductivity of silicon (80 W m$^{-1}$ K$^{-1}$ at 150 nm thickness) [9]. BOX prevents heat dissipation to the substrate from the channel region and results in a high channel temperature. Self-heating not only causes output current degradation (resulting from mobility degradation and the threshold voltage shift) but also leads to serious reliability issues [10–12], such as degraded electromigration and temperature bias instability [13], which is due to the very high asymmetrical channel temperature.

So far, there have been only a few works that discuss the SHE in FinFETs. Makovejev et al [14] used the RF technique...
to extract the self-heating effect on SOI n-channel FinFETs by differing the fin width, fin spacing and number of fins. However, the device under test (DUT) in [14] has a ploy-Si gate stack, and the impact of the gate length and p-channel devices have not been studied. The metal-gate stack has now become the mainstream technology for device fabrication to improve device performance. A metal gate layer can induce a high strain in a channel to enhance channel mobility and avoid the poly-Si depletion effect compared to the poly-Si gate stack. Therefore, the SHE in metal-gate stack FinFETs needs to be investigated. In this paper, the ac conductance technique is adopted to characterize the SHE in SOI FinFETs with a metal gate stack. The extracted thermal resistance and temperature with different device geometry parameters, including gate length, fin width and the number of parallel fins, are comprehensively discussed. The thermal resistance between n-channel and p-channel SOI FinFETs are compared to provide insight for a thermal-aware FinFET-based technology and circuit design.

2. Experimental

FinFETs were fabricated on (100) SOI wafers with 150 nm thick BOX [15, 16]. The fin height is 58 nm, the fin spacing is 200 nm and the fin width varies from 20 to 35 nm. The gate dielectric is 2 nm SiO2 grown by in situ steam oxidation at 975 °C. A 7 nm thin TiSiN was used for the metal gate and deposited by low pressure chemical vapor at 600 °C, followed by the poly-Si gate deposition as the gate contact. The Si channel is undoped (with its intrinsic concentration as $2 \times 10^{15}$ cm$^{-3}$). The gate length varies from 90 nm to 5 um. Fin array structures with numbers of fins from 2 to 50 are studied herein to fully evaluate the impact of the SHE. The device structure is illustrated in figure 1, and the critical device parameters are listed in table 1.

In order to assess the SHE in different device geometry parameters, the ac conductance technique has been utilized [17]. It is convenient for the ac conductance technique to measure the drain-to-source conductance ($g_{ds}$) at a proper frequency range. The $g_{ds}$ was measured by Agilent 4294A with the gate biased by Agilent 4156C, as shown in figure 2. Considering the parastics from the measurement set-up and the DUT, all of the $g_{ds}$ values were obtained at 1 MHz. Although the measurement frequency is not high enough to entirely decouple the SHE, the same measurement condition can still be adopted for evaluating the impact of device geometry parameters in the SHE [18]. The ac $g_{ds}$ and DC $g_{ds}$ (the differential of $I_{ds}$ vs. $V_{ds}$) are shown in figure 3. The ac $g_{ds}$ is larger than DC $g_{ds}$ since the ac measurement partially

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>$L_g$</td>
<td>gate length</td>
<td>90/110/250/500/1000/5000 nm</td>
</tr>
<tr>
<td>$N_{Fin}$</td>
<td>Number of parallel fins</td>
<td>2/6/8/20/30/50</td>
</tr>
<tr>
<td>$W_{Fin}$</td>
<td>Fin width</td>
<td>20/25/35 nm</td>
</tr>
<tr>
<td>$H_{Fin}$</td>
<td>Fin height</td>
<td>58 nm</td>
</tr>
<tr>
<td>$L_{Spacing}$</td>
<td>Fin spacing</td>
<td>200 nm</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>Gate dielectric SiO2 thickness</td>
<td>2 nm</td>
</tr>
<tr>
<td>$t_{BOX}$</td>
<td>Buried oxide SiO2 thickness</td>
<td>150 nm</td>
</tr>
</tbody>
</table>

Figure 1. Multiple-fin SOI FinFETs’ device structure.

Figure 2. AC conductance technique measurement set-up.

Figure 3. AC conductance technology measurement of the $g_{ds}$ conductance at 1 MHz (Close) and the DC $I_{ds}$-$V_{ds}$ differential conductance (Open).
suppresses the SHE, as expected. The $I_{ds}-V_{ds}$ without the SHE can be extracted by integrating $g_{ds}$ over the drain voltage. The $I_{ds}-V_{ds}$ characteristics with/without the SHE are shown in figure 4. The SHE degrades the $I_{ds}-V_{ds}$ severely at the saturation operation condition ($V_{gs} = V_{ds} = 1.5\, \text{V}$).

3. Results and discussion

To investigate the impact of the FinFETs’ geometry parameters and channel dopant type on the SHE, the saturation output current with/without the SHE and the thermal resistances are extracted using the ac conductance technique for the n-channel and p-channel SOI FinFETs of different gate lengths and for different numbers of parallel fins and fin widths. The temperature rise caused by the SHE has been extracted and will be discussed in the following section.

3.1. Self-heating effect on $I_{ds}$

Considering the confined fin structure and the low thermal conductivity of the SOI substrate, the impact of the SHE on SOI FinFETs is worse than a planar bulk MOSFET. The high temperature caused by the SHE reduces the carrier saturation velocity and mobility, according to [17]:

$$\mu_{\text{eff}} = \mu_{\text{eff(0)}} \left(\frac{T}{T_0}\right)^{-2}$$

where $\mu_{\text{eff}}$ is the effective mobility at a temperature of $T$, $\mu_{\text{eff(0)}}$ is the effective mobility at ambient temperature, $T$ is the average channel temperature and $T_0$ is the ambient temperature. The reduced mobility directly influences the output current characteristic. The output current without the impact of the SHE extracted by the ac conductance technique is shown in figure 4. The effect of the SHE on the saturation output current can be defined in equation (2):

$$\eta = \frac{I_{ds,\text{w/o SHE}} - I_{ds,\text{w/SHE}}}{I_{ds,\text{w/o SHE}}} \times 100\%$$

where $I_{ds,\text{w/o SHE}}$ is the saturation output current without the impact of the SHE, $I_{ds,\text{w/SHE}}$ is the saturation output current with the impact of the SHE and $\eta$ represents the rate of the saturation output current degradation by the SHE.

The rate of the saturation output current degradation caused by the SHE as a function of gate length is shown in figure 5. The degradation rate increases as the gate length scales down. When the gate length reduces to 90 nm, the degradation rate of the n-channel device is over 10%, and the degradation rate of the p-channel is above 7%. This behavior is usually attributed to mobility reduction with the increasing channel temperature, according to equation (1), while other thermal influences are neglected. It is obvious that the impact of the SHE on the output current is serious and cannot be neglected. Additionally, the degradation is not identical for the n-channel and p-channel FinFETs, which will pose challenges in the circuit design.

3.2. Thermal resistance

According to the output current characteristic with/without the SHE, the thermal resistances ($R_{th}$) were extracted by the equation:

$$R_{th} = \frac{I_{ds,\text{w/o SHE}} - I_{ds,\text{w/SHE}}}{I_{ds} \cdot V_{ds} \cdot \partial I_{ds}/\partial T}$$

where $I_{ds,\text{w/o SHE}}$ represents the saturation output current without the effect of the SHE, $I_{ds,\text{w/SHE}}$ is the saturation output current with the effect of the SHE. $\partial I_{ds}/\partial T$ represents the saturation output current as the change of the ambient temperature.

To extract thermal resistances in equation (3), the dependence of the drain current on ambient temperature $\partial I_{ds}/\partial T$ must be measured. This dependence is obtained from the
linear fitting of the hot chuck current measurement. Figure 6 shows the saturation output current dependence on the chuck temperature with a different number of fins. The degradation gets more serious with the increasing number of parallel fins at the same temperature condition.

The rising temperature determined by the power and thermal resistance is shown in equation (4) [9]:

$$\Delta T = R_{th} \times P = R_{th} \times (I_s \cdot V_d) \quad (4)$$

The larger thermal resistance $R_{th}$ with the same power $P$ generates a higher temperature. Therefore, thermal resistance $R_{th}$ can work as a standard to assess the SHE.

3.2.1. Gate length dependence. The thermal resistances $R_{th}$ of the n-channel and p-channel SOI FinFETs as a function of the gate length are shown in figure 7. The gate length varies from 90 nm to 5 μm. As the gate length scales down, the thermal resistance $R_{th}$ increases gradually. The gate length scales to sub-100 nanometers, which becomes comparable to the phonon mean free path (approximately 200–300 nm in undoped bulk silicon at room temperature [19]). This leads to sub-continuum transport effects [20], resulting in a rapid increase of thermal resistance $R_{th}$. The small region of the high electric field near the drain gives rise to a strongly localized hot spot. The hot spot is only in the range of tens of nanometers and has a higher temperature than those predicated by the classic diffusion theory [21, 22]. The extracted temperature and the measured current $I_s$ under the saturation condition ($V_{gs} = V_{ds} = 1.5$ for the n-channel, $V_{gs} = V_{ds} = -1.5$ for the p-channel) dependence on the gate length are shown in figure 8. The temperature increases as the gate length scales down. When the gate length reduces to less than 500 nm, the temperature rises quickly.

The thermal resistance $R_{th}$ and the temperature rise of the n-channel SOI FinFETs are larger than those of the p-channel in all of the length scales. The reason for this is that the power of the n-channel is larger than the p-channel, leading to a higher temperature in the n-channel SOI FinFETs. Considering the temperature effect on thermal conductivity, the higher temperature of the material has lower thermal conductivity [23]. Therefore, the thermal conductivity of the n-channel is smaller than that of the p-channel under the same saturation condition, resulting in larger thermal resistance in the n-channel SOI FinFETs.

3.2.2. Number of the parallel fins’ dependence. In order to improve the output capability of transistors, the parallel fin structure was studied. Figure 9 shows the fluctuations of thermal resistance $R_{th}$ with respect to the fin number in the n-channel and p-channel SOI FinFETs induced by the fabrication process. FinFETs with small parallel fin numbers ($N_{Fin} = 2, 6, 8$) have large fluctuations of thermal resistance $R_{th}$. For FinFETs with large parallel fin numbers ($N_{Fin} = 20, 30, 50$), the statistical fluctuations of $R_{th}$ are minimized. The average values of those samples at different fin numbers are illustrated in figure 9. In order to ensure the reasonable and valid value of the extracted thermal resistance with respect to different fin numbers, we selected the sample that is close to the average value. The final results are shown in figure 10.
Figure 10 shows the extracted thermal resistance $R_{\text{th}}$ with the number of parallel fins per gate in the n-channel and p-channel SOI FinFETs. As the number of parallel fins increases, the extracted thermal resistance $R_{\text{th}}$ decreases. The main reason for this is that the device with the higher number of parallel fins has a larger cross-sectional area, which has a better heat dissipation capability. The tendency of the thermal resistance $R_{\text{th}}$ with respect to the fin number is similar with the simulation results in [24]. However, the temperature caused by the self-heating effect rises with the increasing the number of fins under the same saturation bias condition, shown in figure 11, because FinFETs with the higher number of parallel fins have higher power ($I_{\text{ds}}V_{\text{ds}}$) under the same saturated condition. When the number of fins reaches 20, the thermal resistance $R_{\text{th}}$ trends to stable. Therefore, the temperature caused by the SHE would reach a constant value with the increasing number of parallel fins, which is consistent with the simulation results carried out by Swahn et al [25]. The thermal resistance $R_{\text{th}}$ and temperature rise of the SOI n-channel FinFETs are larger than those of the p-channel for different numbers of parallel fins.

3.2.3. Fin width dependence. Figure 12 shows the extracted thermal resistance $R_{\text{th}}$ as a function of fin width in the n-channel and p-channel FinFETs. The extracted thermal resistance increases with the shrinking fin width. The reason for this is that the narrow fin structure enhances the phonon boundary scattering, thus resulting in large thermal resistance. The extracted temperature dependence on the fin width is shown in figure 13. The temperature rises as the fin width shrinks. The larger fin width device presents better thermal properties. Those results indicate that the improved electrostatic control and higher integration density achieved by shrinking the fin width is compromised by increasing the thermal resistance. The thermal resistance $R_{\text{th}}$ and temperature rise of the n-channel SOI FinFETs are higher than those of the p-channel in different fin width conditions.
n-channel and p-channel FinFETs.

Acknowledgements

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Figure 13. The extracted temperature as a function of fin width in the n-channel and p-channel FinFETs.

4. Conclusion

In this paper, the ac conductance technique has been adopted to determine the SHE and thermal resistance in both n-channel and p-channel multiple-fin metal gate SOI FinFETs of various geometries. It is found that the SHE degrades the output characteristic severely under the saturation operation condition. The extracted thermal resistances $R_{th}$ increase with the scaled down gate length, reducing the number of parallel fins and shrinking the fin width. The extracted thermal resistances $R_{th}$ and temperature rise of the p-channel SOI FinFETs are lower than those of the n-channel with the same device geometry. An increase of the fin width leads to improved thermal properties of the devices. However, it compromises the layout efficiency and electrostatic integrity of the FinFETs. Therefore, tradeoffs have to be made between the thermal properties and the electrical performance of the device during the design optimization of SOI FinFETs.