Intrinsic current gain cutoff frequency of 30 GHz with carbon nanotube transistors

A. Le Louarn, F. Kapche, J.-M. Bethoux, H. Happy,[a] and G. Dambrine
Institut d'Electronique, de Microélectronique et de Nanotechnologie, UMR-CNRS 8520, BP 60069, Avenue Poincaré, 59652 Villeneuve d'Ascq Cedex, France

V. Derycke, P. Chenevier, N. Izard, M. F. Goffman, and J.-P. Bourgoin
Service de Physique de l'Etat Condensé (CNRS URA 2464), DSM/DRECAM/SPEC, CEA Saclay, 91191 Gif sur Yvette Cedex, France

(Received 24 January 2007; accepted 3 May 2007; published online 5 June 2007)

High frequency capabilities of carbon nanotube field-effect transistors (CNTFETs) are investigated. Structures with a large number of single-walled carbon nanotubes were fabricated using dielecrophoresis to increase the density of nanotubes in the device channel. The authors obtained an intrinsic current gain cutoff frequency of 30 GHz establishing state-of-the-art high frequency (hf) potentialities of CNTFETs. The device also showed a maximum stable gain above 10 dB at 20 GHz. Finally, the parameters of an equivalent circuit model of multitube CNTFET at 20 GHz are determined, which open the route to the modeling of nanotubes-based hf electronics.
 [DOI: 10.1063/1.2743402]

The intrinsic electrical properties of carbon nanotubes (CNTs) are among the best of all the semiconductors, and carbon nanotube field-effect transistors (CNTFETs) are known to be very promising for high frequency electronics.[1–4] Recent works[4–9] have demonstrated high frequency functionalities of CNTFETs up to tens of gigahertz. While most of the studies so far used indirect methods (such as mixing[4]) to assess the high frequency (hf) properties of the devices, only a few studies used direct measurement techniques[3,6–8,10] and were able to demonstrate current or maximum stable gain (MSG) up to 10 GHz. In these studies several routes for continuous improvement of the high frequency performances were envisaged. They include optimizing the device geometry, using multichannel configurations or increasing the number of gate fingers. Nevertheless, the measured performances remain far from the predicted intrinsic capabilities of CNTs, in particular, in terms of cutoff frequency.[2,11]

An interesting figure of merit to compare and optimize the high frequency potentialities of a transistor is the gate delay defined as CV/I.[12] This expression illustrates the key elements to improve the performances: increasing the drive current (at a given drain-source bias) and decreasing the capacitance. In the case of nanodevices the current per channel (defined by the quantum conductance $2e^2/h$, taking into account the spin) does not exceed a few tens of microamperes. This intrinsic limitation together with parasitic capacitances even of a few femtofarads decreases the intrinsic cutoff frequency by decades and is the main bottleneck in terms of speed. These parasitic capacitances originate from pads, gate-to-source and gate-to-drain overlaps, and electrodes fringing. The negative contribution of these parasitic capacitances can be lowered principally by improving the device geometry. Increasing the current through the device may be possible using two approaches: increasing the number of gate fingers[3,13] or increasing the density of nanotubes for a given device geometry which may prove a better compromise. Using multigate fingers definitely results in a higher drive current which improves the measurement's accuracy by allowing more convenient impedance with respect to conventional 50 Ω equipment. However, most of the parasitic capacitances increase at the same time which may limit the ultimate performance obtained by this approach. Conversely, increasing the nanotube density in a given geometry can also strongly improve the drive current while keeping the parasitic capacitances to an almost unaffected level. This latter approach is the one explored in this work. To prove the dependence of nanotube density on hf performance, we have fabricated *p*-type CNTFETs with a high density of nanotubes per gate finger using the dielectophoresis technique for CNTs deposition.[14,15]

The cross section of the device under consideration is presented in Fig. 1. It is a metallic (Al) back-gate-oxide (Al_2O_3, about 2 nm) CNTFET with a two-gate-finger topology. The unitary gate finger width is 10 μm, the source to drain spacing is 300 nm, and the gate overlaps the source and drain regions by 50 nm. Pd is used to contact nanotubes as it is known to favor hole injection.

The process flow is similar to the one described in Ref. 6 except for the nanotubes deposition technique. Before the deposition of nanotubes, the metallic gate fingers, the gate oxide, and the access electrodes are fabricated. Then, the

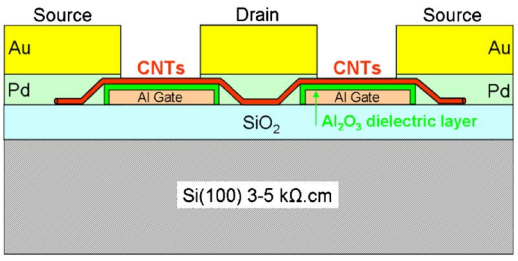

FIG. 1. (Color online) Cross-sectional representation of the CNTFET. Aluminum is used as a back gate, and a thin (about 2 nm) Al_2O_3 layer gate insulator is obtained by plasma.

[a]Author to whom correspondence should be addressed; electronic mail: henri.happy@iemn.univ.-lille1.fr

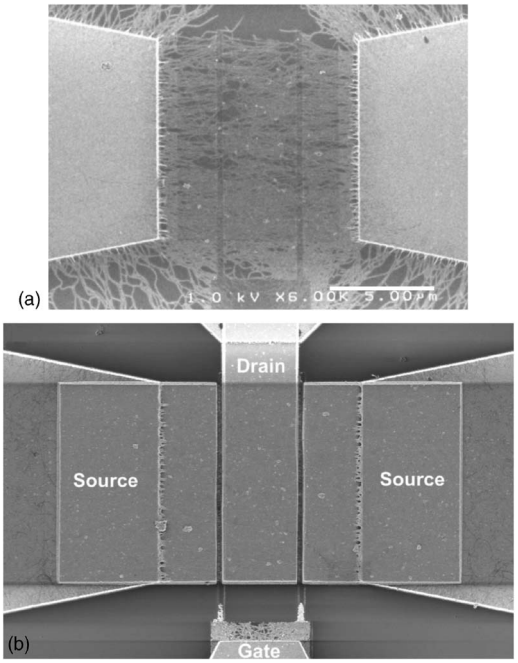

FIG. 2. Scanning electron microscopy (SEM) images of the two-finger back-gate CNTFET active region: (a) after the dielectrophoresis process and (b) at the end of the process.

nanotubes are deposited and the final step consists in connecting the nanotubes to source and drain electrodes by metal (Pd) deposition. In our previous work, nanotubes were deposited at the wafer scale using a selective deposition technique based on surface chemistry.[16–18] This yielded a nanotube density of ~10 NTs/μm of gate width. In the present study, we use the dielectrophoresis (DEP) approach. Nanotubes from Nanoledge were first purified and dispersed at low concentration in *N*-methyl-pyrrolidone using moderate sonication. These results in a highly stable dispersion comprising mostly individual nanotubes. A droplet of this dispersion is deposited on the wafer where the gate fingers, pads, and access electrodes have already been patterned. An ac electric field is applied between the access electrodes of the future source contacts separated by 8.5 μm. This electric field drives the deposition of the nanotubes. An important aspect of this technique is that not only the deposition can be made very dense but it also results in nanotubes preferentially oriented along the field lines. Figure 2(a) shows a scanning electron microscopy (SEM) image of the active area after the DEP process. It is clear that the method results in a highly dense, mostly oriented and two dimensional nanotube film. The very thin thickness of this film (a couple of nm corresponding to a monolayer mainly) is important since thick films would result in limited coupling to the gate due to the intertube screening. It is also clear from this figure that a large number of nanotubes are deposited outside the active area. This is due to the presence of the gate and drain access electrodes which are at a floating potential during the deposition. These undesirable CNTs are destroyed by plasma oxidation through a mask. Figure 2(b) shows the final active region after the source and drain electrodes have been patterned.

While it is difficult to assess directly the nanotube density, we note that the prepared devices show drive currents in the 15–30 mA range at V_{ds}=1.5 V (see the typical $I_{ds_{tot}}(V_{ds})$ curves in the inset of Fig. 3, for example), which is ~10–20

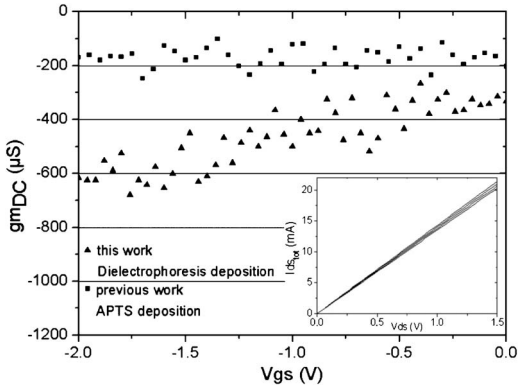

FIG. 3. Measured dc transconductance (gm) as a function of V_{gs} at V_{ds}=1 V in comparison with the previous work (see Ref. 6). Inset: $I_{ds_{tot}}$ as a function of V_{ds}, for V_{gs} from −1.5 to 0 V (step of 0.5 V).

times higher compared to our previous study at a comparable geometry.[6] The major part (90%–95%) of the dc is produced by the large number of metallic nanotubes. Nevertheless, the dielectrophoresis technique allows increasing also the semiconductor nanotubes. As shown in Fig. 3, the dc transconductance, close to −500 μS, is improved by a factor of 2.5 (at V_{gs}=−1.5 V) as compared with our previous work.[6] On-wafer *S*-parameter measurements were carried out using an Agilent PNA series network analyzer from 50 MHz to 20 GHz. The i.f. bandwidth is fixed at 10 Hz to improve the sensitivity and accuracy of the measurements. The current gain $|H_{21}|^2$ and MSG $|S_{21}/S_{12}|$ were deduced from measured *S* parameters and are shown in Fig. 4. The current gain cutoff frequency (f_T) of the total device H_{21_ext} (device with access) is close to 4 GHz (it should be noted that f_T~11 GHz when the coplanar pads are removed). It is almost four times greater than the previous result,[6] using the same structure. Moreover, using the deembedding procedure described in Refs. 6 and 7, we removed by calculation the access and parasitics using a dedicated "open" structure (similar to the active structure but without nanotubes). The main parasitic capacitances are highlighted by the gate-to-source and gate-to-drain overlap capacitances C_{gsp} and C_{gdp} close to 10 fF. These capacitances are directly extracted from the measured *S* parameters of the open structure. As shown in Fig. 4, the intrinsic current gain (H_{21_int}) cutoff frequency

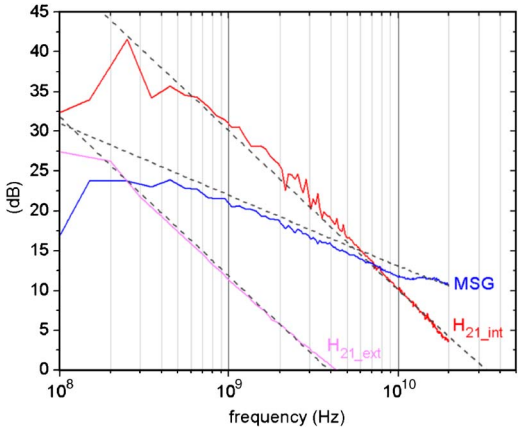

FIG. 4. (Color online) Current gain 10 log 10($|H_{21}|^2$) and MSG (in decibels) extracted from the *S* parameters. The device is biased at V_{ds}=1.5 V and V_{gs}=−2 V. MSG=10 dB at 20 GHz. The dashed lines correspond to the ideal slopes of −20 dB/decade for $|H_{21}|$ and −10 dB/decade for MSG.

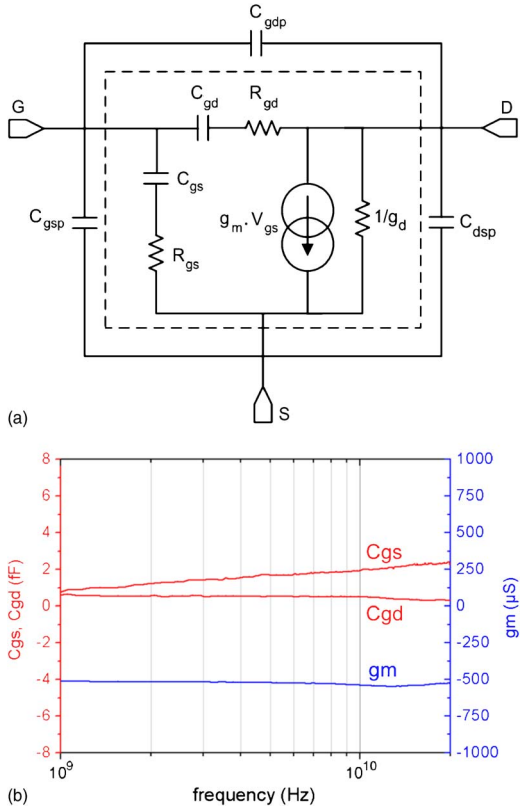

FIG. 5. (Color online) (a) Equivalent circuit for modeling CNTFET. Intrinsic components are displayed inside the dashed rectangle. (b) ac transconductance and intrinsic gate-to-source and gate-to-drain capacitances C_{gs} and C_{gd} extracted from the deembedded S parameters. The device is biased at $V_{ds}=1.5$ V and $V_{gs}=-2$ V.

after such a deembedding procedure is of 30 GHz. This result shows the high frequency potentialities of CNTFETs in the centimeter wave range and corresponds to the state of the art. For the same bias point, the MSG is greater than 10 dB at 20 GHz. It should be noted that the slopes of the current gain and MSG are −20 and −10 dB/decade, respectively, in the whole frequency range. It corresponds to the expected ideal slopes and proves the quality of the deembedding procedure.

From the S parameters, we also deduced the elements of the equivalent circuit described in Fig. 5(a). All values are summarized in Table I. Figure 5(b) represents the evolution of the ac transconductance and of the intrinsic gate-to-source and gate-to-drain capacitances as a function of frequency. The order of magnitude of these intrinsic capacitances is close to 1 fF. In terms of accuracy, such a value is very sensitive to the deembedding procedure (taking into account the parasitic capacitances) and one should be cautious when trying to relate them to a physical origin. Nevertheless, we note that the intrinsic capacitances are extracted directly from the intrinsic Y parameters ($Y_{int}=Y_{measured}-Y_{open}$) without any added correction and are always positive even if they are very small which proves the efficiency of the deembedding technique. These intrinsic parameters remain constant up to 20 GHz. The dynamic gm value is comparable to the dc ones (~500 μS), denoting the low values of source and drain resistances, thanks to the high number of CNTs.

TABLE I. Elements of the equivalent circuit described in Fig. 5 and deduced from the S parameters.

$C_{gsp}=9$ fF	$C_{gs}=2$ fF	$R_{gd}=10$ kΩ
$C_{gdp}=10$ fF	$C_{gd}=0.3$ fF	gm=−0.52 mS
$C_{dsp}=2.7$ fF	$R_{gs}=1$ kΩ	gd=15.2 mS

While these results present the state of the art in terms of intrinsic f_T and MSG, we were expecting higher performance. Indeed, the high value of the conductance (gd ~ 15 mS) denotes the high density of deposited CNTs in agreement with the SEM images. Although the high value of the transconductance as compared with previous works, the ratio gm/gd is very low close to 0.03. These relative values of gd and gm indicate that a large part of the deposited nanotubes is metallic. More investigations and optimizations of the nanotubes deposition technique particularly are still necessary to reach transistors operating in microwave or even millimeter-wave electronics. hile limiting the performances of the present devices, this also indicates that highly improved hf capabilities are in sight in the proposed geometry. Using dispersions of nanotubes enriched in semiconducting tubes[19] should bring the f_T towards the 100 GHz range.

The authors acknowledge support by french ANR under Contract No. ANR-2005-055 HFCNT.

[1] D. J. Frank and J. Appenzeller, IEEE Electron Device Lett. **25**, 34 (2004).
[2] P. J. Burke, Solid-State Electron. **48**, 1981 (2004).
[3] S. Kim, T.-Y. Choi, L. Rabieirad, J.-H. Jeon, M. Shim, and S. Mohammadi, *IEEE International Microwave Symposium Digest* (IEEE, New York, 2005), p. 4.
[4] S. Rosenblatt, H. Lin, V. Sazoneva, S. Tiwari, and P. L. McEuen, Appl. Phys. Lett. **87**, 153111 (2005).
[5] S. Li, Z. Yu, S.-F. Yen, W. C. Tang, and P. J. Burke, Nano Lett. **4**, 753 (2004).
[6] J.-M. Bethoux, H. Happy, G. Dambrine, V. Derycke, M. Goffman, and J.-P. Bourgoin, IEEE Electron Device Lett. **27**, 681 (2006).
[7] J.-M. Bethoux, H. Happy, A. Siligaris, G. Dambrine, J. Borghetti, V. Derycke, and J.-P. Bourgoin, IEEE Trans. Nanotechnol. **5**, 335 (2006).
[8] J.-M. Bethoux, H. Happy, G. Dambrine, V. Derycke, M. Goffman, and J.-P. Bourgoin, Mater. Sci. Eng., B **135**, 294 (2006).
[9] Z. Yu, C. Rutherglen, and P. Burke, Appl. Phys. Lett. **88**, 233115 (2006).
[10] X. Huo, M. Zhang, P. C. H. Chan, Q. Liang, and Z. K. Tang, *IEEE IEDM Technical Digest* (IEEE, New York, 2004), p. 691.
[11] L. C. Castro and D. L. Pulfrey, Nanotechnology **17**, 300 (2006).
[12] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, and M. Radosavljevic, IEEE Trans. Nanotechnol. **4**, 153 (2005).
[13] D. Akinwande, G. F. Close, and H.-S. P. Wong, IEEE Trans. Nanotechnol. **5**, 599 (2006).
[14] R. Krupke, S. Linden, M. Rapp, and F. Hennrich, Adv. Mater. (Weinheim, Ger.) **18**, 1468 (2006).
[15] A. R. Boccaccini, J. Cho, J. A. Roether, B. J. C. Thomas, E. J. Minay, and M. S. P. Shaffer, Carbon **44**, 3149 (2006).
[16] K. H. Choi, J.-P. Bourgoin, S. Auvray, D. Esteve, G. S. Duesberg, S. Roth, and M. Burghard, Surf. Sci. **462**, 195 (2000).
[17] E. Dujardin, V. Derycke, M. F. Goffman, R. Lefèvre, and J.-P. Bourgoin, Appl. Phys. Lett. **87**, 193107 (2005).
[18] S. Auvray, V. Derycke, M. Goffman, A. Filoramo, O. Jost, and J.-P. Bourgoin, Nano Lett. **5**, 451 (2005).
[19] M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, Nature Nanotechnol. **1**, 60 (2006), and references therein.