STIMULUS GENERATION FOR BUILT-IN SELF-TEST OF CHARGE-PUMP PHASE-LOCKED LOOPS

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Abstract - This paper addresses the issue of the stimulation of charge-pump phase-locked loops for built-in self-test applications. It is shown that three nodes of the PLL qualify for test signal injection. The hardware and methodology for each are discussed. In particular, a comprehensive explanation of the use of delta-sigma modulation in the time domain is provided. Furthermore, implementation issues of analog tests with signal generation based on coarse quantization are discussed. The effects of the quantization noise arising from delta-sigma modulation on the dynamic range of phase-locked loop nodes is evaluated. Original experimental results validate one of the methods which was not verified previously. In conclusion, the strengths and weakness of each of the three methods for phase-locked loop stimulation are highlighted.

I. Introduction

The traditional procedure for testing an analog device is to apply a signal at the input and measure the output response. For example, to obtain the frequency response of a filter, a sinewave is used to stimulate the circuit and the amplitude and phase of the output signal are evaluated. However, testing an arbitrary analog device may be very expensive. The signal sources and the measuring instruments can be complex, notably for phase-locked loops (PLL) [1]. Thus, methods for characterizing this device on a test bench may not be directly ported on-chip. Unfortunately, the test circuitry would be very sensitive to process variations, requiring a significant test effort themselves, and the area overhead would be too large. Yet, for circuits based on a negative feedback loop such as a PLL, other options are available for test stimulus and measurement. In fact, because of the loop dynamics, a test signal may be injected at any point and stimulate the whole circuit.

Similarly, the circuit response could be measured at many nodes. The only method proposed so far for measurement is the comparison of the observed signal with the rising edges of a reference signal for the purpose of establishing magnitude relations between the output jitter and discrete jitter values. This technique has been labelled jitter threshold [2]. While this method is simple, it shifts the complexity to the signal generation part of the test problem. The signal source must be capable of a wide variety of signal amplitudes and frequencies. Furthermore, noise and distortion will adversely affect test results.

This paper explores the three methods for generating a stimulus suitable for a PLL. The model of the PLL will be studied systematically as each circuit node will be examined for stimulus injection. It will be demonstrated that three nodes are suitable for this purpose. Strategies for two of these test signal injection methods have already reported in previous papers [2,3]. Each proposition will be evaluated for its amenability to built-in self-test (BIST). Explicitly, signal sources must have four essential characteristics to qualify for on-chip integration. First, circuits which require calibration using off-chip analog instruments should be avoided. Otherwise, the test of the PLL with external instruments is merely replaced by a similar effort to calibrate the signal source. Also, the silicon area required for the source implementation should be relatively small when compared to the device under test. Finally, the signal source should also provide sufficient accuracy and offer some degree of programmability.

Section II introduces the PLL model and then analyzes systematically all the nodes for the possibility of test signal injection. Section III discusses the use of the input terminal for this purpose. The principle of delta-sigma (ΔΣ) modulation in the time domain is also introduced. This concept is further used in Section IV for the presentation of the second test stimulus method, modulation of the PLL feedback. The topic of Section V is the injection of a test signal using an extra charge pump. Section VI then examines the effects of using ΔΣ-based signal generation on the operation of the device-under-test (DUT). Experimental results of the PLL feedback modulation method

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will be disclosed in Section VII. Finally, conclusions are drawn where the advantages and limitations of each test signal injection method are listed.

II. Charge-Pump Phase-Locked Loops

Fig. 1 illustrates the continuous-time model of a PLL. To the left are the phase detector (PD) and charge pump (CP) whose combination is modeled by a summer and a gain stage. They are followed by the loop filter which has a transfer function denoted \( G(s) \). The right most block is the voltage-controlled oscillator (VCO). A counter of length \( N \), modeled as a scaling operation with gain \( 1/N \), may be present in the feedback loop. The four possible nodes for test signal injections are labeled with the variables \( \theta_i(s) \), \( \theta_i(s) \), \( \theta_i(s) \) and \( \theta_i(s) \). While the input and output variables, \( \theta_i(s) \) and \( \theta_i(s) \), represent the phase of the input and output signals, respectively, the other two stand for analog quantities such as voltage or current levels. Note that two nodes appear to have been left out. They are in fact scaled versions of other nodes and, as such, are not considered distinct. Now, the list of candidate nodes for device stimulation should be curtailed by an important criteria, the possibility of introducing a summing operation for the signal injection at the appropriate point in the circuit. Each of the aforementioned nodes will be examined for this requirement. First, as the input variable, denoted \( \theta_i(s) \), refers to jitter on a digital signal, a summing operation at this point of the circuit may be performed by a variable delay circuit. This technique will be described in greater length in the following section. The output variable, \( \theta_o(s) \), is of the same nature and therefore a similar solution may be applied. It will be discussed in Section IV. On the other hand, it is very difficult to sum a signal at the input of the VCO, labelled \( \theta_i(s) \) on the diagram. The quantity represented by the variable at this point is a voltage for which no simple circuit exists. For this reason, the last candidate node is the output of the phase detector, denoted \( \theta_o(s) \). It turns out that its possible use for test signal injection is conditional on the type of charge pump and the filter implementation. For a current charge pump or the combination of a voltage charge pump and an active filter, the summation of signals at the input of the filter may be implemented easily. However, no trivial solution is available for a voltage charge pump coupled with a passive filter. Fortunately, this configuration is seldom employed in modern designs as it results in non-linear PLL characteristics. This signal injection method which requires an extra charge pump will be presented in Section V. Three methods are thus generally available for PLL stimulation.

III. PLL Input Test Signal

The characterization a charge-pump PLL through its input signal requires the generation of a square wave (digital signal) whose phase, sometimes called jitter, can be controlled. Conceptually, this signal may be obtained from a sinusoidal signal fed to a comparator. This signal, \( s(t) \), is thus expressed as

\[
s(t) = \text{sgn}(\sin(2\pi f_c t + \theta(t))) \, ,
\]

where \( \text{sgn} \) is the signum (sign) function, \( f_c \) is the carrier frequency and \( \theta(t) \) is the instantaneous phase. The amplitude of the signal is irrelevant as \( s(t) \) is a binary digital signal. Here the two levels are assumed to be \(+1\) and \(-1\). The instantaneous frequency of the argument of the signum function, \( f_i \), is defined as

\[
f_i = f_c + \frac{1}{2\pi}\frac{d}{dt}\theta(t) \, .
\]

For the purpose of this work, the instantaneous phase is selected to be a sinusoidal signal. This type of jitter function allows the measurement of frequency domain characteristics such as the jitter transfer function or the jitter tolerance. Other types of jitter signals could be used to test, for example, the transient behavior or the lock range of PLLs. The instantaneous phase can therefore be defined as

\[
\theta(t) = A \sin(2\pi f_j t) \, ,
\]

where \( f_j \) is the jitter frequency and \( A \) is its amplitude. Using this definition in Eq. (1), the resulting signal may thus be represented as

\[
s(t) = \text{sgn}(\sin(2\pi f_c t + A \sin(2\pi f_j t))) \, ,
\]

Replacing \( \theta(t) \) in Eq. (2) with the corresponding expression in Eq. (3), the frequency of a carrier which is phase modulated with a sinusoidal signal is

\[
f_i = f_c + A f_j \cos(2\pi f_j t) \, .
\]

It can be seen that the desired stimulus is equivalent to a carrier which is frequency modulated (FM) with a sine-wave. Fortunately, this type of signal is common and a number of circuits have been introduced over the years for its generation. However, sensitive analog circuits are not
Digital circuits are a better choice as they do not require calibration, are very accurate and may be programmed for various signal characteristics.

**Digital Synthesis of a Frequency Modulated Signal**

The most straightforward and versatile digital signal generation scheme is a ROM-based frequency synthesizer followed by a digital-to-analog converter (DAC). A diagram of an FM synthesizer using this technique is illustrated in Fig. 2. A digital FM signal is generated with the help of a ROM implementing a sinusoidal function. The modulated signal is converted to the analog domain with the help of an N-bit DAC. A comparator finally generates the jittery square wave. There are two problems with this proposition for a BIST application. First, the ROM implementation requires a large silicon area. However the biggest problem lies with the DAC and its smoothing filter. As these circuits are analog, they cannot be verified with digital methods before the PLL test. In fact, the DAC may be more difficult to test than the PLL.

A possible solution would be to move the comparator just after the ROM before the digital-to-analog conversion. Then the input of the DAC would become a single-bit signal. This arrangement is illustrated in Fig. 3 (a). One-bit DACs are very simple to design. To examine the effects of this modification, signals from this circuit are compared with signals from the circuit of Fig. 2 and the results are displayed in Fig. 3 (b). The dots show the discrete values of the digital sinusoidal signal. These points are connected by the continuous line representing the signal that would result from a perfect digital-to-analog conversion. The solid square wave is derived from it using an idealized sign operation. This is the desired signal. The dashed square wave shows the result when the comparison is performed in the digital domain. Obviously, significant errors result because the signal transitions are constrained to the clock rising edges. To reduce the magnitude of these errors and thus improve accuracy, a solution is to increase the ratio of the clock frequency to the PLL frequency. However, in most applications, the PLL frequency is too large to afford a ratio that would lead to sufficient signal quality.

**Delta-Sigma Digital Phase Modulation**

Looking at Fig. 3 (b), it can be seen that performing the comparison in the digital domain results in errors in the zero crossings. They occur because these zero crossings are constrained to the clock edges. This situation is analogous to the general problem of digital-to-analog conversion. Indeed, this latter operation aims at representing a continuous signal with discrete values. Similarly, for jitter generation, it is desired to use a square wave with transitions constrained to the clock rising edges to represent an FM signal with zero crossings which fall in between clock events. There is thus an exact mapping between the two problems where one domain is voltage or current levels and the other is time (phase). It is therefore natural to examine how the quality of digital-to-analog conversion with coarse quantizers can be improved and see if any solution can be adapted to jitter generation. It turns out that the technique named delta-sigma (ΔΣ) modulation is suited for this purpose [4]. In a nutshell, the error which occurs because of quantization at a given sample is taken into account for the following quantization operations. If the bandwidth of the device using the signal is much lower than the rate at which the quantizations are performed, then the error adjustment makes the quality of the signal.
almost as good as if no quantization occurred. \(\Delta\Sigma\) modulation is also referred to as noise-shaping because, in the frequency domain, the error power from quantization is located mostly at high frequencies while the signal is low frequency.

\(\Delta\Sigma\) modulation may be applied to jitter generation in the following way. For each PLL cycle, a value for the instantaneous phase is quantized to a clock edge. The error created is recorded and will influence the phase of later PLL cycles. The use of \(\Delta\Sigma\) modulation on phase is pictured in Fig. 4. The vertical dashed lines are rising edges of the clock signal with the ticker ones defining the zero reference for phase in each cycle. Four different cycles of a signal where transitions are restricted to the rising edges of the clock are shown at the top of the figure. Stacking them vertically while aligning the reference phase, the principle of \(\Delta\Sigma\) phase modulation may be visualized. Here, by toggling the phase between \(\pi/4\) and \(\pi/2\) radians, on average a jitter of \(3\pi/8\) radians is created. This averaging is performed because the time constant of the PLL which will use this signal is much smaller than the rate of phase switching. A similar principle was demonstrated for the generation of clock signals with programmable frequency [5]. This scheme is not limited to constants but may also generate complex signal such as sinewaves.

Fig. 5 illustrates a circuit that can generate digital signals with noise-shaped jitter. The signal at the upper left is a pulse whose period is an integer multiple of the test clock period. Using a string of registers, denoted \(z^{-1}\), signals with different phases are created. The output of one of these registers is arbitrarily denoted \(reference\) and is assigned an index of 0. These signals are routed to a multiplexer where a multi-bit digital signal, denoted \(p(n)\) selects the desired phase. This signal is labelled the phase index signal and is updated at every PLL cycle. Because \(p(n)\) is encoded using a \(\Delta\Sigma\) modulator, the phase of the output signal, denoted \(\theta(n)\), will be noise-shaped.

The operation of this circuit can be better understood by examining its signals. Fig. 6 shows typical waveforms in this circuit for a test clock \((f_T)\) 8 times the reference signal frequency \((f_C)\). In fact, the ratio of the two frequency is denoted as the oversampling ratio \(D\). \(T_T\) and \(T_C\) are the periods of the test clock and the reference signal, respectively. The dotted lines represent the test clock edges with the thick ones indicating zero phase references. It can be seen that the reference signal is delayed by a constant three clock periods with respect to the pulse signal. On the other hand, the positions of the pulses of the modulated signal are dictated by the values of \(p(n)\) in each cycle. Specifical-
ly, the phase index signal \( p(n) \) represents the number of clock cycles the output signal is delayed with respect to the reference signal. It varies from \(-D/2\) to \(+D/2\).

For each PLL cycle, the time delay relative to a pulse at the reference position is therefore \( p(n) \cdot T_s \). The instantaneous phase of the output signal is then expressed as

\[
\theta(n) = p(n) \frac{2\pi}{T_C} = 2\pi p(n) \frac{f_c}{f_s} = p(n) \frac{2\pi}{D} \text{ (rad)}. \tag{6}
\]

It is obvious from the example in Fig. 6 that the possible positions of the pulses in the modulated signal are very limited within a period. This observation raises questions about the significance of any test result obtained with such a coarse signal. However, PLLs are frequency selective with respect to jitter. In fact, the jitter transfer function is lowpass and the device filters high-frequency jitter. When incorporating a \( \Delta\Sigma \) modulator in the signal generator, quantization noise is shaped to high frequencies. In fact, the encoded signal from a lowpass \( \Delta\Sigma \) modulator, such as \( p(n) \) in Fig. 6, contains a high-quality low-frequency sine-wave and high-frequency quantization noise as illustrated with the top curve of Fig. 7 (a). Because the PLL is lowpass and is designed to reject high-frequency components in the loop, the quantization noise will be mostly filtered as shown with the lower curve. Fig. 7 (b) shows the signal band in more details. A similar filtering principle was demonstrated for a voice CODEC, another analog lowpass circuit [6].

IV. Modulation of the PLL Feedback

The second access point for stimulus injection in the PLL is the output. It may seem odd to actually use an output terminal to stimulate a device but it should be reminded that this circuit is a closed loop. Therefore, feedback ensures that every block is stimulated by the test signal.

Since the output signal is a jittery digital signal, the addition of a stimulus is performed much like for the input signal. A variable-length counter implements a programmable delay allowing jitter to be added or subtracted. The resulting PLL is illustrated in Fig. 8. This circuit was introduced a few years ago for frequency synthesis under the label of delta-sigma fractional-N synthesizer [7]. In this application, the purpose of the variable length divider is to allow the synthesis of sinewaves whose frequencies are not limited to integer multiples of the input frequency. Therefore, in synthesizers, a counter with two lengths is sufficient. Consequently, the \( \Delta\Sigma \) modulator which encodes the wide baseband signal will have a single-bit output for toggling between the two lengths. On the other hand, for clock distribution applications the output frequency will be an integer multiple of the input frequency. In this case, two supplemental counter lengths, one larger and one smaller are necessary to allow jitter with both positive and negative values to be added. This requirement that both positive and negative delays should be produced imposes the constraint that a counter must already be present in the PLL. Otherwise only positive values of jitter can be added and thus sinewaves may not be injected without an undesired DC component. The above paper only discussed the synthesis of sinewaves and therefore constant phase modulation. The use of fractional-N synthesizer for the generation of time-varying jitter was demonstrated in a later paper [8].

Modulation of the PLL feedback is equivalent to digital modulation of the PLL input as illustrated in Fig. 9. For simplicity, only the phase detector and the signal injection summing operation are shown. Obviously, test signals injected in the input signal or in the feedback path will have the same effect on the circuit except for a negligible sign.

![Diagram](image-url)
change. Therefore, results obtained with any one of these methods applies to the other. They are interchangeable from a theoretical point of view. Practically however, the digital modulation of the input signal necessitates a larger external reference (clock) frequency but does not require the presence of a divider in the feedback loop.

Furthermore, the modulation of the PLL feedback is a non-linear operation and distortion may result. This comes about because the quantization steps in the time-domain, as set by the counter in the feedback path, is the output signal period, denoted $T_o$. This value is not constant but rather depends on the output frequency, $f_o$. On the other hand, the time quantization step at the input is the clock period, $T_S$, which is a constant. An expression can be obtained linking $T_o$ to the output jitter. First, the output signal, $s_o$, is defined as

$$s_o(t) = \text{sgn}(\sin(2\pi f_c t + \theta_o(t)))$$

where $f_c$ is the frequency of the reference input and $N$ is the average value of the counter length. The output period is defined as

$$T_o(t) = \frac{1}{f_o(t)} = \frac{2\pi}{d s_o(t)/d t}.$$  

Using Eq. (7) in Eq. (8), the following expression is obtained,

$$T_o(t) = \frac{1}{N f_c + \frac{1}{2\pi} \frac{d \theta_o(t)}{d t}}.$$  

It should be noted that the frequency deviation is much smaller than the center frequency of the VCO, a relation denoted as

$$\frac{1}{2\pi} \frac{d \theta_o(t)}{d t} \approx N f_c.$$  

Therefore Eq. (9) simplifies to

$$T_o(t) = \frac{T_c}{N} \left(1 - \frac{1}{2\pi N f_c} \frac{d \theta_o(t)}{d t}\right).$$  

The second term in Eq. (10) is the relative frequency deviation. Its maximum value is defined as the modulation index in FM signals. While insight is difficult to grasp with the previous equations, their behavior can be understood using simulations. Fig. 10 shows the power density spectrum, obtained with the help of simulations, of the output jitter, $\theta_o(t)$, at low frequencies. The bottom curve was obtained with digital phase modulation of the input while the top curve represents modulation of the feedback. Although not shown on this graph, the two curves are identical at larger frequencies. It can be seen that the second method results in a higher noise floor at low frequencies and that the second harmonic is visible. Nevertheless, this does not degrade significantly the SNR over the Nyquist band because the noise level at higher frequencies is larger and similar for both. However, here the modulation index of the output signal is a small 0.4%. The effect of the non-linear behavior of the digital modulation of the PLL feedback will become significant for larger maximum frequency deviations.

V. Test Signal Injection with a Charge Pump

The third option for the generation of jitter is the injection of a test signal at the input of the loop filter as shown in Fig. 11. This signal source, represented here by the variable $\theta_x(z)$, is injected through a second charge pump with gain $K_X$. It should be understood that this signal source is not a jittery digital signal but an analog signal embedded in a 1-bit digital signal. However this signal, when referred back to the input is equivalent to input jitter. The
PLL reference signal meanwhile is a square wave and therefore the input jitter $\theta_i(z)$ will be zero. This setup will be used to evaluate the characteristics of the PLL through the measure of its $\theta_o(z)/\theta_i(z)$ transfer function. Examining the model of Fig. 11, it can be seen that this transfer function will be equal to

$$\frac{\theta_o(z)}{\theta_i(z)} = \frac{K_X}{K_P} \cdot \frac{K_P \cdot F(z)}{1 + K_P \cdot F(z)}.$$  \tag{12}

It is thus equivalent within a multiplicative constant to the jitter transfer function $\theta_o(z)/\theta_i(z)$. For a spectral test such as the jitter transfer function, the test signal is a sine-wave encoded into a single bit. The quantization noise is concentrated at high frequencies and is filtered out as explained in the previous sections.

It is important to note that the clock period for signal injection must be an integer multiple of the input reference period to prevent aliasing of the quantization noise back in the PLL passband. This condition implies that the signal injection frequency cannot be higher than the reference signal frequency. Converting the 1-bit digital stream to an analog signal and summing it with the output of the phase detector is quite simple. A second current charge pump is placed in parallel with the phase detector charge pump and both outputs are tied in a current summing node as shown in Fig. 12. The accuracy of this analog-to-digital conversion is a function of the matching of the two current sources $I_P$ and $I_X$, typically ranging between 0.1% - 1% in monolithic form. In this schematic, the impedance $Z_F$ implements the loop filter and $V_C$ is the controlling voltage of the VCO.

| $f_C$    | 155 MHz |
| $K_P$   | $8 \times 10^{-7}$ A/rad |
| $K_O$   | $5 \times 10^8$ rad/V*s |
| $R$     | 1 kΩ |
| $C$     | 220 nF |

Table 1. Phase-locked loop parameters.

VI. Maximum Jitter Amplitude in the Presence of Quantization

A PLL has a limited range of input frequencies. This is usually set by the tuning capability of the VCO and is referred to as the lock range. Any linear PLL test must therefore ensure that the frequency of the stimulus signal remains within the lock range of the DUT. This restriction is more of a concern for noise-shaped signals such as those used in the jitter generation schemes of this paper. At many PLL nodes, the residual quantization noise in the test signal will increase the signal swing. Here, the residual quantization noise refers to the input signal noise that is not attenuated by the loop dynamics. To avoid meaningless test results, this effect must be accounted for so that all signals in the PLL remain within their linear range.

Fig. 13 illustrates the situation for a critical PLL node, the input of the VCO. The voltage at this node will vary to allow the VCO to track the jittery signal. However, quantization noise will increase the voltage swing by an amount $\delta$ at each end. The test designer must make sure that the resulting voltage deviations remain within the range of input to the VCO for linear operation. A typical signal that can be found at the input node of a VCO for a PLL driven by a $\Delta\Sigma$ modulated signal is shown in Fig. 14. It was ob-
tained from simulations of a PLL with an RC passive filter similar the one shown in the lower right part of Fig. 12 and the parameters of Table 1. Part (a) illustrates a full cycle while part (b) shows in more details the time interval where the maximum is located. The signal consists of a high-frequency square wave superimposed on a sinewave. While the sinewave amplitude is only 9.5 mV peak-to-peak, the quantization noise is pushing the voltage range to almost 20 mV peak-to-peak.

To obtain an expression for the added voltage swing, \( \delta \), it should be noted that the maximum disturbance will occur when the sinewave is at its maximum or minimum and a quantization step of relative value \( \Delta \) is added. This event is contained within a single period of the VCO signal. Therefore, as the VCO output is constant, the circuit can be analyzed in open loop configuration. Fig. 15 illustrates the model. A quantization step in the test signal is turned into a pulse of duration \( \Delta \times T_C \) times the period of the phase detector, \( T_C \), set by the reference signal. The pulse amplitude is denoted \( K_I \) representing the gain of the test signal injection circuitry. It will generally be equal to \( K_P \), the gain of the phase detector and charge-pump circuits of the PLL except when an extra charge pump injects the test signal (see Section V). Finally, this pulse is shaped by the PLL loop filter.

The input to the filter, \( x(t) \), is the sum of two steps, \( u(t) \), of equal magnitude, one of which is inverted and delayed. The output of the filter will be the convolution of this signal with the filter impulse response, \( g(t) \). The result will have to discontinuities at \( t = 0 \) and at \( t = \Delta \times T_C \). The magnitude of \( \delta \) is the amplitude of the discontinuities in the output signal. It will thus be proportional to the immediate response of the filter to a step function. This is denoted in the time domain as

\[
\delta = \lim_{t \to 0} x(t) \cdot g(t) = \lim_{t \to 0} K_I u(t) \cdot g(t) \quad (13)
\]

The equation may be reformulated in the frequency domain resulting in

\[
\delta = K_P G(s) \big|_{s \to \infty} \quad (14)
\]

As an example, this theory can be applied to the simple passive RC filter of Fig. 12 with test signal injection using the PLL charge pump. This could be, for example, the method of digital phase modulation of the input. The transfer function of the filter is

\[
G(s) = R + \frac{1}{sC} \quad (15)
\]

Using this function into Eq. (14), the following expression is obtained for the disturbance

\[
\delta = K_P \left( R + \frac{1}{sC} \right) \big|_{s \to \infty} = K_P R \quad (16)
\]
For the values quoted in Table 1, the maximum bound on \( \delta \) is found to be

\[
\delta = 8 \times 10^{-7} \text{ A/\text{rad}} \times 2\pi \times 1 \text{ k\Omega} = 5 \text{ mV}.
\] (17)

This value is consistent with the simulation results shown in Fig. 14.

VII. Experimental Results

Two methods for the stimulation of PLL, digital modulation of the input and test signal injection using a charge pump, were verified experimentally in a previous paper [3]. Some of these results are reproduced here in Fig. 16. Two curves are shown with solid lines representing the measurement of the jitter transfer function with two different methods: the digital modulation of the input and the signal injection with an extra charge pump. A dashed line obtained from the measured values of the discrete components is also displayed for reference. The other PLL stimulus technique, digital modulation of the PLL feedback is validated here with another set of experiments using a similar set-up.

For all the experiments, the set-up is built on a bread board. Discrete components are used to emulate the analog parts of a PLL. The digital portion along with the circuits required for BIST are implemented on a field-programmable gate array (FPGA). The VCO frequency range is centered around 800 kHz and a divide-by-8 counter is located in the feedback loop. A 800 kHz clock is necessary to both generate a 100 kHz reference signal and to evaluate a \( \pi/4 \) jitter threshold.

In test mode, a sinusoidal signal encoded on three bits is generated by a \( \Delta \Sigma \) oscillator [9]. The result is used to modify the length of the feedback counter and thus modulate the output signal. Because the output amplitude is not measured exactly but rather a jitter threshold circuit is used, a binary search algorithm is necessary to find the input jitter amplitude which results in the output jitter closest to the selected threshold. For each frequency point, the amplitude is resolved to a 15-bit accuracy.

The experiments are carried for two different configurations of the PLL loop filter. These PLLs exhibit different jitter transfer function bandwidth and damping value. The results of the first experiment are shown in Fig. 17. The measured jitter transfer function is plotted with a solid line. For comparison, a transfer function obtained using the measured values of the discrete components and PLL theory is plotted with a dashed line. It can be seen that the experimental results are quite similar to what is predicted by theory. However, a 0.6 dB offset is noticeable. It can...
be attributed to the static jitter of the PLL arising from mismatch in the up and down charge pumps.

The measurement of a jitter transfer function with a smaller damping value is shown in Fig. 18. There is a small discrepancy of the maximum jitter gain between the measured results and theory. It can be traced back to the parasitic capacitance of the circuit which is not accounted for in the theoretical calculations.

VIII. Conclusions

Three methods have been presented for the stimulation of charge-pump PLLs. The first one, digital phase modulation of the PLL input is non-intrusive but it requires a reference clock signal with a frequency significantly larger than the PLL input frequency. In contrast, digital modulation of the PLL feedback necessitates a reference signal with a lower frequency. However it is non-linear and therefore distortion and noise mixing will occur. Nevertheless, these effects can be kept negligible by careful selection of the test signal parameters. Finally, injection of a test signal at the input of the loop filter requires an additional charge which may lead to matching errors. Furthermore, multi-bit operation may not be implemented easily. However, it is the only method which can use a reference frequency lower than the PLL input reference signal. Then the effect of quantization noise on the device-under-test was evaluated. Finally, experiments for digital modulation of PLL feedback complemented results disclosed in previous papers.

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References


