Parallel Waveform Relaxation and Matrix Solution for Large PEEC Model Problems

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Overview

- State of Parallel Processing
- Waveform Relaxation + Partitioning of Large Problems
- Application to PEEC using WR
- Results and Conclusions

Research

Application Ready

Present Status
New Role of Parallel Processing for Electrical Package Analysis

Real Parallel Processing has Finally Arrived!

- Parallel processing was key issue at 2007 DAC
- Interest in parallel EDA algorithms + software!
- New path for speed-up (hardware + software)

Challenge: New, fast, parallel algorithms

Hardware / Software

- Multi-core chips - lower latency solutions
- Networked processors - larger latency
- Large computer systems, multiple multi-core processors - larger latency connections
Using Combined Solution Approach

*Local Near* - Point by Point Type Computations
- Faster for low latency algorithms!
- Mostly *localized* computations
- Used to equalize subsystem compute time

*Global Far* - Waveform Coupling Computations
- Use Waveform Relaxation (WR) for solution
- WR, exchange of *waveforms* rather than *point* data
- Important: Works well for parallel machines with larger latency
Application: Large EM/Ckt Problems

EM/Ckt Problems

- EM/Ckt solution with many interactions
- Real problems: Heterogeneous mix of interactions both linear/nonlinear
- Nonlinear solvers needed for drivers/loads
- High frequencies demand 3D full wave solution

Large Problems Need Partitioning

- Some problems can be naturally partitioned
- WR: Partition with iterations, errors control
Fundamental Idea of Waveform Relaxation (WR)

Two subsystems ($SS_y$) example

- Choose parts which interact (weakly or One-Way)
- Large problems result in many $SS_y$s

\[ v_{i}(t) \]

System Partition \( m \)

System Partition \( m+1 \)
PEEC Model for WR-EM Solution

Waveform Relaxation with All Circuit Domain EM Solution

- Transient (and frequency) domain electromagnetic models
- Circuit domain: capacitances, inductances, resistances, voltage, current sources
- Mixed Spice circuits and EM circuit analysis
- Using modified nodal analysis (MNA) formulation
- MNA: Full spectrum - $dc$ to daylight EM solution
Basic Derivation of PEEC Model

Equation for Total Electric Field

- **KVL**: \( v = \int \mathbf{E} \cdot d\mathbf{l} \)

\[
\bar{E}^i(\bar{r}, t) = \frac{\bar{J}(\bar{r}, t)}{\sigma} + \mu \int_{V_t} G(\bar{r}, \bar{r}') \frac{\partial \bar{J}(\bar{r}', t_d)}{\partial t} dV' \\
+ \frac{\nabla}{\varepsilon_0} \int_{V_t} G(\bar{r}, \bar{r}') q(\bar{r}', t_d) dV'
\]  

(1)

PEEC Circuit Model Element Computation

- **KVL**: Voltage = \( R \ I + s \ Lp \ I + Q/C \)
- **RHS Term 1**: Resistance
- **RHS Term 2**: Partial Inductance
- **RHS Term 3**: Coefficient of Potential
(Lp,P,R,τ)PEEC Equivalent Circuit Model

PEEC Equivalent Circuits For Two Basic Cells

- Example: 3 Node Discretization of “Metal Stick”
- Path along metal conductor is strongly coupled
- Coupled Partial Inductances and Capacitances

![Diagram of Equivalent Circuit Model](attachment:image.png)
Utilization of Different Ways for Partitioning

- Break into Subsystems $SSy$, How?
- Special circuit based splitting, partitioning into $SSy$
Outline of Partitioning Approach

EM Geometry Partitioning into SSys

- Conductors are strongly coupled
- Partial inductances and potential coefficients?
- Check for strength of the couplings
- Separate at weakly coupled boundaries

Utilization of Different Couplings

- **Assemble the Subsystems** SSy
- All components in an SSy have strong couplings
- Most SSy interconnects have weak couplings
- Tradeoff between SSy size and no. of iterations
Coupling Factors for Partial Elements

Coupling factors checks for partitioning

- Find that for PEEC majority of couplings are weak
- Coupling factors $\gamma \leq 0.25, 0.5$
- Convergence in 3 to 10 iterations
- Inductive coupling: $\gamma = \frac{Lp_{12}^2}{(Lp_{11}Lp_{22})}$
- Capacitive couplings, similarly
- Inductive, capacitive far couplings weak $\gamma \ll 0.1$
- Can also use distance-size related criteria
Inductive $SS_y$ WR Decoupling

\[ V_2 = Lp_{26} sI_6 + Lp_{29} sI_9 + \cdots \]
\[ ; V_6 = Lp_{62} sI_2 + Lp_{69} sI_9 + \cdots \]
Capacitive $SS_y$ WR Decoupling

$$I_2 = \frac{p_{25}}{p_{22}} I_{c5} + \frac{p_{27}}{p_{22}} sI_7 + \cdots$$
Assembling the SSys form elements

Test Coupling all Elements Between SSy Elements

- Some \( dc \) paths are directly coupled
Solution of Partitioned SSys

- Neutral Delay Differential Equations (NDDE) in Modified Nodal Analysis (MNA) form

\[ C_0^* \dot{x} + G_0^* x + \sum_i G_i^* x(t - \tau_i) + \sum_i C_i^* \dot{x}(t - \tau_i) - \sum_i B_i^* u_i(t - \tau_i) = \]
\[ -\sum_i C_i^+ \dot{x}(t - \tau_i) - \sum_i G_i^+ u_i(t - \tau_i) + \sum_i B_i^+ u_i(t - \tau_i) \]

- Solve the subsystems SSy in usual Spice form
- Each processor has its own Spice circuit solver
- Always use updated waveform results
- Each subsystem SSy has its own timestep
- Need multi-rate interpolation among the coupled waveforms
Ordering and Scheduling for SSy

Ordering: (Pin1: SSy1), (Pin3: SSy2), (Pin4: SSy3), (Pin5: SSy4), (Pin2, Gnd: SSy5)

- Basic schedule SSy1, SSy2, SSy4, SSy5, SSy3
Waveform Validation for WR Solution

Set of Contacts over a groundplane

- Center to center spacing is 1mm
- Example 6 contacts, $400\mu^2 \times 13\mu$

Contacts are connected to 50 Ohms
The first contact is driven by a pulse voltage source with rise time $\tau_r = 50$ ps.

Left: transient voltage; Right: magnitude spectrum.
Induced Voltage at Other Contacts

First contact terminated with a 50 Ω resistance while all the other contacts are floating. The analysis is carried out by using the standard PEEC method as well as the (WR)PEEC solver.

Voltage at contacts 2 and 6.
Induced Voltage at Other Contacts

Potential of grounded contacts 2 and 6.
Connector Problem
## Connector PEEC SSy Circuits

<table>
<thead>
<tr>
<th>Inductive cells</th>
<th>Capacitive cells</th>
<th>Nodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>552</td>
<td>752</td>
<td>200</td>
</tr>
</tbody>
</table>

Table 1: Global problem.

<table>
<thead>
<tr>
<th>Inductive cells</th>
<th>Capacitive cells</th>
<th>Nodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>264</td>
<td>304</td>
<td>80</td>
</tr>
</tbody>
</table>

Table 2: Grounded pin+ground plane.

<table>
<thead>
<tr>
<th>Global [s]</th>
<th>Grounded pin+ground plane [s]</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>119.4</td>
<td>21.35</td>
<td>5.59</td>
</tr>
</tbody>
</table>

Table 3: CPU-time requirements.
Parallel Matrix Solution of SSy

- Size of each SSy is different for real problems
- Several processors to solve SSy circuits

Parallel compute time for 1 pin and pin + ground
Multi-Bar: Crosstalk Problem

MTL: 11 conductors

Multiple parallel bars
Multiple Bars Waveform Validation

Input/output port voltages (left) and near/far end port voltages (right).
**Single Processor Results for WR vs. Flat**

- WR Speed Up Obtained for Conductor Array
- Number of subsystems (SSy): 11
- Unk. 1188: WR: 151 s; Flat: 553 s; SpU: 3.66
- Unk. 2508: WR: 323 s; Flat: 1433 s; SpU: 4.46
- Unk. 3388: WR: 660 s; Flat: 3284 s; SpU: 4.97
Summary and Conclusions

Parallel PEEC Solution using WR

- New research area for EM/Ckt parallel processing
- Guaranteed fast convergence ≤ 10 WR iterations
- Key interchange of waveforms rather than point data!
- New algorithm is highly suitable for parallel processing
- Experiment with larger problems in progress

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