Static and low frequency noise characterization in surface- and buried-mode 0.1 μm PMOSFETS

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Abstract

In this work, static and low frequency noise parameter extraction are carried out on surface- and buried-mode 0.1 μm PMOSFETs. The two architectures are based either on a surface mode of operation (SC) or on a buried one (BC) featuring P+ and N+ polygate, respectively. The impact of the gate architecture i.e. P+ and N+ polysilicon, on the static and noise parameters is analyzed. The 1/f noise, which can be interpreted in terms of carrier number fluctuations, is found to be about one decade lower for buried-mode devices. The statistical sample-to-sample dispersion of the noise level has also been studied and found to be as large as 4–5 decades for the nominal area devices. Standard RTS analysis has also been performed on representative PMOS devices.

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1. Introduction

The miniaturization of integrated circuits leads to an enhancement of the problems related to the dimension shortening in MOS transistors. Indeed, the device area reduction reinforces the 1/f noise, which can constitute a serious limitation for analogue and digital circuit applications as well as for the performance of non-linear RF circuits [1]. The comprehension of these fluctuations is therefore essential for process optimization and design of integrated circuits.

In this work, we have carried out a detailed investigation of low frequency (LF and RTS) noise and static properties, such as threshold voltage, drain induced barrier lowering (DIBL), low field mobility, mobility attenuation factor as well as effective channel length and series resistances of surface- and buried-mode P channel MOS devices. The buried channel (BC) architecture uses a polysilicon gate material that is doped identically for both n-channel and p-channel devices. Typically, if the gate material is n-type, the PMOSFET works as a BC device. In the case where the gate material is p-type, a surface channel (SC) PMOSFET is formed. The design and application of these two gate architectures have been already discussed [2–5].

2. Devices and experiments

The devices used throughout this study have been fabricated at CEA/LETI. P+ and N+ polysilicon gates are used for SC and BC PMOSFETs, respectively. The gate oxide thickness \( t_{ox} \) is about 2nm, the channel doping concentration lies in the range of 5 to 7 \( \times 10^{17} \) cm\(^{-3} \) for both N+ and P+ gate devices. LDD regions have also been realized. The channel length in the test module, \( L \), varies between 0.075 and 1 μm, while the lateral confinement has been made using a conventional local oxidation of silicon (LOCOS).

The low frequency (LF) noise and RTS measurements have been performed using a FFT dynamic signal analyzer HP35665A loaded by a high sensitivity current/voltage converter and a low noise voltage amplifier. The voltage sources were filtered NiCd batteries. The static characteristics of the devices were measured with a semiconductor parameter analyzer HP 4155.
3. Results and discussion

3.1. Static parameter extraction

Typical $I_d(V_g)$ transfer characteristics as obtained in Ohmic region on both architectures (P+ and N+ gate) are shown in Fig. 1 for various channel lengths ($L = 0.075–1 \, \mu m$) and a large width $W = 10 \, \mu m$. The good performance of the drain current below threshold can be noticed and indicates a good control of short channel effects at least down to $0.1 \, \mu m$ as will be detailed below for both channel types.

The extraction of the main static MOSFET parameters has been performed using the function $Y(V_g)$ defined as [6]

$$Y(V_g) = I_d/\sqrt{g_m}$$

(1)

where $g_m$ is the transconductance. The linear part of this function observed above threshold provides the charge threshold voltage $V_t$ and low field mobility $\mu_0$ regardless of the influence of access series resistance $R_{sd}$ and mobility attenuation factor $\theta$ [6].

![Fig. 1. $I_d(V_g)$ transfer characteristics for (a) SC and (b) BC PMOS devices with various gate lengths and a fixed channel width $W = 10 \, \mu m$ (drain voltage $V_d = -50 \, mV$).](image)

The gate length dependence of the threshold voltage shown in Fig. 2 indicates an overall good behavior for both SC and BC mode PMOSFETs down to $0.1 \, \mu m$. However, the good control for BC devices requires a higher $V_t$ to compensate for poorer short channel effect properties as compared to SC mode PMOSFET.

The channel length reduction in MOS transistors induces DIBL effects, resulting in a lowering of the source/substrate potential barrier after application of a high drain voltage. From the $I_d(V_d)$ output characteristics (not shown here), obtained in saturation region, we have extracted and plotted in Fig. 3 the DIBL coefficient, which is defined in saturation as,

$$\text{DIBL} = \frac{d \ln(I_d)}{d V_d}$$

(2)

As can be seen from Fig. 3, BC MOS devices exhibit larger DIBL effect as expected from their buried mode of operation [2–4]. For both types, the DIBL coefficient...
appears to increase with reciprocal gate length in agreement with simple theory.

The extraction of the effective dimensions of the devices has been carried out after plotting the reciprocal transconductance parameter $G_m$ defined by $G_m = WCM_0\mu_0/L$ as a function of drawn gate length [5]. This enabled us to obtain the gate length reduction $\Delta L \approx 0.036$ and $0.037 \mu m$ for BC and SC PMOS, respectively, emphasizing the very good dimension control for this advanced PMOS technology.

The effective channel lengths being known, the low field mobility has then been calculated from the transconductance parameter, $G_m$, giving values for N+ and P+ PMOSFETs respectively as $\mu_0 \approx 57$ cm$^2$/V$s$ and $\mu_0 \approx 48$ cm$^2$/V$s$.

After extraction of mobility attenuation factor $\theta$, a further plot of $\theta$ as a function of $G_m$ should give a straight line from which the slope provides $R_{sd}$ and the y-axis intercept the intrinsic mobility attenuation factor $\theta_0$. We found $R_{sd} \approx 110$ and $180 \Omega$ for a 10 $\mu m$ wide channel, and, $\theta_0 \approx 0.12/V$ and $0.55/V$ for BC and SC PMOSFETs, respectively, indicating less surface scattering for buried devices.

### 3.2. LF noise parameter extraction

In Fig. 4 we show the variation of the normalized drain current 1/$f$ noise $S_{id}/I_d^2$ with drain current from weak to strong inversion regions at $V_g = -50$ mV and $f = 10$ Hz in SC and BC PMOS transistors. The device gate length is taken as a parameter. The correlation of the drain current noise level with the corresponding transconductance to drain current ratio squared, $(g_{m}/I_d)^2$, over a wide drain current range, clear indicates that carrier number fluctuations due to hole trapping in the oxide dominate for both SC and BC PMOS devices. Indeed, in the carrier number fluctuation model, the drain current noise is given by [7]

$$S_{id}/I_d^2 = \left(\frac{g_m}{I_d}\right)^2 \cdot S_{tg}$$

(3)

where $S_{tg}$ is the input gate referred noise. Therefore, if $S_{tg}$ is weakly bias dependent, $S_{id}/I_d^2$ essentially varies as $(g_{m}/I_d)^2$.

The input gate referred noise is actually related to the flat band voltage spectral density $S_{fB}$ and correlated mobility fluctuations in strong inversion as [7]

$$S_{fB} = S_{tg}(1 + \kappa \cdot C_{ox} \cdot \mu_0(V_g - V_t))^2$$

(4)

where $\kappa$ is the Coulomb scattering coefficient.

The flat band voltage spectral density is associated to the slow oxide trap charge fluctuations as

$$S_{fB} = \frac{q^2kTn_t}{WLC_{ox}^2}$$

(5)

where $q$ is the electron charge, $kT$ is the thermal energy, $\lambda$ is the tunneling constant ($\approx 0.1$ nm), $N_t$ is the slow oxide trap density (eV$^{-1}$ cm$^{-3}$) and $f$ is the frequency.

The oxide trap density for SC PMOS devices is found in the range $(2-5) \times 10^{17}$ eV$^{-1}$ cm$^{-3}$ and about one decade lower for BC devices. The Coulomb scattering coefficient $\kappa$, extracted from the slope of $S_{fB}^2/(V_n - V_t)$ plots (see Fig. 5), lies around $3-5 \times 10^4$ V s/C in agreement with standard data [7]. The small value for the oxide trap density of surface mode devices is a good indication of the oxide-substrate quality in such advanced technologies. Both diminution in LF noise and $\kappa$ coefficient in BC devices infer the BC operation of such devices.

### 3.3. LF noise level dispersion and RTS noise analysis

As is well known [8], for small area MOS devices (here $0.25 \times 0.1$ $\mu m^2$), the LF noise becomes more and more
RTS like as illustrated on the time domain plot of drain current fluctuations displayed in Fig. 6. This RTS behavior strongly modifies the $1/f$ noise behavior generally observed on large area MOSFETs evolving into Lorentzian spectra [8] as shown in Fig. 7. These features are responsible for a strong sample-to-sample noise level variation (see Fig. 8a) due to the limited number of defects involved in carrier trapping. It should be noted that the drain current noise has been measured at constant normalized drain current to avoid $V_t$ mismatch (see caption of Fig. 8a). The statistical character of the
random placement of defects within the oxide and/or Si energy gap explains reasonably well the huge dispersion in noise level for small area devices for such a 0.1 \( \mu \)m technology [8], which can reach 5–6 orders of magnitude for the smallest areas (see Fig. 8b).

The oxide trap density \( N_t \) values extracted from the mean value of the experimental dispersion plot confirmed those determined from the 1/f noise measured on large area devices. It should be noted that such dispersion in noise level could not be explained by the dispersion in static parameters, which exhibit good reproducibility from device to device as illustrated in Fig. 9 for \( V_t \) and \( g_m/I_d \) data. The account of the area dependence of \( g_m/I_d \) average values (due to short and narrow channel effects i.e. variations of \( V_t \) and \( g_m/I_d \) with \( L \) and \( W \)) in the statistical noise modeling allows to obtain a better description of the noise level dispersion as shown in Fig. 8c.

Specific analysis of a particular device exhibiting RTS noise has also been performed in terms of high and low time constants (i.e. capture and emission times) as a function of gate bias (see Fig. 10a) and drain current amplitude (Fig. 10b). The overall behavior of the capture and emission times with gate bias is conformed to the SRH statistics, whereas the decrease of drain current amplitude is well interpreted by the simple model accounting for single hole trapping over the whole device area as [8]

\[
\frac{\Delta I_d}{I_d} = \frac{g_m}{I_d} \frac{q}{WLC_{ox}}
\]
4. Conclusion

The electrical performances in terms of output/transfer characteristics, threshold voltage, short channel effects as well as LF and RTS noise of surface- and buried-mode 0.1 \( \mu \)m PMOS transistors have been investigated. Static characterization shows that BC devices are penalized with larger threshold voltage and poorer short channel effect, but they are less prone to LF noise due to remote operation. Huge statistical noise level variation has also been demonstrated and well explained by the presence of RTS fluctuations due to the limited number of oxide defects contributing to noise for the smallest area devices.

References

[1] Gierkink SLJ, Klumperink EAM, van-der-Wel AP, Hoo- 
1999;34:1022.
Nakajima K, et al. In: Symp VLSI Tech Dig Tech Papers, 