Characterization and analysis of trap-related effects in AlGaN–GaN HEMTs

M. Faqir a, G. Verzellesi a,*, F. Fantini a, F. Danesin b, F. Rampazzo b, G. Meneghesso b, E. Zanoni b, A. Cavallini c, A. Castaldini c, N. Labat d, A. Touboul d, C. Dua e

a Department of Information Engineering, University of Modena and Reggio Emilia, Modena, Italy
b Department of Information Engineering, University of Padova, Padova, Italy
c Department of Physics, University of Bologna, Bologna, Italy
d IXL Laboratoire, Université Bordeaux 1, Talence Cedex, France
e Alcatel-THALES III-V Lab/Tiger, Marcoussis, France

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Abstract

Traps are characterized in AlGaN–GaN HEMTs by means of DLTS techniques and the associated charge/discharge behavior is interpreted with the aid of numerical device simulations. Under specific bias conditions, buffer traps can produce “false” surface-trap signals, i.e. the same type of current-mode DLTS (I-DLTS) or ICTS signals that are generally attributed to surface traps. Clarifying this aspect is important for both reliability testing and device optimization, as it can lead to erroneous identification of the degradation mechanism, thus resulting in wrong correction actions on the technological process.

1. Introduction

At the current stage of GaN technology development, AlGaN–GaN HEMTs must demonstrate adequate electrical reliability before they can massively be adopted in RF power applications, such as cellular base stations, satellite and radar transmitters, where they can offer unquestioned performance advantages over all other competing device technologies. Trap generation and the consequent amplification of RF current-collapse and power-slump phenomena are, in particular, among the most deleterious effects originating from high-electric-field operation [1,2]. Trap characterization methods, such as deep-level transient spectroscopy (DLTS), isothermal current transient spectroscopy (ICTS), and low-frequency transconductance ($g_{m}$) dispersion measurements are, therefore, key techniques for device-degradation monitoring and reliability assessment.

The aim of this work is to present results from a detailed, trap-characterization study in GaN HEMTs and to provide a consistent interpretation for the different traps detected, both in terms of localization within the device structure and of associated charge/discharge mechanism. It is in particular shown that, under specific bias conditions, buffer traps can produce the same type of current-mode DLTS (I-DLTS) or ICTS signals that are generally attributed to surface traps. Clarifying this fact is crucial for both reliability testing and device optimization, as it can completely hinder a correct identification of degradation mechanisms.

2. Experimental results

Tested devices include short-gate HEMTs, FAT-HEMTs, as well as Schottky-diode test structures all having the same GaN/AlGaN/GaN epitaxial structure grown on
semi-insulating SiC substrates by MOCVD. The epixtal multilayer consists (from bottom to top) of a 1 μm-thick undoped GaN buffer/channel layer, followed a 30 nm-thick Al0.22Ga0.78N barrier (20 nm of AlGaN doped with Si at the concentration of $5 \times 10^{17}$ cm$^{-3}$, sandwiched between two 5 nm AlGaN undoped spacers) and by a 3 nm-thick undoped GaN cap. Ohmic contacts consist of a Ti/Al/Ni/Au structure annealed for 30 s at 900 °C, while gate metallization is made of Mo/Au deposited by electron evaporation. A not-to-scale sketch of short-gate and FAT-HEMTs is shown in Fig. 1. Short-gate HEMTs have a gate length ($L_G$) of 0.15 μm, and gate-source ($L_{GS}$) and gate-drain ($L_{GD}$) spacings of 0.7 and 2 μm, respectively. FAT-HEMTs have $L_G = 14$ μm, $L_{GS} = 0.7$ μm, and $L_{GD} = 2$ μm. All structures are passivated with SiN (500 Å).

Fig. 2 shows DLTS results from a FAT-HEMT structure, pointing out the presence of three dominant trap levels, i.e. 0.18 eV (trap A), 0.5 eV (trap B) and 0.76 eV (trap C). Trap A is not found by DLTS in the Schottky-diode, while it is shown to govern the gate-lag transients measured from short-gate HEMTs if $V_{GS}$ is pulsed from negative and very large values in modulus to above-threshold values [3]. Moreover, it gives rise to a “hole-like” peak [4] in the I-DLTS spectrum of FAT-HEMTs. All of these findings consistently indicate that trap A is a surface trap.

Traps B and C were revealed by DLTS also in the diode, this suggesting that they are located in the device bulk. However, they give rise to hole-like peaks in the I-DLTS spectrum of FAT-HEMTs and to a downward $g_m$ dispersion, these indications being instead consistent with surface localization [4–6].

In order to investigate these contrasting evidences, the drain-current ($I_D$) transients were measured at room temperature, where trap B dominates (see Fig. 2), by using different $V_{GS}$ test pulses. As a matter of fact, as long as $V_{GS}$ is pulsed from 0 V to a negative value ($V_{GS,off}$) higher than the pinch-off voltage, the $I_D$ transient is of the type that is generally attributed to surface traps (see Fig. 3a). However, when $V_{GS,off}$ approaches the pinch-off voltage (that is about −4.8 V in the devices under test), the shape of the $I_D$ transient changes to that characteristic of a bulk trap (Fig. 3b).

3. Numerical simulations

Two-dimensional, drift-diffusion simulations were been carried out with the code DESSIS8.0 (Synopsys Ltd.), including deep-level-trap dynamics and gate tunneling (field emission) injection. To account for polarization charges at the two AlGaN–GaN heterointerfaces, positive fixed charges with a sheet density $N_{pol}^+ = 1 \times 10^{13}$ cm$^{-2}$ were placed at the bottom AlGaN–GaN interface (uniformly distributed over a 0.5 nm-thick region), while negative fixed charges having an equal sheet density $N_{pol}^- = 1 \times 10^{13}$ cm$^{-2}$ (and similarly distributed over a 0.5 nm region) were accounted for at the top GaN–AlGaN interface (Fig. 1).

In agreement with the surface-donor theory explaining the channel 2DEG formation in GaN HEMTs [7], donor-like traps (with a density $N_{TD} = 8.5 \times 10^{12}$ cm$^{-2}$) have been...
assumed to be present at the device surface (see Fig. 1). Consistently with experimental results, trap A parameters ($0.18 \text{ eV}, 4.5 \times 10^{-19} \text{ cm}^2$) were assumed for energy and capture cross-sections of these surface donors. Acceptor-like traps were instead placed within the GaN buffer layer (with a density $N_{BA} = 1 \times 10^{17} \text{ cm}^{-3}$). Assumed trap parameters were in this case those characterizing trap B ($0.5 \text{ eV}, 5 \times 10^{-16} \text{ cm}^2$).

Consistently with measurements shown in [3], surface traps is found to dominate simulated gate-lag transients if $V_{GS}$ is pulsed from negative and very large values in modulus to above-threshold values. The gate-lag mechanism suggested by simulations agrees with the concept of “virtual gate” as proposed in [5], i.e. surface traps capture gate-injected electrons when $V_{GS}$ is negative and large in modulus and they emit electrons as $V_{GS}$ is stepped to higher values.

Moreover, simulations reproduce the same behavior observed experimentally in FAT-HEMTs and shown in Fig. 3a and b. This is demonstrated by Fig. 4a and b, showing simulated $I_D$ transients (at $T = 300 \text{ K}$) in response to $V_{GS}$ pulses similar to those adopted for measurements.

The type of the $I_D$ transient actually changes from “surface-trap”-like (see Fig. 4a) to “buffer-trap”-like (see Fig. 4b), as $V_{GS,off}$ is decreased to a value close to the pinch-off voltage. However, inspection of internal electron and trapped-charge distributions points out that buffer-trap modulation is involved in both cases (whereas the contribution of surface-trap modulation is negligible). The underlying physics can be understood with the aid of Figs. 5–8, showing the time evolution of the electron and trapped-charge distributions during the $I_D$ transients shown in Fig. 4a and b, respectively.

As can be noted from Fig. 5, for $V_{GS,off}$ values sufficiently higher than the pinch-off voltage, the (free) electron density decreases moderately, immediately after the application of the $V_{GS}$ turn-off step, in the region of the buffer closer to the AlGaN–GaN interface. It instead increases in the deeper buffer region. Afterwards, the electron density decreases slowly with time (see Fig. 5), as a consequence of trapping by buffer traps (see Fig. 6). This explains why $I_D$ decreases during the slow transient governed by trap B (see Figs. 3a and 4a).

On the other hand, for $V_{GS,off}$ values close to the pinch-off voltage, the electron density drops drastically when the $V_{GS}$ turn-off step is applied (see Fig. 7). As a result, the
trapped-charge density decreases with time (see Fig. 8), and $I_D$ increases during the slow transients shown in Figs. 3b and 4b.

Trap C (which is not included for simplicity in the simulations) behaves similarly to trap B and is therefore inferred to be a buffer trap, too.

4. Conclusions

In conclusion, traps have been identified in AlGaN–GaN HEMTs by means of different characterization techniques and the associated physical behavior has been interpreted with the aid of numerical device simulations. Unless $V_{GS}$ is pulsed to a value close to the pinch-off voltage, buffer traps in HEMT structures have been shown to produce “false” surface-trap signals and the underlying physics has been explained. Clarifying this aspect is important for both reliability testing and device optimization, as it can lead to erroneous identification of the degradation mechanism, thus resulting in wrong correction actions on the technological process.

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