Simulation of Crosstalk through Bonding and Package in Mixed-Signal CMOS ICs

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Abstract—This paper presents an approach for simulation of mixed-signal CMOS integrated circuits, aiming at estimating crosstalk effects, by identifying possible sources of disturbances in analog-digital integrated systems, such as current pulses drawn from voltage supplies. A simple expression of voltage and current in the pull-up and the pull-down of a CMOS logic gate can be derived. A computer program demonstrates the feasibility of the proposed approach, and a representation of digital switching noise in time domain has been derived. This representation has been used to perform an analog simulation using SPICE/SPECTRE, to evaluate the propagation of the switching noise through the parasitic elements of the package and of the bonding wires.

I. INTRODUCTION

In mixed analog-digital integrated circuits, effects of digital switching noise on the analog section are often the limiting factor affecting the overall system performance [1]. Therefore, the analog designer must choose the optimum circuit architecture taking robustness and crosstalk immunity into account. Hence, simulation tools, capable of accurate analysis of current consumption during logic transitions, are required [2]. Digital simulation tools are mostly optimized for simulation speed and for “average” power consumption. On the other hand, analog simulators are quite inefficient for the analysis of large digital circuits.

In our work, we propose a simulation method to analyze the current consumption and switching noise due to the digital part of the circuit. To this end, suitable simplified models of active devices are required: in particular, we need to consider all relevant aspects to obtain sufficiently accurate results, and we wish to neglect all issues that do not contribute to a remarkable improvement, in order to keep simulation time reasonably small [3].

It is well known that circuit-level (SPICE/SPECTRE) simulation for large digital circuits is very time-consuming. Dedicated algorithms can be more efficient, although they can be applied only to a specific class of circuits. In the case of mixed analog-digital circuits, we can speed up simulation by analyzing the digital and the analog sections separately, as illustrated in Fig. 1. Our algorithm, described in Sect. II., evaluates the supply currents $i_{DD}$ and $i_{SS}$, and saves a piece-wise linear (PWL) description of current waveforms. In Sect. III., the current waveforms are used as an input for subsequent simulation of the analog section of a mixed-signal circuit. Our case study is focused on a pipeline analog-to-digital converter (ADC), which includes a two phase clock generator acting as digital noise source, and a flash ADC based on resistive string affected by digital disturbances.

II. SIMULATION ALGORITHM BASED ON CONTINUOUS FUNCTIONS

The proposed algorithm, written in C++, uses time-continuous functions, instead of sample sequences, to represent signals. The advantages of this approach are: better accuracy in the calculation of derivatives, pre-layout switching noise estimation, and faster simulation speed compared to a circuit-level simulator. Accurate calculation of derivatives is important, as voltage drops due to bonding inductances represent a major source of crosstalk in mixed-signal systems.

Let us assume that the bonding and package parasitics between the digital supply $V_{DD}$ and an analog signal $v_s$ can be modeled as illustrated in Fig. 2 [4]. The instantaneous current $i_{DP}$ due to digital switching of logic gates produces a voltage drop, which propagates to the adjacent wires through both capacitive coupling due to the capacitance between wires $C_{1,2}$ and inductive coupling due to the mutual inductance represented by $K$. The analog on-chip voltage $v(t)$ is a function of the external voltage $v_s$ and of the digital switching current $i_{DD}$ and its derivative:

$$v(t) = f\left(v_s, i_{DD}, \frac{di_{DD}}{dt}\right). \quad (1)$$

In our analysis of the digital switching in CMOS log cells, the pull-up and the pull-down branches of logic gates are modeled either as current generators (MOS transistors in the saturation region) or as resistive switches (MOS...
transistors in the triode region), in order to keep the complexity of the network at an acceptable level.

The analysis method is similar to the one described in [5]. The overall simulation time is divided into time slices, depending upon input signal variations and the operating region of pull-up and pull-down MOS devices. Within each time slice, time-continuous functions describing the output voltage \( v_{out}(t) \) and the supply currents \( i_p(t) \) (through the pull-up branch) and \( i_n(t) \) (through the pull-down branch) are calculated. When the operation region of a digital cell changes (at time \( t_c \)), an event is generated and all the digital cells are analyzed again, using the values of currents and voltage at \( t = t_c \). At any time slice, the operating condition of the pull-up and the pull-down branch of each cell is determined. The output voltage \( v_{out}(t) \) and the currents drawn from the positive and the negative supply \( (i_{DD}(t) \) and \( i_{SS}(t) \), respectively) are calculated as a function of the input voltage \( v_{in}(t) \). The use of a simple model for active elements ensures that a closed-form expression exists.

Under the above assumptions for the models of MOS transistors, when piece-wise linear external inputs are applied, all signals at the output of digital gates can be expressed in the form:

\[
v(t) = \sum_i p_i(t) \cdot e^{-\alpha_i t}
\]  

where \( p_i(t) \) is a (real) polynomial function in \( t \) and \( \alpha_i \) is a real quantity (the inverse of a time constant).

As an example, let us consider the case of a CMOS inverter having the NMOS transistor working in the saturation region and the PMOS transistor in the triode region; this occurs when \( V_{SS} + V_{th,n} < v_{in}(0) < V_{DD} + V_{th,p} \) and \( v_{in}(0) - v_{out}(0) < V_{th,p} \). Fig. 3 illustrates the simplified model used for the analysis.

The current through the NMOS transistor is:

\[
i_n(t) = K_n \cdot (v_{in}(t) - V_{SS} - V_{th,n})^2
\]

where \( K_n = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \), with usual meaning of symbols.

Assuming that the PMOS transistor in the triode region can be approximated by a resistance \( r_p \) constant over the time interval \([0, t_{max}]\), the output voltage can be obtained from the differential equation:

\[
r_p C_L \frac{dv_{out}(t)}{dt} + v_{out}(t) - V_{DD} + r_p i_n(t) = 0
\]

where \( C_L \) is the capacitive load. The solution is:

\[
v_{out}(t) = v_0 e^{-\frac{r_p}{C_L} t} +
+ e^{-\frac{r_p}{C_L} t} \int_0^t \left( \frac{V_{DD} - V_{out}(t)}{r_p} - i_n(t) \right) e^{\frac{r_p}{C_L} t} dt
\]

The current through the PMOS transistor is:

\[
i_p(t) = \frac{V_{DD} - v_{out}(t)}{r_p}
\]

If the input voltage \( v_{in}(t) \) is expressed in the form (2), a closed form solution for voltages and currents can be calculated. For the cascade configuration of logic cells, the output of any gate is used as the input for the next one.

After calculating the output voltage, we also need to determine the maximum time \( t_{max} \) for which the computed solution is valid: \( t_{max} \) is the time instant until which no change occurs in the operation region of any device in the circuit.

The average on-resistance of a MOS transistor, \( r \), depends on its gate-to-source voltage \( v_{GS} \) and, therefore, on its input voltage, through the relationship:

\[
r = \frac{1}{K [v_{GS} - V_{th}]}
\]
where the drain-to-source voltage $v_{DS}$ has been neglected with respect to the gate-to-source voltage $v_{GS}$.

To simplify the calculation, in (5) we consider $r$ as a constant over the time interval $[0, t']$, with $t'$ small enough so that the error in the value of the exponential function is below 1%. It is worth pointing out that this is an additional condition of the computation of the time interval $t_{\text{max}}$ at every step of the simulation. A more detailed description of the algorithm can be found in [6].

The proposed algorithm has been used to simulate the two phase clock generator illustrated in Fig. 4. The simulation results are shown in Figs. 5 (output voltages), 6 (currents) and 7 (switching noise due to series inductances). To obtain the switching noise waveform shown in Fig. 7, the currents calculated assuming ideal supply lines ($L_{SS} = L_{DD} = 5 \text{nH}$) were injected into the respective inductances. For comparison, Fig. 8 illustrates
III. Analysis of Crosstalk through Parasitics

To evaluate the effects of switching currents in Fig. 6 on an analog circuit, we have considered a pipeline ADC, whose architecture is shown in Fig. 9. Each pipeline stage contains the flash ADC shown in Fig. 10. The sample-and-hold (S/H), the digital-to-analog converter (DAC) and the residue amplifier are synchronized with a two phase clock generated by the circuit in Fig. 4.

We have simulated the flash ADC including the effects of the switching currents through all parasitics associated to bonding and package. Each wire has series inductance and resistance, capacitance to ground, and both capacitive and inductive couplings towards the other wires.

Fig. 11 shows the on-chip supply voltages waveforms of the analog section (nodes V_{DD} and V_{SS} in Fig. 10). Values of parasitic elements used in simulation are: inductance L = 2.5 nH, resistance R = 50 mΩ, ground capacitance C_{GND} = 15 fF, capacitance between wires C_{ij} = 5 fF, mutual inductance coupling factor K = 0.2. From the waveforms in time domain, we can see that on-chip supplies are affected by digital noise and display a “bouncing” effect with a peak value of about 10 mV, which limits the resolution of the pipeline converter to 8 bits.

IV. Conclusion

A method for the analysis in time domain of effects due to digital switching current has been presented. Current waveforms obtained through a dedicated algorithm can be used as an input for SPICE-like analysis of the analog section, to evaluate overall performance of the circuits. Disturbances generated by switching currents in digital blocks propagate through bonding and package parasitics, affecting analog voltages. Such effects must be carefully considered when designing accurate analog circuits.

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References