Systematic design and modelling of high-resolution, high-speed pipeline ADCs

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Abstract

This paper describes a suitable mathematical model for the design of high-speed, high-resolution pipeline ADCs. The effect of capacitor mismatch and finite amplifier bandwidth and gain on the converter INL and DNL are accurately modelled. On the basis of this model a design optimisation method is provided.

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1. Introduction

Pipeline Analog-to-Digital Converters (ADCs) are widely used in many high-speed, high-resolution applications such as wireless communications because of their high sampling rate and dynamic range. Indeed, resolutions in the range of 10–14 bits are achieved up to 100 MSamples/s in CMOS technologies [1–3]. A/D converters featuring higher sampling speed are reported in advanced BiCMOS technologies [4]. Switched-capacitor implementation in CMOS technology is more attractive than bipolar and BiCMOS ADCs for high-resolution applications, but their linearity decreases when the sampling frequency is higher than few megahertz. In fact, at these frequencies, small value capacitors have to be used for keeping gain-bandwidth product of the operational trans-conductance amplifier (OTA) sufficiently high, thus increasing the capacitor mismatch, which is inversely proportional to the square root of the capacitor value. For these reasons, at high frequency either foreground or background calibration techniques are mandatory for linearity enhancing.

The high-level design of pipeline ADCs involves several variables (capacitor size, OTA DC gain...
and gain-bandwidth product) affecting the converter linearity, noise and power consumption, so that the bit partitioning between the ADC stages and the selection of the stages to be calibrated should be optimised. Usually, systematic design is carried out using a simplified model of noise and Differential-Non-Linearity (DNL) only. No equations predicting the Integral-Non-Linearity (INL) are reported in literature.

This paper presents an accurate comprehensive model of noise, DNL, and INL allowing systematic design optimisation for high-resolution, high-speed pipeline ADCs. Section 2 reports a brief description of the pipelined ADC architecture and of the most important sources of non-ideality. In Section 3 a mathematical model based on worst-case equations of DNL, INL, and noise is presented. In Section 4 a design methodology based on the proposed model is described. Finally, the analytical model is validated by means of extensive Matlab simulations in Section 5.

2. Pipeline architecture

The pipeline architecture is shown in Fig. 1. Each stage consists of a sample-and-hold amplifier (SHA), a low-resolution flash ADC with \(2^{N_i}-2\) comparators, a DAC, a subtractor and a residue amplifier. The switched capacitor multiplying DAC (MDAC) drawn in Fig. 2 plays the role of SHA, DAC, subtractor and residue amplifier at the same time. The input voltage \(V_{IN_i}\) is sampled by the coarse sub-ADC and the MDAC at the same clock phase \(\phi_1\). In this phase all the \(2^{N_i-1}\) capacitors of the MDAC are connected to \(V_{IN_i}\), so that the charge at the input of the amplifier is \(Q = V_{IN_i}C_{MDAC}\), where \(C_{MDAC}\) is the total...
capacitance of the MDAC. In a second phase $\phi_2$ the capacitor $C_0$ is switched in the opamp’s feedback loop while the other capacitors are switched to ground or $\pm V_R$ depending on the value of the input code [5]. Therefore, in the ideal case, the value of the output residue will be

$$V_{O_0} = \frac{C_{MDAC} + C_{sel}}{C_0} V_{IN} + \frac{C_{sel}}{C_0} V_R$$  

(1)

where $C_{sel}$ is the sum of the capacitance connected to $\pm V_R$. Since all capacitors have nominally the same value $C$, the gain $G_i$ of the MDAC is $C_{MDAC}/C_0 = 2^{N_i-1}$.

The pipeline ADC is susceptible to several non-idealities which can limit the resolution to 10–12 bits if calibration or trimming are not used. In particular, the finite gain and the incomplete settling of the opamp, and the mismatch in the capacitors that set the interstage gain are the most relevant sources of non-linearity [6], while thermal noise arises from sampling switches and opamp [7]. The non-linearities of the $i$th sub-ADC, if not exceeding $2V_R/2^{N_i}$, are tolerated thanks to the digital correction.

3. Mathematical model

If the main opamp non-idealities such as input capacitance, finite DC gain and bandwidth are taken into account, Eq. (1) becomes:

$$V_{O_0} = \left(1 - e^{-2\pi f_T T_S A}\right) \frac{C_{MDAC}}{C_0 + \frac{1}{A} (C_p + C_{MDAC})} + \frac{C_{sel}}{C_0 + \frac{1}{A} (C_p + C_{MDAC})} V_R$$

(2)

where $f_T$, $A$, $T_S$, and $C_p$ are, respectively, the open-loop unity-gain bandwidth, the DC gain, half the clock period, and the input capacitance.

Let

$$\varepsilon_S = \exp(-2\pi f_T T_S A)$$  

(3)

$$\varepsilon_A = \frac{C_p + \sum_{k=0}^{G_i-1} C_k}{C_0 A}$$  

(4)

We include now the effect of the capacitance mismatch on the residue voltage. Neglecting the contribution of the mismatches whose amount is divided by the opamp DC gain, and considering that $C_{MDAC} = \sum_{k=0}^{G_i-1} C_k$ and $C_{sel} = \sum_{k=1}^{D_i} C_k$, where $D_i$ is the number of capacitors connected to $\pm V_R$, the residue is approximated by the following relationship:

$$V_{O_0} \approx (1 - \varepsilon_S - \varepsilon_A) \times \left(\frac{C_{MDAC}}{C_0 + \frac{1}{A} (C_p + C_{MDAC})} V_{IN} + \frac{C_{sel}}{C_0 + \frac{1}{A} (C_p + C_{MDAC})} V_R\right)$$

$$= (1 - \varepsilon_S - \varepsilon_A)\left(1 - \frac{\Delta C_0}{C}\right)\left(G_i\left(1 + \sum_{k=0}^{G_i-1} \frac{\Delta C_k}{G_i C}\right) V_{IN} + \frac{D_i}{1 + \sum_{k=1}^{D_i} \frac{\Delta C_k}{D_i C}} V_R\right)$$

(5)

Finally, the output residue can be approximated as:

$$V_{O_0} \approx (1 - \varepsilon_S - \varepsilon_A)(G_i(1 + \varepsilon_C) V_{IN} + D_i(1 + \varepsilon_D) V_R)$$

(6)

where

$$\varepsilon_C = \sum_{k=1}^{G_i-1} \frac{\Delta C_k}{G_i C} - \frac{G_i - 1}{G_i} \frac{\Delta C_0}{C}$$

(7)

$$\varepsilon_D = \sum_{k=1}^{D_i} \frac{\Delta C_k}{D_i C} - \frac{\Delta C_0}{C}$$

(8)

$\Delta C_i$ being the shift of the capacitance $C_i$ from its nominal value, arising from wafer-level effects, such as random mismatch and gradients. Obviously the shift of the nominal value due to process tolerance does not contribute to the error on the residue voltage, since such shift equally affects all the capacitors. Therefore, the error on the sampled residue is:

$$\Delta V_{O_0} \approx (-\varepsilon_S - \varepsilon_A + \varepsilon_C) G_i V_{IN} + \frac{D_i}{1 + \sum_{k=1}^{D_i} \frac{\Delta C_k}{D_i C}} V_R$$

(9)

3.1. DNL

Let suppose that the $i$th MDAC only is affected by mismatch, finite gain, and settling time errors. In this case, all the quantization cells of the final ADC will have the same width, but the cells
including the thresholds of the $i$th MDAC. It is possible to demonstrate that the DNL (in LSB) of the former cells are given by

$$\text{DNL} = \varepsilon_S + \varepsilon_A - \sum_{k=1}^{G_i-1} \frac{\Delta C_k}{G_i C} + \frac{G_i - 1}{G_i} \frac{\Delta C_0}{C}$$  \hspace{1cm} (10)

The DNL error of the cells close to the threshold of the MDAC under evaluation can be estimated from (9). Let assume, in fact, that $E_{U,J}$ and $E_{D,J}$ are the errors in the residue when the input value $V_{IN_i} = V_R (J - 0.5)/G_i$ is approximated from the left and, respectively, from the right side (see Fig. 3), i.e.

$$E_{U,J} = (-\varepsilon_S - \varepsilon_A + \varepsilon_c)(J - 0.5)V_R$$

$$- (-\varepsilon_S - \varepsilon_A + \varepsilon_d)(J - 1)V_R$$  \hspace{1cm} (11)

$$E_{D,J} = (-\varepsilon_S - \varepsilon_A + \varepsilon_c)(J - 0.5)V_R$$

$$- (-\varepsilon_S - \varepsilon_A + \varepsilon_d)V_R$$  \hspace{1cm} (12)

Therefore, the DNL of the cell including the threshold $J$ of the $i$th MDAC is given by

$$\text{DNL}_J = (E_{U,J} - E_{D,J}) \frac{2^{m_i - 1}}{2^{m_i - 1} V_R}$$

$$= 2^{m_i - 1} \left[ - (\varepsilon_S + \varepsilon_A) + \frac{\Delta C_J}{C} - \frac{\Delta C_0}{C} \right]$$  \hspace{1cm} (13)

where $m_i$ is the overall resolution of the stages following the $i$th MDAC. From (10) and (13), it is apparent that the DNL of the whole ADC reaches its maximum value close to the thresholds of the first MDAC, and the worst case DNL can be estimated to be

$$\text{DNL}_w = 2^{m_i - 1} \left[ - (\varepsilon_S + \varepsilon_A) - 2 \frac{\Delta C}{C} \right]$$  \hspace{1cm} (14)

The capacitor mismatch $\Delta C$ can be modelled as a Gaussian random variable, whose standard deviation is evaluated by recalling an approximated form of the Pelgrom’s law:

$$\sigma_{\Delta C} = k_c \sqrt{C}$$  \hspace{1cm} (15)

where $k_c$ is a technology dependent parameter. For design purposes, $\Delta C$ can be replaced with $3 \times \sigma_{\Delta C}$ in the worst-case DNL expression.

3.2. INL

The INL errors corresponding to a generic quantization cell can be evaluated by summing the DNL errors of the previous cells. Assuming a positive DNL for the quantization cells (but the ones bounded by the threshold of the $i$th MDAC), the INL is a steadily increasing function of the cell’s position along the ADC characteristic, until we arrive at the threshold of the MDAC under evaluation. At this point the INL function exhibits a step, see (13). Since it is easy to prove that the INL is maximized at one of the cells including the threshold of the involved MDAC, the analysis can be restricted to such cells. The INL of the cell corresponding to the threshold $V_{IN_i}/V_R = (J - 0.5)/G_i$ is given by

![Fig. 3. The true (—) and the ideal (---) input–output characteristic of the $i$th MDAC.](image-url)
\[ \text{INL}_J = \left[ \frac{3}{2} + (G_i - J) \right] 2^{m-1} \left( \varepsilon_S + \varepsilon_A - \varepsilon_C \right) \]
\[ + \sum_{k=J}^{G_i-1} \text{DNL}_k \]

The worst-case INL can be found for \( J = G_i/2 \), thus leading to
\[ \text{INL}_w = 2^{m-1} \left[ \frac{\varepsilon_S + \varepsilon_A}{2} + \frac{G_i - 1}{2} \frac{\Delta C}{C} \right] \]

As for the worst-case DNL, \( \Delta C \) should be substituted by \( 3 \times \sigma_{\Delta C} \) (15).

3.3. Noise

A simplified noise model for the MDAC is reported in Fig. 4.

The main noise sources of the MDAC in Fig. 2 are the input-referred noise voltage of the opamp, \( e_{n,\text{REF}} \), the thermal noise of the on-resistance of the switches, and the noise voltage contributed by the reference generator.

As referred in Section 1, the MDAC exhibits two phases which correspond to two different circuit arrangements. The noise voltage affecting the converter's SNR is the sum of the rms noise voltages evaluated at the end of the residue amplification phase at the output of the MDACs. As a first approximation let we assume that the noise contributions of the \( J \)th MDAC in the two phases are almost independent. This assumption allows to obtain the overall MDAC noise, by superposition of the two noise power terms.

In the sampling phase the inputs and the output of the opamp are shorted to ground, so that the contribution of the opamp noise is negligible in this phase. On the contrary, the thermal noise of the on-resistance of the switches is integrated by the total MDAC capacitance, \( C_{\text{MDAC}} = G_i C_0 \), at the bottom-plate terminal of the capacitors [7], Fig. 4a,

\[ v_{n,\text{IN}} = \sqrt{\frac{kT}{C_{\text{MDAC}}}} \]

where \( k \) is the Boltzmann constant. At the transition from the sampling to the residue amplification phase, \( v_{n,\text{IN}} \) is sampled and transferred to the opamp output, leading to the noise contribution from the sampling phase, \( v_{n,\text{S}} \), equal to:

\[ v_{n,\text{S}} = G_i v_{n,\text{IN}} = \sqrt{\frac{G_i kT}{C_0}} \] (19)

Notice that the opamp input capacitance, \( C_p \), does not contribute to the overall noise, the input terminals being shorted to ground. During the residue amplification phase, Fig. 4b, a voltage feedback is established and both the thermal noise voltage due to the switches and the input opamp noise are transferred to the output and their spectra are shaped by the transfer function of the amplifier. Assuming a single-stage opamp, the noise bandwidth of the amplifier in Fig. 4b is

\[ B_{eq} \approx \frac{\pi}{2} \frac{g_m}{2 \pi C_L G_i} \]

where \( g_m \) is the transconductance of the input pair and \( C_L \) is the overall loading capacitance of the opamp in this phase.

\[ C_L = \frac{(G_i - 1)C_0 + C_p}{G_i + C_p/C_0} + C_{MDAC} + C_{ADC} \] (21)

\( C_{MDAC} \) (\( C_{ADC} \)) being now the input capacitance of the next MDAC stage (of the next flash ADC, respectively).
The opamp input noise is mainly contributed by the output noise current from the MOS input pair
\[ i_n = \sqrt{4\gamma kTg_mB_{eq}} \]  
with \( \gamma \) ranging from 2/3 to 3 depending on the process and on the gate length. The input noise voltage is readily evaluated from \( i_n \) as \( e_{n-oA} = i_n/g_m \). The contribution of the noisy reference generator \( \pm V_{R} \) is modelled with an equivalent noise resistance, \( R_R \). Therefore, the rms noise voltage at the opamp output related to the residue amplification phase is
\[ v_{nRA}^2 = G_i^2 B_{eq} \left( 4KTR_{ON} + 4KTR_R \frac{4\gamma kT}{g_m} \right) \]  
where \( R_{ON} \) is the on-resistance of the switches connecting the top plates of all the capacitors \( C_1, \ldots, C_{G-1} \). Assuming that the switch size is scaled together with the capacitance value, \( R_{ON} \approx R_{on}/G_i \). Finally, the overall output noise of the MDAC stage is obtained by summing the contribution related to the sampling and to the residue amplification phase [9]
\[ v_{nO}^2 = \left[ \frac{G_i kT}{C_0} + 4kT (R_{ON} + R_R) \frac{g_m G_i}{4C_L} + \frac{\gamma kT G_i}{C_L} \right] \]  

4. Model-based design methodology

In a reasonable design approach for high-resolution pipeline ADCs, the maximum allowed INL, DNL, and output noise should be evaluated at first. In order to achieve an effective resolution higher than \( N - 1 \) bit, where \( N \) bit is the nominal resolution, both the DNL and INL should be below 0.5 LSB and the total output noise should be well below the quantisation noise.

It has to be remarked that, commonly, the design is carried out by using a simplified relation for the DNL, without the contribution arising from the finite opamp’s gain and bandwidth [8]. Moreover, the INL contribution is not considered even though it can limit the overall linearity.

From the proposed equations (14) and (17) it is possible to see that, in order to ensure a maximum INL (DNL) less than \( \text{INL}_w \) (\( \text{DNL}_w \)), respectively, the DC gain, the unity-gain frequency of the amplifier, and the minimum value of the capacitors of the MDACs should be
\[ A \geq \frac{G_i 2^{m+1}}{\min\{\text{DNL}_w, \text{INL}_w\}} \]  
\[ f_T \geq \frac{G_i}{2\pi T_S} \left( (m+1) \ln 2 - \ln(\min\{\text{DNL}_w, \text{INL}_w\}) \right) \]  
and, respectively,
\[ C \geq \left( k_c / \min \left\{ \frac{\text{DNL}_w}{2^{m+1}}, \frac{3\text{INL}_w}{G_i - 1} \right\} \right)^2 \]  
Similarly, a different constraint on the minimum value of the sampling capacitors can be obtained from (24).

Nevertheless, while the noise contribution cannot be removed, the non-linearities arising from capacitor mismatch and opamp limitations can be removed by either background or foreground calibration. Therefore two lower bounds for the feedback capacitance of each stage can be determined by noise and linearity requirements. While the former should be always satisfied, the latter can be removed by resorting to digital calibration. Because of its impact in terms of silicon area and power consumption, the calibration will be introduced only when the minimum capacitance imposed by linearity requirements is larger than a threshold, that can be considered a design parameter.

5. Simulation results

The procedure described in the previous section has been automated by means of a dedicated software and has been applied to the design of a 14 bit, 100 MSamples/s ADC. Some results are reported in Fig. 5, where the x-axis represents some possible pipeline architectures. The labels refer to bit numbers in the converter stages, from the first to the last one. For instance in a 42222223 architecture first stage, stages from the second to the eighth, and last stage exhibit a nominal resolution of,
respectively, 4 bit, 2 bit and 3 bit. Architectures 422...23 and 332...23 are two sub-optimal choices with respect to the ADC input capacitance (which impacts the input track-hold requirements) and the OTA requirements (load capacitance $C_{MDAC}$ and $f_T$) for the first stage MDAC. Such OTA requirements can be fulfilled using a 0.18 μm CMOS technology.

In order to validate the mathematical model, a MATLAB model of the ADC (332...23 architecture) was implemented based on the Eqs. (2)–(6) together with (19). Capacitor mismatch parameter $k_c$ and $\gamma$ noise factor were derived from a digital 0.18 μm CMOS technology.

Since the proposed design methodology is based on the assumption that worst-case DNL and INL are mainly affected by the non-idealities of the first stage, Montecarlo simulations of the complete converter has been performed. Simulations with capacitor mismatch and OTA limitations in the first stage only shown that the maximum DNL and INL occur, as expected, close to the thresholds of the ADC in the first stage.

A more realistic Monte Carlo simulation was performed with all the stages affected by capacitor mismatch and OTA limitations. The returned maximum DNL and INL (least-squares fit definition) are shown in Fig. 6. The maximum values
still occur close to the thresholds related to the first stage. In addition, the comparison between the simulation results and the value predicted by the analytical model (14) and (17) demonstrates the effectiveness of the a priori estimation of the maximum DNL and INL without any calibration. Introducing digital calibration for the first three stages, the maximum INL decreases below 0.6 LSB. Finally, a complete converter model in a behavioral circuit description (Verilog-A) was implemented. This electrical model allowed to verify the performances of the MDAC with a relatively short simulation time, with respect to a transistor-level implementation. Fig. 7 points out a good agreement between Verilog-A and transition level implementation; indeed, at the sampling point (arrow) the returned residues differs by a fraction of LSB.

The behavioral model of the OTA was based on the specifications (DC gain, bandwidth and maximum input capacitance) provided by the analytical model described in the previous section. The circuit simulation provided an error on the output residue in good agreement with the high-level analytical model. Nevertheless, even if the Verilog-A model allows the simulation of the complete 14-bit ADC, the required simulation time does not permit an extensive Monte Carlo simulation.

6. Conclusions

An improved model of CMOS pipeline ADCs has been presented, allowing estimating the effect of capacitor mismatch and finite opamp bandwidth and gain on the DNL and the INL. A design methodology for the optimisation of high-speed, high-resolution ADCs has been described and Monte Carlo MATLAB simulations, validating the analytical model, have been provided.

References