Process Control for 45 nm CMOS logic gate patterning.

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ABSTRACT

This paper presents an evaluation of our CMOS 45nm gate patterning process performance based on immersion lithography in a production environment. A CD budget breakdown is shown detailing lot to lot, wafer to wafer, intrawafer, intrafield and proximity CD uniformity characterization. Emphasis is given on scatterometry library development and deployment. We also look more into detail to focus effect on CD control. Finally status of overlay performance with immersion lithography is also presented.

Keywords: 45nm logic gate, immersion lithography, scatterometry, CD uniformity.

1. INTRODUCTION

CMOS 45nm is the first technology using immersion lithography. In the early phase of immersion process development, process was quite limited by overlay performances of the tool and also by photo resist imaging. In these conditions it has been decided to pattern the gate using “double patterning” scheme for the SRAM blocks. With such approach, end cap (line end) in the SRAM (which is pattern with a specific lithography step) is not correlated to CD and overlay control of the gate and is therefore no more a bottleneck factor for gate process development.

A 45nm gate is really challenging by its CD range control in all aspects. After the setup of the double patterning integration scheme, most of our activity was focused on CD budget breakdown with special attention to immersion cell process performance. However, in this paper most of the CD analysis data will be shown after the complete patterning of the gate.

Breaking down our CD budget quickly lead us into the need of extensive metrology and as such, to the need of extensive development of scatterometry.

All along this paper we present the current CD control performance of CMOS 45nm gate patterning using immersion lithography and outline the coming actions we think are needed to breakthrough the 3 sigma challenge. Overlay is also reported in a less extensive manner.

2. GATE PROCESS INTEGRATION

Our 45nm gate patterning integration scheme is based on our 65nm gate patterning scheme using amorphous carbon / Dielectric ARC stack as antireflective and Hardmask [1]. However, if for the logic (like in our CMOS 65nm), the pattern is defined in a single exposure, the end cap control in the SRAM in CMOS 45nm is using a second photo/Etch “assist” step to perform the line cut. This has led us to introduce an intermediate Hardmask.

Also due to the hyper NA imaging we had to adapt our DARC which is now a double oxide layer with properly tuned n,k [2]. With such anti reflective layers we are able to control the resist swing effect within 1nm. On figure1 we see typical swing curves registered for immersion process, showing important bulk effect but rather low swing amplitude at working setpoint.
Fig 1: Normalized swing curves (experimental + fit) observed for four critical CMOS 45nm patterns using immersion lithography.

Another important point in this integration scheme (double photo / double etch described on figure 2) is the second photo steps which does not play any role in CD (L poly) control. The resist line defined after the first photo steps are trimmed down during the intermediate Hardmask Etch. The final etch poly steps brings down the pattern to the desired target.

Fig 2: double patterning integration scheme chosen for CMOS 45nm logic Gate patterning. Both photo steps are immersion lithography steps.

3. CD CONTROL PERFORMANCE EVALUATION

3.1. Average CD regulation

From the 2 photos and 2 etch steps, CD is dynamically controlled at Photol and Etch1 like shown on figure 2

1: A multivariate Run to Run system is used to control Photo CD centering [3]. This system includes feedforward (Reticle maskshop CD bias & error datas / Scanner Spot sensor / Product target) and feedback effects (Scanner / Layer / Mask effects) which are dynamically controlled. Using such system, average lot CD can be controlled without rework within ± 2nm.
2: Etch1 process is based on resist trim which is adjusted by a feedforward loop, compensating any average CD miscentering (within ±2nm) at Photo1.

3: The second photo step doesn’t impact Gate CD and the final etch process is running at fixed bias.

Feedforward / feedback loop quality is strongly relying on metrology residual noise level which can be reduced by higher sampling or improved metrology methods. At the start of CMOS 45nm development, CD’s were measured using CDSEMs. Residual noise was not good enough and the throughput not acceptable to increase the sampling plan. Today for CD regulation, scatterometry has been deployed allowing us to sample 8 wafers per lot with 17 points per wafer.

3.2. CD metrology Setup

Due to the stack used at Photo1, the development of the libraries was not straightforward. Some publications are available regarding the development of scatterometry libraries on APF stack for our CMOS 65nm process [4].

Several DOE’s were ran to set up scatterometry library which demonstrates stable behavior with respect to polysilicon / TEOS hardmask / amorphous carbon and oxides DARC thickness variations and also with respect to n,k from the DARC stack. The CD measurements were calibrated with SEM (after photolithography) and SEM&TEM (after etch) on exposure matrix wafers. Before switching to scatterometry as primary measurement for process control, double data collection has been performed during about 8 weeks of production. Figure 3 shows the CD correlation results between top down CDSEM measurements after photo1 and etch2 and also with TEM cross section after etch2.

For photolithography the first running version of the library (with which we have done most of the CD budget work) was using 5 levels of freedom. In order to continuously improve the CD measurement, a second library with 7 levels of freedom is being developed which shows better response in term of stack variations.

3.3. CD budget breakdown

As a start for CMOS 45nm process development, a target level of 4.5nm (3σ) CD dispersion after Etch has been set (for transistors). This budget includes (i) Lot to Lot (ii) Wafer to Wafer (iii) Within Wafer (iv) Intrafield (v) Proximity effects. Our goal is to use scatterometry for the first four items while proximity effect would be integrated in the OPC model which is characterized by CDSEM. In parallel, some works are on going to evaluate real impact of line width roughness (LWR) on device performance and this is why it is not reported in the budget.

The current evaluation and progression of this CD breakdown (after etch) is described on figure 4, details regarding these values are reported later in this paper.
3.3.1. Lot to Lot CD control

As said earlier the CD lot to lot control relies on Photo Run to Run system and Photo – Etch feedforward loop. Once the scatterometry model has been generated and validated, CDSEM measurement has been replaced by optical CD measurement as lead metrology. Doing so, we could double our sampling scheme and still increase the measurement throughput. The most significant interest of scatterometry was a drastic reduction of the measurement residual noise enabling a better Run to Run regulation at photo and etch. As an example we can see on figure 5 the difference in term Min/Max CD range (in µm) per lot observed with scatterometry on the left side and CDSEM on the right side after photolithography.

![Normalized Min/Max CD per lot observed over the same period with scatterometry (left side) and CDSEM (right side)](image)

In line specs could then be set to ± 2 nm for CD average at photo, the remaining error being corrected by the feedforward loop between Photol and Etch 1. CD dispersion after photolithography and after etch using scatterometry are represented on figure 6. Two periods are represented, one (left) during the implementation phase of the feedforward and the other (right) after stabilization of the process.

![Observed in line CD dispersion (after Photo1 and Etch2) over (left) 2 month period in Q4/07 and (right) over last month Q1/08](image)
On this graph, photolithography process looks much more stable than etch process but this picture may be too optimistic for photolithography. If fact, we’ll see later that if etch process can have its own signature, some part of it is induced by photolithography focus control.

3.3.2. Wafer to Wafer process control

Using scatterometry we could afford measuring up to 8 wafers within a lot. Whether we should measure all the wafers or not was indeed questioned. It means that we would correct process trim time, at wafer level. This option is possible and still open. In our development history and still today we regularly measure full lot, fullmap. We also decided to use the immersion cell with a maximum of process units (3 coaters, 7 PAB, 7 PEB plates, 4 developer module, dual chuck) in order to be able to run at a throughput above 120 wafers per hours and really evaluate the immersion cell in production mode.

We still see some moderated process module effects. A typical intralot signature can be seen on figure 7a. Intra lot signature is not really significant and moreover looking back after etch, tuning trim time per wafer could even induce more noise. We should rather correct for a trend than for a single wafer information.

From photolithographic point of view, modules matching are controlled off-line on structures with aggressive pitches. With such criterias coater, PEB, developer module or chuck effects can be easily detected (see figure 7b).

![Fig 7a: Intralot CD average trend (photo1 & Etch2)](image1)

![Fig 7b: CD trend and dispersion from 25 photolithography monitor wafers](image2)

Basically after photo, beside module matching effects, we systematically see slight begin to end batch trends (<0.5nm in amplitude), effect which is also visible on scanner monitoring. In this case we tend to think of lens heating effects. We are now in a position to see tiny CD signatures across wafers and or batches. The lens heating model, for example, is a parameter we know we can improve especially when using multi-pole illumination. From this side investigations are still one their way. In fact if we trace resist side wall angle, it shows same kind of trend as CD (figure 8). These are evidences that focus control and so, resist side wall angle, will also start to show up in CD dispersion evaluations.

![Fig 8: CD and Resist Side Wall Angle trend within a batch of 25 photolithography monitor wafers from the immersion cell.](image3)
3.3.3. Intra Wafer process control

Our in-line sampling checks 17 points per wafer. For process setups and also for variance analysis many lots were also measured fullmap / full lot after photolithography and etch, using scatterometry.

In the early phase of process development we typically saw the intrawafer signatures shown as reference process on figure 9. This radial signature was, after etch, systematic on all the measured wafers. At that time we decided to tackle this issue from two angles. First one was from etch process side and the second one from photo lithography process side using intrawafer dose correction sub-recipes.

Intrawafer dose correction using scanner exposure sub-recipes generated by the dose mapper® application was tested. The sub-recipe was generated from an intrawafer profil average from about 100 wafers mapping. We could remove the radial signature but in parallel etch process was improved and the center edge effect was removed [5]. Finally, intrawafer dose correction was set aside.

![Diagram showing intrawafer dose correction process](image)

Fig 9: Intrawafer critical dimension profiles evolution along the gate patterning brick, using dose mapper® subrecipes (on top) and etching chuck temperature tuning (at the bottom)

From these experiments we also realized that using exposure dose as the only knob to control CD could be dangerous. We start then to pursue our evaluation looking more carefully at the focus effect on CD budget. Wafers with Focus Exposure Matrix and fixed focus shift were exposed and extensively measured by scatterometry inter and intrafield. Basically 74 fields per wafers with 22 measurements per fields (say 1628 points per wafer up to 3mm from wafer edge) were done. Radial presentation of typical CD profiles and uniformity are represented on Figure 10.

![Graph showing radial representation of CD profiles](image)

Figure 10: Radial representation of typical intrawafer CD profiles for different focus exposure shifts after Etch2 and Photo1.
We observe that tiny CD variations after photo are amplified after etch (especially at wafer edge) and also that focus shift induces large etch CD variations strongly impacting etch Bias (see Figure 11a). So to estimate intrawafer CD uniformity performance from photolithographic process, we should consider that a part of the variation seen after etch is coming from lithography. On the graph (Figure 11b), CD variations after photo are within 1 to 1.5 nm $3\sigma$, while they reach 3nm $3\sigma$ after etch. Most probably, a non negligible part of the difference could be directly attributed to focus or resist sidewall angle variations.

![Graph showing CD variations after photo and etch](image)

Fig 11: (a) Evolution of etch bias with respect to defocusing (b): 3 sigma intrawafer CD variations after Photo1 and Etch2.

### 3.3.4. Intra Field process control

Intrafield CD control is less easy to do in-line. Our strategy (outside scanner monitoring itself) has several aspects.

1. First, we need to insure that reticle will be delivered with an acceptable CD range. Since many years, work is done with the maskshop to improve mask CD uniformity and also to improve mask CD error feedback. The ultimate idea is to correct the mask CD error map (so 2D correction) in the feedforward system.

2. The second aspect is more linked to in-line control of intrafield CD. This will rely on in-field dropped scatterometry targets from which positions and CD mask errors will be known. In the first phase engineering recipes are created to measure these in field targets, giving us feedback. Depending on the mask, we can have tens of scatterometry targets dropped in the field.

3. Since focus will play an important role, we also introduced focus Reticle Shape Correction® (RSC) which is an option on the scanner. It allows focus compensation of distortions from the reticle on the reticle stage (reticle glass plate distortion and clamping).

Mask CD error dispersions is quite stable like seen on Figure 12.

![Table showing CD error dispersions](image)

Fig. 12: Distribution of the average mean to target errors (at wafer level including MEEF) measured at maskshop on incoming reticles
We have investigated the use of Dose Mapper® for intrafield mask bias correction. This work is on going for its implementation as a regular procedure for incoming reticles. The concept is to get the mask CD error map and generate a corresponding intrafield dose correction recipe. To validate the concept, experiments have been done with different level of feedforward corrections (figure 13). To insure proper statistic, two fullmaps wafers (like in chapter 3.3.3) have been measured for each conditions. Results are encouraging but still require deeper characterization.

![Intrafield CD distribution using Dose Mapper® subrecipes generated from mask CD error map.](image1)

As we already said, dose is probably not the only knob to use and intrafield is certainly not only mask CD / Scanner dose uniformity composite. We also investigated focus effect at intrafield level. The best way to put in evidence the intrafield focus effect is to compare results with and without Reticle Shape Correction. For this, two time two wafers were exposed with focus matrixes, with and without Reticle Shape Correction. They are measured the same way as reported on the previous chapter. When looking at intrafield CD dispersion (from this given pattern) it is clear that compensating from reticle focus distorsion on the reticle table significantly opens up the process window. It does not really improves intrafield CD uniformity at best focus, but it stabilizes it across process window (figure 14).

![Intrafield CD 3 sigma dispersion measured after photolithography on focus matrix wafers with and without Reticle Shape Correction](image2)

Like reported for intrawafer effects, de-focusing will introduce CD deviations after etch. Within the focus window where photo CD uniformity stays within 1nm, we see that after etch this will be increased by 50 to 100% (figure 15 a&b)

![Intrafield CD uniformity From FEM wafer at best dose](image3)

![Intrafield CD uniformity From Fullmap wafers at best dose with focus shifts](image4)
3.3.5. Proximity effects – OPC

From the beginning a lot of attention has been paid to the OPC.

1. First the model used is a process window aware model taking into account focus and dose variability.
2. Second, etch contribution is being used to optimize the model. Therefore we always look and report data after etch.
3. Third, using process aware model we could get a safer positioning of process set point with respect to OPC-hotspots, and also more stable CD versus pitch trend across process window.
4. Fourth, due to the double patterning scheme we could afford less restrictive rules on scatterbar size.

Amongst all the checks that can be done for the OPC model, CD versus pitch behavior and hotspot window centering are the one we more carefully look at. In the last model, CD range across pitches was checked within process window after etch. On the two graphs (figure 16) CD versus pitch data after etch are presented across dose and focus.

![Fig 16: CD versus Pitch after etch observed across dose and focus (focus steps = 50nm).](image)

It is observed that CD range remains within 2 to 2.5nm across the process window. It is also interesting to note that focus (within our DOF window) has more impact on global CD for all the pitches than on iso-dense bias itself. Thanks to the process aware model we can be quite confident on the stability of this proximity effect within dose and focus window. However, these data also reveal once again, how large etch CD shift can be when photo focus is shifting by even 50nm.

3.3.6. CD budget evaluation conclusion

Hunting sources of CD variances is a neverending story. Overall, the immersion cell shows a good level of performances. During this evaluation, we could show that focus is probably now one of the main CD variance contributor.

Focus effect needs to be investigated with etch bias. We are now deploying a new scatterometry library from which resist sidewall angle information can be used by the photo etch feedforward loop.

4. IMMERSION CELL OVERLAY PERFORMANCE EVALUATION

4.1.1. Overlay and wafer timing

Immersion overlay is facing new challenges. One of them is related to the track / scanner timing. We saw regularly wafers presenting translation shifts and/or instability in intrafield. It was quickly related to variations of delay time between two wafers and therefore throughput matching between track and scanner (figure 17a and 17b)
Fig 17: (a) Typical within lot overlay translation behavior observed  (b) Corresponding exposure delay timing.

The first action was then to insure that scanner is always bottleneck. We can also remark that intrawafer overlay uniformity was also not optimum. Since then, many improvements have been done leading to seriously improved overlay performance. In order to properly monitor overlay up to 7 wafers are measured on critical layers and systematic full lot measurement is done for the CONTACT to GATE.

4.1.2. Overlay performances

On the following charts (figure 18a & b) are reported typical registration error distributions (2 month period) for Gate & Contact overlay. Knowing that we still have improvement actions to be deployed to tighten overlay control, we can say that the immersion cell performance is compliant with 45nm process requirements

Fig 18: 8 weeks overlay distribution (a) GATE to ACTI (7 wafers / lot) (b) CONT to GATE (25 wafers / lot)

5. CONCLUSION

Along this paper we have shown that keeping CD uniformity within range require a lot of attention on many contributors. The immersion process really shows good performances. If exposure dose, process temperature, etch trim conditions are well controlled, it is clear that focus effect is taking a significant part of the budget and at all levels, lot to lot, wafer to wafer, within wafer and field and also for proximity.

Looking back at these CD uniformity results along with overlay data, we can say that immersion is ready for production. There are still a lot of improvement actions in the pipe (i) Scanner hardware-software (ii) track hardware (iii) new resist materials (iv) mask process improvement (v) new options in feedforward / feedback loop system etc…

The next challenge of this work will be a development of focus feedforward / feedback loop methodology. Today a lot of attention is paid to focus budget because it is not easy the measure directly and even less easy to control in line.
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