Investigation of Digital Sensors for Variability Characterization on FPGAs

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Abstract—In this paper, we address the variability problems in FPGA devices both at design-time and at run-time. We consider a twofold approach to compensate variations, based on measurements issued from digital sensors implemented with FPGA building blocks. We compare two digital structures of sensors: the Ring Oscillator and the Path Delay Sensor. The Ring Oscillator allows a fine grain variability characterization thanks to a tiny replicable hard-macro structure (2 Slices). Although less accurate, we show that the Path Delay Sensor has a lower total area overhead as well as a smaller latency compared to the ring oscillator implementation. In our experiments conducted on Spartan-3 FPGAs, the ring oscillator is used to perform intra-chip cartographies (1980 positions), while both sensors are then compared for characterizing inter-chip performance variations. We conclude the two structures are efficient for fast variability characterization in FPGA devices. The Ring Oscillator is the best structure for design-time measurements, whereas Path Delay Sensor is the preferred structure to allow rapid performances estimations at run-time with a minimal area overhead.

I. INTRODUCTION

Variability has become a major issue with recent technologies in the semiconductor industry [1]. While process variations impact process, supply voltage and internal temperature [2], chip performances are also dependent on environmental and on applicative changes that may further influence chip’s behavior [3].

Field-Programmable Gate Arrays (FPGAs) devices are not spared by these unpredictable disparities. As underlined in [4], both inter-die and within-die variations affect FPGAs. So, it is necessary to implement solutions in order to compensate these variations.

Because of their inherent reconfigurability, it is possible to place a component of a design at a specific place on the FPGA floorplan, and to relocate it when it is required. In the literature, it has been suggested either to model FPGA variability [5] [6], or to measure it [7]. Both methods suggest then to constraint or to adapt the design so that it takes into account these variations and improves performance yield.

In this paper, we investigate the problem of variability characterization on FPGA. We provide a twofold method for variability compensation based on digital sensors used either at design-time or at run-time. Our study is focused on digital sensors, directly implemented in the FPGA building blocks. Their role is to measure the effective performance of the device. The novelty of this paper is that we compare two digital sensor structures, analyze their accuracy and area overhead in order to determine how they could be efficiently used to characterize the variability of any FPGA. In the scope of this paper, experiments was conducted on Xilinx Spartan-3 FPGAs.

The remainder of the paper is organized as follows. The next section presents the related works in the area of variability analysis and compensation techniques on FPGAs. Section III introduces a new multi-level compensation flow. In section IV, two digital sensors are presented to measure performance variations. Finally, in section V, results are exposed and discussed: overhead comparison, experimental setup, intra and inter-chip comparisons are analyzed to determine the efficiency and the accuracy of the provided digital sensors.

II. RELATED WORKS

Few recent papers suggest techniques to characterize and compensate performance variability on FPGAs. A first approach is based on modelization. Three papers have suggested theoretical techniques [5] [6] [8]. They are all verified through timing modeling. First, a multi-cycle Statistical Static Timing Analysis (SSTA) placement algorithm is exposed in [5]. In simulation, it is possible to improve performance yield by 68.51% compare to a standard SSTA. A second approach proposes a variability aware design technique to reduce the impact of process variations on the timing yield [8]. Timing variability is reduced thanks to the increase of shorter routing segments. Another side, the author of [6] confronts different strategies for compensate within-die stochastic delay variability. Worst case design, SSTA, entire FPGA reconfiguration and sub-circuits relocation within a FPGA are considered. SSTA provides better results than Worst case design although both reconfiguration methods allow significant improvements. However, in these papers, only theoretical techniques and simulated results are exposed.

A second approach is based on delay measurements [7]. In this paper, a ring oscillator is placed on the FPGA. The frequency of each oscillator is measured. A cartography of the chip is done. Nevertheless, the study proposes here to characterize 8 LUTs together as well as the impact of external variation is not introduced.

These two sorts of approaches suggest it is required to have two stages of characterization with digital sensors: one off-line and one on-line.
III. MULTI-LEVEL COMPENSATION FLOW

In order to tackle FPGA variability issues, a multi-level compensation flow is proposed. Basically, it uses FPGA digital resources (LUTs and interconnects) to implement Hard Macro sensors. An overview of our methodology is depicted in Figure 1. It is divided into two parts. In the first phase, the FPGA performance is deeply analyzed off-line at a fine granularity by our dedicated monitors. At run-time, a reduced monitoring setup is implemented within the system itself, in order to check the run-time performances. Each level is further explained in the two following sections.

A. Off-line monitoring and module placement strategy

The first step of the flow is depicted in Figure 2 and is divided into two global parts: the FPGA characterization and the module placement strategy. The monitoring system is directly applied at the technological level, i.e. it is intended to check at a fine granularity intrinsic performances of the FPGA device.

In order to realize an accurate characterization of performances, an array of sensors covering the whole area is used (Fig.2(a)). Sensor data are collected and analyzed to build a cartography of the floorplan (Fig.2(b)).

Once the cartography of the FPGA is built, a placement strategy is performed, considering both the system and its run-time monitoring service (Fig.2(c)). Basically, it consists in placing critical modules on “best performance” areas. A subset of on-line sensors is also implemented within the system in order to check at run-time the evolution of the performances. The sensor placement strategy takes into account requirements of run-time modules as well as the result of the off-line cartography.

B. On-line monitoring and dynamic compensation

The second stage of the compensation flow is based on hardware run-time monitoring. The run-time system implemented in the FPGA is composed of a microprocessor, some peripherals, a Management Unit (MU), a set of sensors and actuators. The on-line monitoring process is illustrated in Figure 2(c).

Our objective is to perform a dynamic compensation of system variations. For this purpose, a subset of digital sensors using the FPGA resources is implemented. Digital sensors measure performances; data monitoring are then collected and analyzed by a management unit. Based on the information available, this unit can adapt the system to the actual performances; for instance, it is possible to adjust the frequency with a DFS actuator (Dynamic Frequency Scaler).

As depicted in the figure 1, a deeper FPGA performance analysis can be triggered when the management unit identifies suspicious system behavior. A partial or total analysis can be then performed in order to build a new cartography and to update the module placement strategy.

IV. DIGITAL HARDWARE SENSORS IN FPGA

The objective of the previously described compensation flow is to adapt the system in relation to the effective performances of the FPGA device. Next, we study how to measure locally and globally this performance. The idea developed in this paper is to use digital hardware sensors designed with internal resources of the FPGA, namely CLBs and switch matrices. In this section, we present the principle and the implementation of two structures: a Ring Oscillator and Path Delay Sensor.
A. Ring Oscillator Sensor

The Ring Oscillator Sensor is based on the measurement of the oscillator frequency. In [9], the author exposes an internal temperature sensor for FPGA. The frequency of a ring oscillator is measured and converted into temperature. However, the ring oscillator is implemented into an old technology where process variability is very low.

An update of this sensor is exposed here. Its structure is depicted in Figure 3. The main part of the sensor is a \( 2p + 1 \) inverter chain. The oscillation frequency directly depends on the FPGA performance capabilities. The first logic stage enables the oscillator to run for a fix number of periods of the main clock. The flip-flop at the end of the inverter chain is used as a frequency divider and allows filtering glitches from the oscillator. The final logic stage counts the number of transitions in the oscillator and transmits the count result. Then, the count result is used to calculate the oscillator frequency as follows:

\[
F = \frac{\text{count} \cdot f}{p} \tag{1}
\]

where \( F \) is the ring oscillator frequency, \( \text{count} \) is the 14-bit value of the counter, \( f \) is the operating frequency of the clock and \( p \) is the number of enabled clock periods for which the sensor is active.

B. Path Delay Sensor

In ASIC, in order to estimate the speed of a process, sensors for Critical Path Monitoring (CPM) are used. A. Drake presents a survey of CPM [10]. It exists a lot of techniques to manage Critical Path but very few are used in FPGAs. The Path Delay Sensor proposed here is directly inspired by CPM. The structure of the Path Delay Sensor is depicted in Figure 5. The idea of the Path Delay Sensor is to adapt CPM to FPGA. Indeed, the regularity of the FPGA structure enables to create more easily a critical path replica in FPGA than in ASIC.

The Path Delay Sensor is composed of \( n \) LUTs and \( n \) flip-flops (FF). The LUTs are chained together and a FF is set at the output of each LUT. A clock signal is applied to the chain and is propagated into the LUT. At each rising edge, a \( n \)-bits thermometer code is available at the output of FFs. This thermometer code is representative of LUTs and interconnects performances.

\[
T = \frac{N_z + 2}{f} \tag{2}
\]

where \( f \) is the frequency of the clock signal applied to the sensor and \( N_z + 2 \) represents the number of crossed LUTs over one for the crossing of the sample rate FF. The time \( T \) measured here enables to fast estimate the maximum frequency of one critical path.

In order to have relevant information, the size of this sensor must take into account the FPGA family in which it operates. For example, for a Spartan-3 device, this sensor is composed of 32 stages. It allows propagating a complete period of the Spartan-3 reference frequency clock (50MHz). The figure 4(b) shows the Hard Macro integration of this sensor.

V. EXPERIMENTAL RESULTS

The Ring Oscillator and Path Delay Sensor described in the previous section are studied and compared. They were
both implemented into a Xilinx Spartan 3 Starter Kit Board with a XC3S1000-4FT256 (Fig.6(b)). This FPGA has a nominal operating point of $1.2V @ 25^\circ C$. In order to ensure reproducible results, the temperature is kept constant in a thermal chamber during all measurements (this instrument only allows heating, and then experiments are done at $40^\circ C$; this point will be discussed further) (Fig. 6(a)). We analyze first the resource overhead required by both structures. Then, the measurement errors are exposed and after that their impact is discussed. Finally, we provide both intra and inter variability characterizations of Spartan-3 FPGA devices.

![Experimental setup in the thermal chamber](image1) ![Spartan 3 board](image2)

**Fig. 6.** Experimental setup

### A. Overhead comparison

This section introduces an overhead comparison of the two sensors (Table. I). The area impact and the computing time for each sensor are presented.

<table>
<thead>
<tr>
<th></th>
<th>Hard Macro Size (# Slices)</th>
<th>Total Size (# Slices)</th>
<th>Sensor Latency (# Cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ring Oscillator</td>
<td>2</td>
<td>80</td>
<td>2046</td>
</tr>
<tr>
<td>Path Delay</td>
<td>16</td>
<td>16</td>
<td>2</td>
</tr>
</tbody>
</table>

The Hard Macro corresponds to the “probe” of the sensor. A smaller size for the probe allows characterizing a smaller area during the off-line monitoring phase. That’s why the Hard Macro Size is directly connected to the minimal size probing. Regarding on-line Monitoring, a small Hard Macro size is preferable to put it close to the critical modules (e.g., critical path). In this case, the Ring Oscillator Sensor is more interesting.

The total size of the sensor acts out the space needed for one full implementation of the sensor. This is to compare to the total space available in the FPGA. Indeed, the space used for sensor implementation is no longer available for the monitoring design. The Path Delay Sensor is better in this case.

The computing latency represents the number of clock periods between two successive measurements. Since the Ring Oscillator Sensor requires 2046 cycles, the Path Delay Sensor allows updating more rapidly the performance measurements. However, this potential advantage is to be considered with the processing capabilities of the management unit.

It is possible to take benefit from each sensor in different contexts. The Ring Oscillator Sensor will be preferably used for off-line monitoring characterization and for an accurate management of performance. The Path Delay Sensor will be preferred for a dynamic and direct critical path delay management.

In the next sections, the results of our experiments are presented. Our objective is to analyze the effectiveness of each sensor in its chosen field.

### B. Impact of sources of error

This part proposes a study of the impact of each error source. We will reach successively voltage error, temperature error and toggle count error.

Xilinx Spartan-3 Starter Kit does not provide the feature to manage directly the power supply voltage. Hence, the voltage regulator of our boards was substituted by an external voltage regulator. The figure 7 depicts the normalized output frequency of the Hard Macro depending on the power supply voltage. A voltage variation of $0.4V$ around the default value implies a $22.5\%$ of the sensor frequency. In our experiments, the supply voltage variation was only about $0.01V$ between boards. It involves a variation about $0.65MHz$ on the frequency (Tab. II). The supply voltage variation due to the fluctuation effects of the board regulator is less than $0.001V$. This has an impact of less than $65kHz$ on the frequency.

![Normalized Output frequency versus Power Supply Voltage](image3)

**Fig. 7.** Normalized Output frequency versus Power Supply Voltage

A representation of the normalized frequency depending on the temperature variation is illustrated in figure 8. The frequency of the ring oscillator Hard Macro decreases linearly as the temperature increases. During our experiments, the FPGA device is placed into a thermal chamber with a constant temperature (the variation is more or less $0.5^\circ C$). This change causes a fluctuation of about $0.1MHz$ of the oscillator frequency.
Regarding the ring oscillator, the fluctuation of the toggle count is also to take into account. For a best efficiency, this sensor was dimensioned for an error of a maximum of 3 in the toggle count. It results an error on the measurement about 73 kHz.

<table>
<thead>
<tr>
<th>Error</th>
<th>Frequency impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intra-board Voltage</td>
<td>0.001V</td>
</tr>
<tr>
<td>Inter-board Voltage</td>
<td>0.01V</td>
</tr>
<tr>
<td>Temperature</td>
<td>0.5°C</td>
</tr>
<tr>
<td>Toggle count</td>
<td>3</td>
</tr>
</tbody>
</table>

The total error due to external sources for intra-chip measurement is around 238 kHz. Nevertheless, all measurements are average 500 times thereby error due to variations is decreased. In fact, the total variation is around 6 times the standard deviation $\sigma$. The average standard deviation $\bar{\sigma}$ is then:

$$\bar{\sigma} = \frac{\sigma}{\sqrt{N}}$$

(3)

where N is the number of samples. Consequently, the total error attributable to external sources of variation is around 0.005% which corresponds to 10 kHz. This variation will be compared to the results obtained in next sections.

### C. Intra-Chip Characterization using Ring Oscillator Sensor

The Ring Oscillator Sensor was used to achieve full cartographies of the Spartan-3 S1000 chip. During the measurements, the external temperature of the chip is kept constant at a temperature of 40°C. This sensor is alternately placed at each CLB location, arranged into an array of 40 * 48 positions. Each measurement provided by the sensor is sent to an external computer, via an UART (Universal Asynchronous Receiver Transmitter), which performs the cartography of the chip (Fig. 9). The resulting frequency presented here corresponds to the mean oscillation frequency at the output of the Hard Macro. It takes around 5 hours for a complete cartography with a 500 times averaging for each point.

The figures 9 and 10 depict the results of two cartographies. The cartography of the Board 4 is relatively constant with a maximum frequency variation about 458 kHz while the second cartography presents a variation relatively large with a maximum frequency variation about 832 kHz. The cartography of the board 3 shows two features. First, there is a gradient of frequency all over the chip. Second, some slices on the middle of the chip are much less efficient than others. This type of results reinforce us in the necessity of a fine-grain cartography in order to achieve placement strategy for optimal performances on FPGAs.

Note that variations measured in a same board (> 100 kHz) are minor compared to the error calculate previously (≈ 10 kHz). Since we can assume that the supply voltage and the external temperature are fixed, we can infer that the variations measured on the frequency are effectively due to internal

![Fig. 8. Normalized Output frequency versus external temperature](image)

![Fig. 9. Oscillator frequency cartography at T = 40°C for Board 3](image)

![Fig. 10. Oscillator frequency cartography at T = 40°C for Board 4](image)
performance variations.

In future work, cartographies will be conducted with other temperature settings in order to confirm the trend on a same chip.

D. Inter-Chip Characterization

A similar characterization was conducted on several boards. Sample results are summarized in Table III. The figures 9 and 10 illustrate the difference between two boards. We can see that there are significant discrepancies between boards. Indeed, we observe here a difference of about 16.2% of the average frequency.

In this section, the Path Delay Sensor is used to perform a comparison between multiple boards. In Table IV, we have compared the five boards from the experience. This table introduces a time, which corresponds to the delay required by a signal edge to cross one LUT and the associate interconnect of the sensor. The Path Delay Sensor corroborates the results obtained with the Ring Oscillator Sensor (Fig. 11). However, with the Path Delay Sensor, we cannot distinguish the best FPGA between boards 3 and 4. This sensor is less accurate, but nevertheless allows fast estimations. For this reason, it will be used for on-line monitoring services.

### Table III

Comparison of Ring Oscillator Frequency Between Multiple Boards

<table>
<thead>
<tr>
<th>Board</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (MHz)</td>
<td>215.0</td>
<td>204.0</td>
<td>198.9</td>
<td>196.6</td>
<td>185.0</td>
</tr>
</tbody>
</table>

### Table IV

Comparison of Path Delay Speed Between Multiple Boards

<table>
<thead>
<tr>
<th>Board</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>T (ns)</td>
<td>2.86</td>
<td>3.07</td>
<td>3.2</td>
<td>3.2</td>
<td>3.33</td>
</tr>
</tbody>
</table>

VI. Conclusion and Future Works

Managing variability is one of the major issues in recent silicon technologies. As previously mentioned in the literature, FPGA devices are also subject to process, voltage, and temperature variations. In this paper, we have considered a twofold compensation flow for FPGAs, based on the use of digital sensors directly implemented in the reconfigurable resources. For this purpose, this article brought new results on the comparison of a Ring Oscillator structure and a Path Delay Sensor. In our experiments on Spartan-3 FPGAs, the ring oscillator was successfully used to perform intra-chip cartographies (1980 positions). Both sensors were evaluated for characterizing inter-chip performance variations.

We conclude that both structures are efficient for fast variability characterization in FPGA devices. The ring oscillator is the best structure for design-time measurements, whereas the Path Delay Sensor will be the preferred structure to allow rapid performances estimations at run-time with a minimal area overhead.

In future work, both sensors will be studied to perform run-time performance measurements. We will particularly focus on strategies to efficiently manage sensors (number, placement) and collect monitored information in order to adapt the system.

REFERENCES


