DIAMOND FOR ENHANCED GaN DEVICE PERFORMANCE

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ABSTRACT

AlGaN/GaN high electron mobility transistors (HEMT) semiconductor technology holds promise for revolutionary improvements in the cost, size, weight, and performance of a broad range of military and commercial microelectronics [1]. However, exploiting the true capabilities of GaN is a compromise between the desired RF performance and the realities of current thermal solutions. In this work we present modeling and integration details on performance of AlGaN/GaN high-electron-mobility transistors (HEMTs) fabricated on freestanding and mounted, heat-spreading diamond substrates. The excellent thermal properties of diamond substrates grown by chemical vapor deposition (CVD) provide a superior heat spreading material for electronic packages. The successful on-wafer integration of diamond with gallium nitride (GaN) has emerged as a critical solution for the expected thermal challenges of the next generation of high power RF and microwave devices.

INTRODUCTION

AlGaN/GaN HEMTs have demonstrated incredible power densities exceeding 40 W/mm [2]. However, this new generation of high power microwave devices faces significant thermal challenges due to ever increasing power densities. Due to its relatively low thermal conductivity, GaN is unable to effectively remove heat generated during device operation. Heat is typically conducted through a hierarchy of material structures, each of which adds thermal resistances. Efficient thermal management is essential for realizing intrinsic GaN capabilities.

With up to 150 mm in deposition diameter and 3-mm in thickness, CVD diamond is grown with room temperature thermal conductivities that range from 1000 W/mK to 2000 W/mK. CVD diamond has proven its superiority in replacing standard heat spreading materials such as aluminum nitride and beryllium oxide and it is already being used as heat spreader for high power density electrical devices, though more typically bonded through novel solder/metallization strategies.

The latest advancement in GaN-on-diamond substrates enables better thermal performance over standard GaN/SiC substrates. A significant portion of the enhanced performance stems from the reduction of the thermal resistance between the GaN device layers and the heat spreading CVD diamond. The decrease in the overall thermal resistance (R_{TH}) is achieved through material and structural improvements in the design of GaN-on-diamond substrate. By and large this is done by minimizing the thickness of all low thermal conductivity layers and all other thermal resistance components. The critical components of R_{TH}, are thickness sensitive thermal resistance components including thermal interface materials (TIM) and thermal boundary resistances (TBR).

Thermal boundary resistance, also known as thermal interface resistance is the resistance to heat flow at multilayer materials interface due to differences in the electronic and/or vibrational

properties of the materials, and by presence of impurities and dislocations at the interface [3].

We have extensively studied and have published on the impact of TBR on R_{TH} for GaN-on-diamond structures [4]. In this work we primarily focus on the impact of the thickness sensitive thermal resistance from the GaN buffer and the thermal interface material (TIM). As a thickness sensitive component of R_{TH} a typical thermal interface material provides matching interface which ideally possesses a high thermal conductivity, however in reality this is often compromised with a matched CTE and chemical compatibility.

In case of GaN-on-diamond, the primary role of our TIM is to maintain reliability and assure long term stability for the total structure. As such, the removal of GaN transition layers (buffer) and the optimization of the thermal interface material (TIM) properties are key contributing factors to any reduction in total thermal resistance (R_{TH}).

In this work we set to investigate that in presence of multiple thermal boundaries, would it be advantageous to leave some section of the buffer layer to allow for heat spreading? We use a 3D heat conduction solver to predict the thermal performance of the GaN-on-diamond structures. The model predicts that the thermal resistance decreases proportionally with the thickness of the proprietary TIM and somewhat surprisingly, peaks at an optimum GaN thickness for a finite TIM thickness.

DESCRIPTION OF PROBLEM

In GaN HEMTs built on Si, SiC, or diamond, the GaN buffer layer has lower thermal conductivity than the substrate. Intuitively one expects that thinning down the GaN buffer will result in lowering the

overall thermal resistance. However, for most epilayers grown on non-lattice matched substrates, this approach does not always lead to the lowest thermal resistance. This is primarily due to the presence of any additional thermal boundaries between the GaN buffer and the substrate.

An analysis of this phenomenon was pursued by numerically solving for the thermal resistance of typical GaN/D HEMT structures. The basic structure with the definition of thermal resistance used in this work is shown in Figure 1.
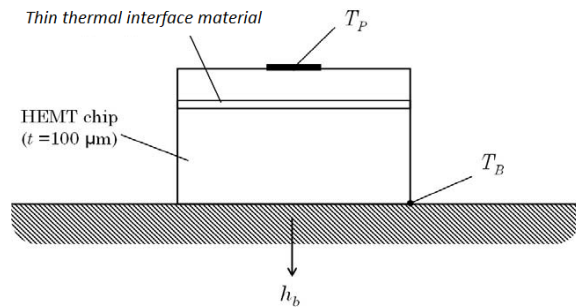

Figure 1 – Thermal resistance defined via the temperature drop across the chip only: It is the difference between the channel temperature TP and the average temperature at the bottom edge of the chip TB. Referred to as *chip only* thermal resistance $R_{TH} = (T_P-T_B)/P_{DISS}$.

The thin layer of thermal interface material represents a thermal boundary.

MODEL

The modeling was done using a 3D heat conduction solver which uses 2D Fourier expansion in x and y coordinates and matrix defined Green's function in the z-direction [5]. The program solves for the temperature distribution anywhere in a rectangular chip and accepts one planar heat source of arbitrary shape and infinitesimal thickness. The heat dissipation is uniform along the heat source. The convection cooled heat-sink is specified by the equivalent heat transfer coefficient h_b, = 35 W/cm²K.

STRUCTURE DESIGN

Figure 2 in combination with Table 1 detail the topical view of HEMT geometry and Table 2 describes the vertical details of the epi-layer on diamond structure. The epi-layer on diamond type A designation refers to the GaN/D with bulk-diamond thermal conductivity of 1000 W/mK. Type B refers to the GaN/D with diamond substrate with thermal conductivity of 1600 W/mK. The thickness of the diamond substrates is maintained at 100 μm, while the 20 μm of the substrate closest to the GaN buffer has been assigned thermal conductivity on the order of half that of the bulk [6].

The baseline design (a) uses HEMT geometry 2 x 100 μm with gate pitch 20 μm and shows the general behavior of the thermal resistance as a function of the buffer layer thickness and any interface material layer.
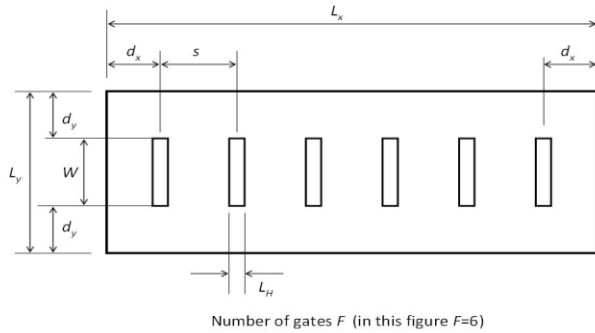

Figure 2 – Top view of a HEMT with dimension definitions

Table 1 – HEMT geometric parameters

Design	(a)	(b)	(c)	(d)	(e)
Epilayers On Diamond	A & B	B	B	B	B
F	2	2	80	2	2
L_x	400 μm	820 μm	820 μm	820 μm	820 μm
L_y	400 μm	458 μm	2,480 μm	458 μm	458μm
L_H	1 μm	1 μm	1 μm	2 μm	0.5 μm
W	100 μm	125 μm	125 μm	125 μm	125 μm
s	20 μm	26 μm	26 μm	26 μm	26 μm
d_y	150 μm	347 μm	347 μm	347 μm	347 μm
d_x	190 μm	216 μm	216 μm	216 μm	216 μm

Table 2 –Structures (Epi+TIM+Diamond) used in the model

Case A: GaN/D 1000

$h = 0.0$ W/m²K

0.0500 μm	318.0 W/mK	0.16 m²K/GW	Au contact
0.0200 μm	25.0 W/mK	0.80 m²K/GW	AlGaN barrier heater
***			
(varies) μm	130.0 W/mK	0.08 m²K/GW	GaN buffer
(varies) μm	3.0 W/mK	0.33 m²K/GW	Interface Mat.
20.0000 μm	500.0 W/mK	X m²K/GW	Diamond-surface
80.0000 μm	1000.0 W/mK	X m²K/GW	Diamond-bulk

$h = 350.0$ kW/m²K

Case B: GaN/D 1600

$h = 0.0$ W/m²K

0.0500 μm	318.0 W/mK	0.16 m²K/GW	Au contact
0.0200 μm	25.0 W/mK	0.80 m²K/GW	AlGaN barrier heater
***			
(varies) μm	130.0 W/mK	0.08 m²K/GW	GaN buffer
(varies) μm	3.0 W/mK	0.33 m²K/GW	Interface Mat.
20.0000 μm	800.0 W/mK	25.00 m²K/GW	Diamond-surface
80.0000 μm	1600.0 W/mK	50.00 m²K/GW	Diamond-bulk

$h = 350.0$ kW/m²K

RESULTS
The buffer and interface material thickness impact

Figure 3 and 4, show the general behavior of the thermal resistance with the buffer layer thickness for select interface layer thicknesses and diamond thermal conductivity. It is clear that there are two distinct regions in the parameter space: for low values of thermal boundary (thin interface material and/or high thermal conductivity) lowest thermal resistance is obtained when the GaN buffer thickness is brought to zero. In these regimes, the impact of the thermal boundary is so weak that no benefit can be obtained by allowing the heat to spread in the buffer [7]. When the thermal boundary - equivalent to certain interface layer thickness- increases beyond an *onset* value, the minimum thermal resistance occurs at a GaN buffer thickness greater than zero, and the thickness of GaN buffer for which the minimum thermal resistance occurs increases with the interface layer thickness.
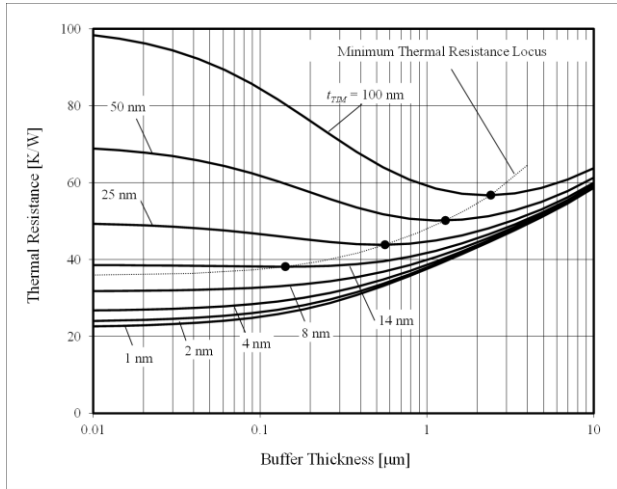
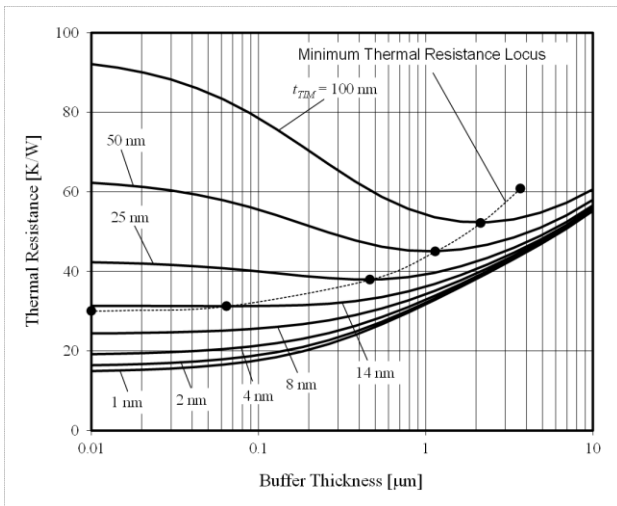Figure 3 – Structure A with diamond thermal conductivity of 1000 W/mK.

Figure 4 – Structure B with diamond thermal conductivity of 1600 W/mK.

In addition to demonstration of how thermal resistance varies with buffer layer thickness, Figures 3 and 4 show the locus for the minimum thermal resistance. The buffer layer thickness for which the minimum thermal resistance occurs is also plotted for these two cases in Figure 5. The dependence is slightly sub-linear and the plot covers the range of practical interface layer thicknesses.
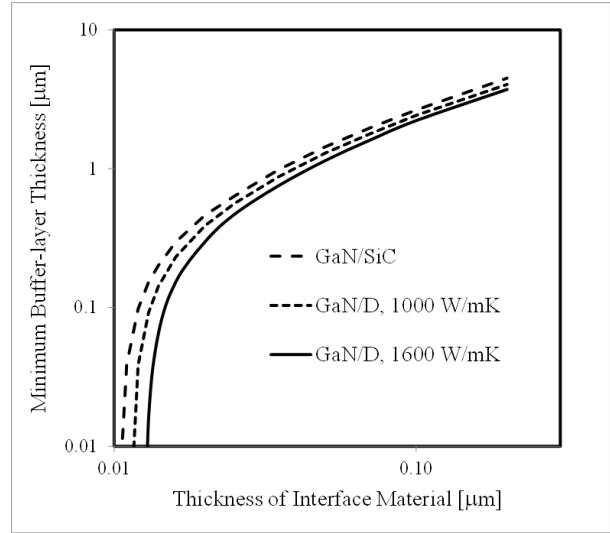

Figure 5 – Minimum buffer-layer thickness for various design structures

Figure 5 also bares the plot for GaN/SiC epi-layer with the same geometry. That is offered in the figure to illustrate that the optimal thickness of the GaN buffer reduces with the increased substrate thermal conductivity. It is deduced that the heat spreading in the substrate compensates for the heat spreading in the GaN buffer.

CONCLUSION

In general, for heat sources atop of a buffer layer on a thermally conductive substrate with a distinct thermal interface in between, it would be beneficial to optimize the thickness of that buffer to achieve lowest thermal resistance with respect to the heat source. The buffer thickness that results in lowest thermal resistance is greater than zero if the equivalent thermal boundary resistance is larger than a certain *onset* value.

Since the optimal buffer layer thickness depends on many parameters including the width of the heat source, one should model equal structures individually to determine the optimal thickness.

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ACRONYMS

GaN: Gallium Nitride

AlGaN: Aluminum Gallium Nitride

HEMT: High-electron mobility Transistor

CVD: Chemical Vapor Deposition

TIM: Thermal Interface Material

TBR: Thermal Boundary Resistance