A SOFTWARE-BASED PLL MODEL: ANALYSIS AND APPLICATIONS

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Abstract¾ This paper discusses the modeling of a fully software-base Phase Locked Loop (PLL) algorithm for power electronic and power system's applications. The theoretical analysis and design procedure are based on instantaneous vector calculation and orthogonality concepts. Although the uni-dimensional (single-phase) PLL structure provides a general model, a suitable tri-dimensional (three-phase) structure is also considered. Assuming that the frequency tracking is of great interest for utility connected devices, the PLL steady state and transient dynamic performances are analyzed under different disturbing voltages conditions. Simulation results validate the models and experimental results using a DSP-based system confirm the expectations for two different applications.

Keywords¾ digital PLL, frequency detection, orthogonality, phase-locked loop, synchronization.

Resumo¾ Este trabalho discute a modelagem de um algoritmo de sincronismo PLL (*Phase-Locked-Loop*) para aplicações em eletrônica de potência e em sistemas de energia elétrica. O embasamento teórico e o método de projeto são baseados em conceitos de álgebra vetorial e ortogonalidade entre funções temporais. Apesar do modelo genérico do PLL proposto ser baseado em sistemas unidimensionais (monofásicos), também será apresentado e discutido um modelo multidimensional (trifásico), o qual apresenta algumas características interessantes em condições específicas. Uma vez que a informação correta sobre a fase e a freqüência do sistema é de extrema importância para vários tipos de equipamentos e sistemas de controle conectados à rede elétrica, os erros de regime e a resposta dinâmica do PLL proposto serão analisados sob diferentes condições da tensão de alimentação. Resultados de simulação são apresentados para validar os modelos propostos, bem como resultados experimentais de um filtro ativo de potência, o qual utiliza as informações do PLL em sua malha de controle de corrente.

Palavras-chave¾ circuito de sincronismo, identificação da freqüência, ortogonalidade, PLL digital.

1 Introduction

More and more, industrial and power system's equipments must be synchronized with the frequency of the utility voltage and the most common methods are based on PLL systems.

The conventional PLL circuits were derived from the classical feedback control model, using a phase detector, a voltage controlled oscillator, a low-pass filter and a comparator. However, in the last years, several different algorithms and circuits have been proposed to provide the necessary information (Begovic, 1993), (Kaura, 1997), (Zhan, 2001), (Arruda, 2001), (Rossetto, 2003) and (Awad, 2003). Fast dynamic response, accuracy and robustness in presence of harmonics or transients have been the most important issues to deal with (Hsieh, 1996).

Regarding power system analysis and control, some interesting approaches have been derived from instantaneous power definitions (Silva, 2002), (Sasso, 2002), (Deckmann, 2003), (Lopes, 2003) and (Jesus, 2003). However, although these methods are quite simple to implement, since they use some analogies to the instantaneous power concepts (Akagi, 1999), they could lead to misinterpretation by those not familiarized with such relatively new and still controversial concepts (Depenbrock, 2003).

Considering a general uni-dimensional (single-phase) structure, as well as, an special tri-dimensional one (three-phase), the aim of this paper is to discuss a suitable methodology to design and analyze two software-based PLL models, which are based on instantaneous vector calculation rather than power concepts.

The proposed PLL structures derive from inner (scalar or dot) product and properties of orthogonal functions. Since the precision and dynamic behavior of the PLL is extremely dependent on its proportional-integral (PI) regulator, the design of such regulator is also discussed. Simulation and experimental results validate the models.

2 Inner product and orthogonality concepts

Multi-dimensional representation and vector calculus have been widely used in modern electrical networks analysis (Depenbrock, 2003), particularly due to their general and well-stated mathematical basis (Kreyzig, 1999). Accordingly, this paper deals with the definitions of inner product and orthogonality of instantaneous multi-variable vectors, in order to explain the digital PLL model.

2.1 Instantaneous Inner Product

The inner product $(\cdot)$ of two n-dimensional instantaneous vectors $\boldsymbol{v}$ and $\boldsymbol{u}$, consists of summing up the products of terms with similar index in both vectors (Kreyzig, 1999). Thus:

$$\boldsymbol{v}\cdot\boldsymbol{u} \equiv [v_1\ v_2 ... v_n]\cdot[u_1\ u_2 ... u_n] = \\ = v_1.u_1 + v_2.u_2 + \ldots v_n.u_n = \sum_{l=1}^{n} v_l.u_l \quad (1)$$

Considering tri-dimensional vectors (three-phase voltage or current signals), the resulting instantaneous inner product would be:

$$\boldsymbol{v}\cdot\boldsymbol{u} = [v_a\ \ v_b\ \ v_c]\cdot[u_a\ \ u_b\ \ u_c] = \\ = v_a.u_a + v_b.u_b + v_c.u_c = \sum_{l=a,b,c} v_l.u_l \quad (2)$$

2.2 Orthogonality Definition

Two non-zero vectors are called orthogonal ($\perp$) over the interval $t_1 \le t \le t_2$, with respect to a strictly positive weight function $w(t) > 0$, if and only if (Kreyzig, 1999):

$$\boldsymbol{v} \perp \boldsymbol{u} \iff \int_{t_1}^{t_2} w(t).[\boldsymbol{v}(t)\cdot\boldsymbol{u}(t)].dt = 0 . \quad (3)$$

If the weight function is assumed to be the inverse of the integration interval i.e. $w(t) = 1/(t_2-t_1)$, then (3) states that the *mean dot product* ($\overline{\ \cdot\ }$) of orthogonal signals is *always zero*, independently of their relative amplitudes:

$$\overline{\boldsymbol{v}\cdot\boldsymbol{u}_\perp} \equiv \frac{1}{t_2 - t_1}\int_{t_1}^{t_2}[\boldsymbol{v}(t)\cdot\boldsymbol{u}(t)].dt = 0 . \quad (4)$$

In the case of periodic signals, such as trigonometric functions, the orthogonality condition applies to the function period *T*:

$$\overline{\boldsymbol{v}\cdot\boldsymbol{u}_\perp} \equiv \frac{1}{T}\int_{t_2-T}^{t_2}[\boldsymbol{v}(t)\cdot\boldsymbol{u}(t)].dt = 0 \quad (5)$$

and, considering a digital implementation, expression (5) could be represented by the discrete summation:

$$\overline{\boldsymbol{v}\cdot\boldsymbol{u}_\perp}(k) = \frac{1}{m\Delta}\sum_{i=1}^{m}\left[\sum_{l=1}^{n} v_l(k - i\Delta).u_l(k - i.\Delta)\right] \\ = 0 \quad (6)$$

where "Δ" is the sampling interval, "*m*" is the number of samples per period ($T=m\Delta$) and "*k*" is the sampling counter.

The previous expression can also be interpreted as a moving average filter (Oppenheim, 1999), which is simple to implement and represents an efficient approach to calculate the mean value of time domain vectors (variables).

3 Digital PLL using Inner Product Model

The main goal is to introduce a PLL design methodology valid for single and three-phase (uni or multi-dimensional structure) applications, without using the instantaneous power concepts.

3.1 General Single-Phase Model (1ϕ-PLL)

The proposed 1ϕ-PLL is shown in Fig. 1 and the central idea is to synthesize a unitary sinusoidal function ($u_\perp$), which is orthogonal to the input voltage (v) under steady conditions. Thus, the dot product result (dp) of this digitally synthesized function with the input voltage must converge to zero mean value. The instantaneous argument θ, used to synthesize the sinusoidal function $u_\perp$, is obtained by integrating the PI regulator output ω. While the PLL algorithm seeks to synthesize the unitary sinusoid to satisfy the orthogonality condition with the input voltage v, the PI controller converts the product error (dp_{error}) into a varying correction term (Δω) that leads to the desired input signal frequency ω, rendering the argument function θ by simple integration.

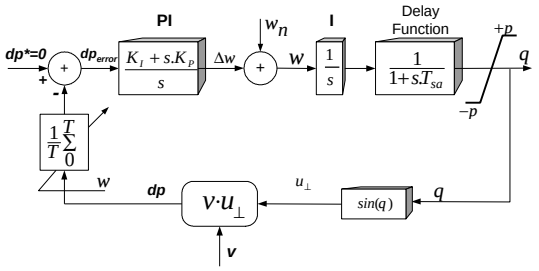

Figure 1 – Generalized 1ϕ -PLL Model.

A feed-forward reference ($\omega_n = 2\pi f_n$) is included to improve the initial dynamic performance, where f_n is the utility nominal frequency. Since the interest is to develop a digital PLL, a sampling delay function may be added to the PLL model in order to represent the sampling process (sampling time T_{sa}). The PI regulator reaches a constant output ω if the mean input error is zero ($\overline{dp}_{error} = 0$). At this condition θ=ω.t, and the PLL tracks the input voltage frequency ω, with a phase-angle delay of (-π/2), which guarantees the orthogonality condition. Hence, the PLL is able to provide the utility's varying frequency (ω) and the synchronizing angle ($\phi = \theta + \pi/2$).

3.1.1 Adaptive Moving Average Filter

In order to satisfy the orthogonality condition (5-6), the moving average filter should be self-adjustable to the fundamental period and can be represented in the *Laplace*'s domain simply as:

$$H_{filter}(s) = \frac{1 - e^{-sT}}{sT}, \quad (7)$$

where T is the input fundamental period, which is dependent of the instantaneous evaluated angular frequency (ω).

After some calculation and using Taylor series approximations, the transfer function of the average filter can be simplified, rendering a constant

and unitary gain, as discussed in (Deckmann, 20003).

In order to ensure that the number of samples in the fundamental window (period) is always constant (6), this strategy needs to alter the window size or the sampling frequency according to the frequency variations (Δω). Considering DSP (Digital Signal Processor) implementations, the second choice seems to be more suitable.

3.2 Design Methodology of the PI Regulator

Assuming that the usual sampling frequencies are significantly higher than the systems bandwidth, the non-linear feedback functions of Fig. 1 can be simplified to the linear structure of Fig. 2 (Silva, 2002). Thus, the close-loop transfer function, including the controller and the plant become:

$$H_{CL}(s) = \frac{k_p s + k_i}{s^3 T_S + s^2 + k_P s + k_I}. \quad (8)$$

The resulting third-order system should ideally be controlled with fast dynamic performance and small steady-state errors. It should also be robust under transients and noisy input signals. However, in practical applications this tuning is relatively difficult to prescribe and the designer may choose to focus on the essential characteristics of each project.

Different tuning methods can be applied (Aström, 1997), (Deckmann, 2003) and with the assumption of small sampling delays, the third order system (8) could be reduced to the *canonical form of second order system* (9), without affecting the control capabilities (Nise, 2000). Such simplification is possible since the pole relative to the sampling delay, placed in the left side of the s-plane, is far from the origin and the other two dominant poles.

$$H_{CL}(s) = \frac{k_p s + k_i}{s^2 + k_P s + k_I}. \quad (9)$$

Thus, $k_P = 2xw_n$ and $k_I = w_n^2$, where w_n is the *closed-loop* crossover frequency and ξ is the damping factor (usually in the range 0.5 to 1).

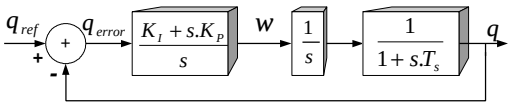

Figure 2 - Simplified PLL model.

3.3 Particular Three-Phase Model (3ϕ-PLL)

Frequency-tracking requirements are also quite common in three-phase applications, but since the necessary information can be obtained from the mains frequency (common to all phases) and one of the synchronization angles (e.g. phase "a"), the previous 1ϕ-PLL is able to provide all necessary information.

Nevertheless, since previous papers (Silva, 2002), (Sasso, 2002), (Deckmann, 2003) and (Lopes, 2003) have been exploring the implementation of 3ϕ-PLL structures, this paper also deals with a 3ϕ model using the multi-dimensional approach described in Section 2, as depicted in Fig. 3.

The three-phase model leads to the same expressions of the single-phase, and the close-loop transfer function yields identical (the simplified three-phase structure is equal to that presented in Fig. 2). Thus, the described procedure for tuning the PI regulator is valid for both models, as well as the stability and dynamic analysis.

However in this case, the very convenient characteristic of automatically rendering constant inner product can be achieved in balanced sinusoidal voltage conditions, even without using the moving average filter for "*dp*". The average filter may also be neglected if the voltage's distortion or unbalances were not very high, since the filtering capability of the PI regulator itself ensures a good performance of the PLL.

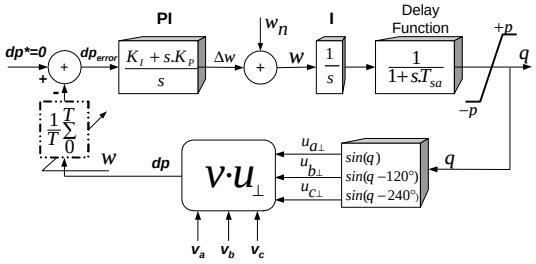

Figure 3 -Three-phase digital PLL using instantaneous inner product of orthogonal functions.

3.4 Measured Voltage Conditions

The central point on using the 3ϕ-PLL is the understanding of how the set of measured voltages can affect the PLL performance or the PI design. The following analysis considers the variations of the mean inner product, regarding to different voltage conditions and thus, beneficial or harmful effects can be associated to such conditions:

3.4.1 Sinusoidal and Balanced Voltages

If the input signals constitute a balanced, three-phase sinusoidal voltages set ($\boldsymbol{v} = [v_a \; v_b \; v_c]$), then the instantaneous dot product of such voltages and the synthetic PLL signals ($\boldsymbol{u}_\perp = [u_{a\perp} \; u_{b\perp} \; u_{c\perp}]$) converges very fast to zero mean, just with a slight PI regulator action (without the "*dp*" average filter). In such situation, the PI filtering capacity is not critical and its dynamic response can be very fast (less than half cycle).

3.4.2 Influence of Voltage Distortions

To analyze the effects of harmonics in the input voltage set, it is necessary to substitute vector $\boldsymbol{v}$ by the corresponding harmonic series ($\boldsymbol{v} = [\Sigma v_{ah} \;\; \Sigma v_{bh} \;\; \Sigma v_{ch}]$). Now, the resulting instantaneous dot product will be time variant due to the product of different frequency components:

$$\begin{aligned} \boldsymbol{v} \cdot \boldsymbol{u}_{\perp} &= [\Sigma v_{ah} \;\; \Sigma v_{bh} \;\; \Sigma v_{ch}] \cdot [u_{a\perp} \;\; u_{b\perp} \;\; u_{c\perp}] \\ &= \Sigma v_{ah}.u_{a\perp} + \Sigma v_{bh}.u_{b\perp} + \Sigma v_{ch}.u_{c\perp} \end{aligned} . \quad (10)$$

As long as the fundamental (h=1) input voltages are orthogonal to the PLL sinusoidal output signals, the mean value of the dot product will be zero:

$$v_{a1}.u_{a\perp} + v_{b1}.u_{b\perp} + v_{c1}.u_{c\perp} = \overline{\boldsymbol{v} \cdot \boldsymbol{u}_{\perp}} = 0 . \quad (11)$$

In this case the PLL convergence is not as smooth as in the previous case and the PI regulator action should filter out the fast oscillations of the instantaneous product with zero mean value, while keeping a good dynamic performance and precise tracking capability. However, it requires a fine adjustment of the regulator parameters.

3.4.3 Influence of Voltage Unbalances

To analyze the effects of asymmetries in the voltage set, it is necessary to substitute, the input vector $\boldsymbol{v}$ by the corresponding sequence components ($\boldsymbol{v}=[\Sigma v_{as} \;\; \Sigma v_{bs} \;\; \Sigma v_{cs}]$), where e.g. $v_a = \Sigma v_{as} = v_a^{+} + v_a^{-} + v_a^{0}$ is the sum of the sequence components of phase "a". In this case the instantaneous dot product will also be oscillatory with zero mean, due to the product of different sequence components.

$$\begin{aligned} \boldsymbol{v} \cdot \boldsymbol{u}_{\perp} &= [\Sigma v_{as} \;\; \Sigma v_{bs} \;\; \Sigma v_{cs}] \cdot [u_{a\perp} \;\; u_{b\perp} \;\; u_{c\perp}] \\ &= \Sigma v_{as}.u_{a\perp} + \Sigma v_{bs}.u_{b\perp} + \Sigma v_{cs}.u_{c\perp} \end{aligned} . \quad (12)$$

Regarding the PI regulator design, the previous conclusions could also be drawn, for small unbalances. However, if large unbalances are present, the use of the moving average filter for "*dp*" is mandatory to provide good dynamic behaviour and precise tracking capability at the same time. In such case, the minimum response time is typically one cycle.

3.4.4 Line Input Voltages

Since the orthogonal functions ($\boldsymbol{u}_{\perp}$), synthesized by the PLL, are mathematically imposed to be sinusoidal and balanced, they always sum up to zero ($u_{a\perp} + u_{b\perp} + u_{c\perp} = 0$). Thus, it is possible to rearrange (2) in order to obtain the same dot product using only two-measured line voltages (17), while reducing the number of input voltage sensors for three-phase practical applications:

$$\overline{\boldsymbol{v} \cdot \boldsymbol{u}_{\perp}} = v_{ab} \cdot u_{a\perp} + v_{cb} \cdot u_{c\perp} = 0 . \quad (13)$$

In addition to the comments about the voltage conditions, it is very important to point out that the input signals should be normalized to ensure that the PLL works in a large input range. Thus, it is recommended to use per unit values.

4. Simulation Results

Figures 4 and 5 show the performance of the 1ϕ-PLL, designed for a crossover frequency (w_n=20rad/s) and ξ =0.707. In such simulation the measured input voltage presents 15% of 7th harmonic. Figure 4 illustrates the distorted input voltage (v), the digital sinusoidal function ($u_{\perp}$), which results orthogonal to the fundamental of (v) and the PLL output phase-angle (θ) in the range [0,2π]. Since the fundamental frequency was set to 60Hz, Fig. 5 shows the angular frequency convergence (ω≈377rad/s) and shows the performance of the moving average filter, which is responsible for calculating the mean value of the instantaneous inner product (dp_med ≅ 0).

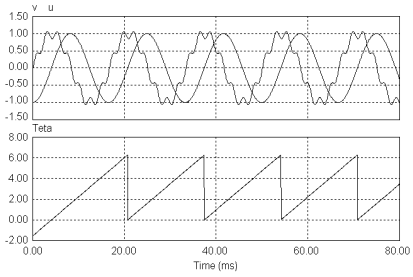

Figure 4- Single-phase PLL: Distorted input voltage, PLL quadrature sinusoid and its cyclic argument angle θ [0,2π].

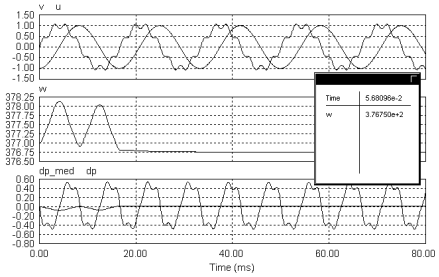

Figure 5- Upper: input and PLL voltages. Middle: PLL frequency. Lower: input/output signals of the average filter.

Figure 6 shows three-phase input voltages ($v_a \;\; v_b \;\; v_c$), respectively distorted by 10% of 5th, 7th, and 3rd harmonics, and their fundamental amplitudes are unbalanced by 20% amplitude reduction in phase "a" and 10% increase in phase "b". Note that the PLL preserves its good performance, as long as the internal sinusoidal functions "$u_{\perp}$" are orthogonal to the input voltages "v", as detailed for phase "a" in the middle curves.

Fig. 7 illustrates the effect of imposing a sudden frequency change. Even combined with an

amplitude discontinuity, the PLL tracks very smoothly the new frequency with a settling time of less then one cycle.

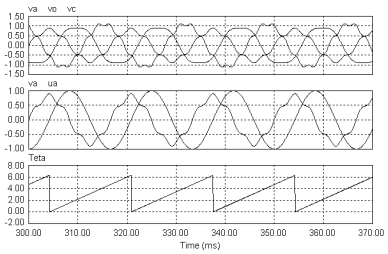

Figure 6 - Three-phase PLL: a study case with distorted and unbalanced input voltages.

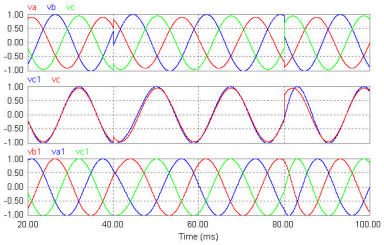

Figure 7 – Three-phase unbalanced voltages during a (-2Hz) frequency step and fundamental unitary 3ϕ-PLL outputs.

5. Experimental Results

In order to validate the algorithms in practical applications, the proposed 3ϕ-PLL model was implemented in a selective harmonic active power filter, as shown in the diagram of Fig. 8 and described in details in (Marafão, 2004).

The experimental setup was based on a 5kVA converter and a 16 bits fixed point DSP controller (ADMC401). The results have shown that the classical control tuning procedure (9) provides quite robust performance of the PLL, even with distorted and unbalanced input voltages.

Firstly, the PLL performance is evaluated without the closed-loop controller. Figure 9 shows the input voltage (minor trace) and the PLL inter-

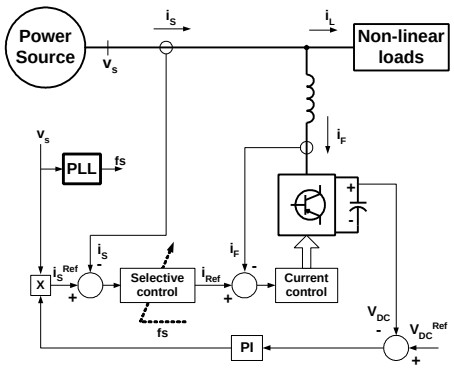

Figure 8 – Diagram of the active power filter using selective harmonic compensation.

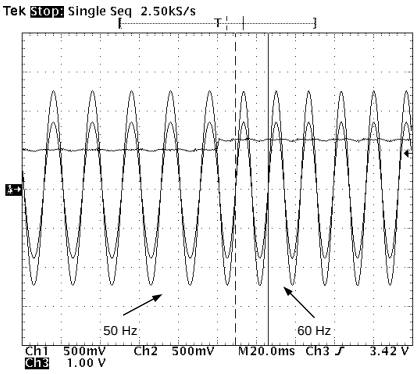

Figure 9 – 3ϕ-PLL action during a frequency step from 50 to 60Hz.

nal sinusoid (higher trace), shifted by +π/2 (ϕ) in order to be in phase with the input voltage, during a frequency step (DC trace) from 50Hz to 60Hz. Note that the voltage period changes very fast from 20ms to 16.66ms. This test was performed using a programmable AC power source and the PI regulator was adjusted to converge within a cycle.

For the active power filter, the PLL provides the necessary sampling frequency adjustment for correct action of the selective harmonic compensation method. Figure 10 shows the effective current compensation and, the almost sinusoidal source current confirms that the filter tracks precisely the mains frequency.

The proposed PLL models have been investigated under several other different applications, such as high performance controlled rectifiers or the line-interactive inverter controller described in (Machado, 2004) and further discussions and experimental results are going to be presented in next papers.

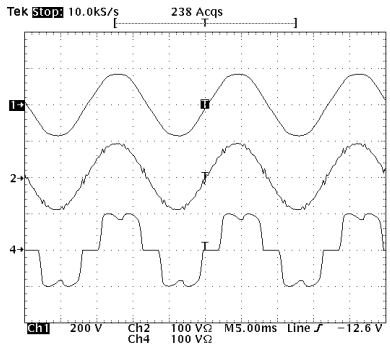

Figure 10 – Active Filter using 3ϕ-PLL in the selective control: line voltage (1), line current (2) and load current (4).

6. Conclusion

This paper has discussed two simple software-based PLL models. Although recent PLL structures have been based on instantaneous power definitions, the proposed models are basically derived from vector algebra and orthogonal signal proper-

ties. The design methodology is quite simple and it is valid for the general single-phase model, as well as a suitable three-phase structure.

Since the PLL performance is directly related to the measured voltages conditions, the influence of distortions and asymmetries have also been discussed, particularly to the three-phase model.

To confirm the theoretical expectations, simulation and experimental results have been considered and the proposed models have shown to be very effective for the applied active power filter application.

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