Reconfigurable Computing: Is it Ready for Industry?

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Some History

• Reconfigurable Computing research since late eighties
• Significant penetration in the research community – (e.g. whole tracks in some conferences)
• But is it ready for industry to make money out of it?
What is Reconfigurable Computing?
Temporal-Spatial Processing
RC Status today

• Thriving research activities in universities.
• Industry is interested…. But:
  – Still looking for RC’s value proposition
  – Global economy delaying new product launches
  – No sufficient R&D resources for Tech. Transfer
• Wrong architectures for the right applications
• Intended users
• Software tools!!!
What works?

- Part of a solution, or the whole solution (i.e. Core IP or Chip?)
- What is RC intended to replace? ASIC or DSP?
- No single size fits all
  - Different application domains require different capabilities
  - I/O and memory
- Flexibility costs area, performance, power
  - Some functions are still more efficiently implemented in ASIC blocks
- Target a programming paradigm familiar to intended users
The Ubiquitous Mobile

Many Different Wireless Networks

Intelligent, Reconfigurable Clients

Seamless access to all networks, apps, & services anytime anywhere

Public Networks/Internet Converged services

Communications and Interconnect Lab
Standards are Many
Which 3G do you mean?
Standards are not really fixed

Figure 3: 3GPP approved change requests

Source: Deutsche Bank Securities Inc. estimates and company information
Not Only standards but applications also

Source: U. Ramacher, Infineon
When ReConfigurability Makes Sense
(100% WLAN Wireless, 2% Active)

(For Baseband PHY and lower MAC)

Source: Intel Corp.
Architecture of MS1 Core
MS1-16 Core
Designed for use in 3G Base Stations

Specialized Blocks
- IQ Buffer
- Sequence Generator

Specialized Block
- Interleaver

I/O Interface

Data Memory

Context Memory

Controller

2 Rows 8 Columns rDSP fabric
Software Structure
Applications
3G Device
Implementation with MS1

- Multiple functions require a single MS1 Core and uController
- rDSP provides flexibility for modifications
- Smaller silicon area
- Shorter time-to-market
Applications
Example: Forward Link WCDMA AMR Channel
Fully Implemented for the MS1-16 Development Board

IQ Samples → RAKE Rcvr → 2nd Deinterleaver → 1st Deinterleaver → DTX bits Removal

Demux → 1/3 Rate Viterbi Dec → CRC Check → Block Code Removal → Decoded Block Segmentation

1/3 Rate Viterbi Dec → 1/3 Rate Viterbi Dec → 1/3 Rate Viterbi Dec

Enhanced Full Rate Decoder → D/A → VOICE
Applications
Example: RAKE Receiver
Fully Implemented for the MS1-16 Core

8-bit IQ samples 8x oversampling

RAKE Finger N
RAKE Finger 1
RAKE Finger 2
RAKE Finger N

Channel Estimation
Path Selection

Despreeder
Symbol Timing Estimation
Symbol/Code Tracking

Early Late Punct

CPICH

I² + Q²

Phase Estimation
Phase Offset Estimation

DDS

AFC

RSSI_{CPICH}

RSSI_{DPCH}

τ

MRC
Applications

WCDMA Links on the MS1
AMR 12.2 Kbits/s Voice Channel

Tasks are executed in a time-multiplexed fashion
Applications

WCDMA Links on the MS1
2-Branch Diversity 384 Kbits/s Data Channel

downlink
Rake Receiver
→
Rake Receiver
→
Turbo Decoder
R = 1/3 K = 4
→
MPEG-4 Decoder

uplink
Spreading
→
Turbo Encoder
→
MPEG-4 Encoder

% of 10ms radio frame
35% headroom

% of 10ms radio frame
35% headroom
Introducing MRC6011

- Six RC cores at 250 MHz
  - 0.13μ, 1.2v core
  - 48 Giga Complex Correlations (4bit) per sec
  - 24 (16bit) GMACs

- Each Core Features
  - Array of 16 RC elements
  - Optimized RISC processor
  - Dedicated Frame & Input Buffers
  - Instruction cache & Data cache

- Each RC Features
  - 16-bit arithmetic, logical and conditional units
  - 16 bit Pipelined MAC unit
  - Complex correlation unit

- Memory Subsystem Features
  - Host-visible data memory & Control memory
  - Inter–module shared Memory

- High-Throughput 100 MHz Bus Interfaces
  - 2 Slave-IO Bus Interface
  - 2 Multiplexed Data Input

- Power consumption and packaging
  - Under 3W (typical)
  - 31mm x 31mm TBGA

RCF = Reconfigurable Compute Fabric

www.motorola.com/sndf
Generic System Architecture

DL TX IF

UL RX IF

DL TX IF

UL RX IF

DL TX IF needs a 60x Bus IF Master

SDRAM

PQ II

SDRAM

SDRAM

Trsp Network IF

Ctrl Network IF

Source: Motorola SPS
Scenario 1: 128 AMR Users UL+DL, RACH

- 128 AMR Users for UL and DL, includes 1 Sector RACH Processing.
- This scenario implies **Worst Case load** on the devices

Source: Motorola SPS
We now calculate a Scenario, where 30% Data Traffic is assumed to be the average load of the system. This translates roughly into 89 x AMR Channels and 3 x 384 kbit/s data channel.

2 HSDPA carriers with 18 Users of H-Set1 could be processed at zero additional cost, and still with a DSP System load of only 75%!
## Channel Capacities for Different Services

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Services</th>
<th>Data Rate</th>
<th>Number of Users</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3G AMR</td>
<td>12.2 Kbit/s</td>
<td>128</td>
</tr>
<tr>
<td>2</td>
<td>3G Data 384</td>
<td>384 Kbit/s</td>
<td>28</td>
</tr>
<tr>
<td>3</td>
<td>3G HSDPA H-Set1</td>
<td>534 Kbit/s</td>
<td>144*</td>
</tr>
<tr>
<td>4</td>
<td>EDGE AMR</td>
<td>12.2 Kbit/s</td>
<td>144</td>
</tr>
</tbody>
</table>

Assumes maximum no of Channels processed on the flexible proposed solution.
* Example, does not refer to available capacity/code space

Source: Motorola SPS
What about Others?

A Proposed Communications Architecture

- Configurable array of processing elements (PEs)
- Each PE has nearest neighbor connectivity via mesh
- PEs can be heterogeneous
- 32KB memory and 4 16b MACs per PE
- Embedded controller to configure the PEs and route data

Source: Intel Corp.
Other RC industry adoptions

• QuickSilver Technology recently announced that it has licensed its technology to Olympus for camera apps.
• Sony announced the latest Clie TG50 PDA incorporating a reconfigurable processor.
• Phillips acquired Systemonics for their Wi-Fi solution on RC
• Infineon acquired MorphICs
What was the press saying in 1998

Adaptive Chips

Each and every software application on your system has specific needs. Your word processor, for instance, requires only minimal multimedia and computational resources. Web browsers and games, on the other hand, may need a maximum of both.

To help computers allocate resources more efficiently, professors Fadi J. Kurdahi and Nader Bagherzadeh at the University of California, Irvine, are looking into ways to let computer chips change dynamically. “Our approach is to use computer power to make chips extremely flexible, so they can dynamically adapt their structure to each application they run and execute that application as efficiently and as quickly as possible,” says Kurdahi. According to Bagherzadeh, the technology should take five years to come to fruition.

Recent advancements in manufacturing processes that have increased the number of transistors per chip are key to the technology. The Pentium II, for instance, has 7.5 million transistors; Intel’s next-generation chip Merced will contain nearly 30 million. Kurdahi and Bagherzadeh look to the day when a chip can have 1 billion transistors.

President Clinton recently announced steps to fund this and other university projects to develop so-called billion-transistor chips. “These chips will be no larger than my fingernail, but their computing power will be 25,000 times greater than this entire mainframe computer,” he said. Through the Defense Department, the government is supporting this effort to the tune of $14 million.
And five years later…..

Will parallel chips pay off?
Mar 13th 2003
From The Economist print edition

The key to success in parallel processing on a chip will be the ability to map computational algorithms efficiently on to an array of resources, and hide the complexity from both programmer and user. *The company that can do that has a shot at being the next Intel.*

An architecture must be chosen to optimize power, cost and flexibility
Perhaps theses are Configurable Logic Processors

Communications and Interconnect Lab

Source: Intel Corp.
Conclusion

• Reconfigurable Computing provides viable solutions to real problems
• Industry adoption of RC in some segments
• Tools, tools, tools!