Developing a novel sinusoidal pulse width modulation (SPWM) technique to eliminate side band harmonics

Ilhami Colak a,⁎, Ersan Kabalci b

aDepartment of Electrical & Electronics Engineering, Faculty of Technology, Gazi University, 06500 Ankara, Turkey
bDepartment of Electrical & Electronics Engineering, Faculty of Engineering and Architecture, Nevsehir University, 50300 Nevsehir, Turkey

A R T I C L E   I N F O

Article history:
Received 19 January 2012
Received in revised form 10 August 2012
Accepted 19 August 2012

Keywords:
Sinusoidal pulse width modulation
Digital signal processor
Simulink
Voltage source inverter
Harmonic elimination

A B S T R A C T

In this study, an enhanced SPWM modulation scheme is developed in order to minimize total harmonic ratio (THD) by eliminating the side band harmonics that are not paid attention in regular modulation schemes. Unlike the conventional SPWM, the developed modulation scheme considers the elimination of harmonics that are located at the carrier frequency and at the side bands of carrier frequencies. Therefore, the harmonic elimination feature of SPWM that eliminates the base harmonic orders but not considers the side band harmonics in frequency domain is improved with the developed analytical definition. The side band harmonic elimination feature of the proposed SPWM scheme eliminates higher order harmonics. The elimination of high-ordered attenuated harmonics decreases the harmonic contents seen in the THD spectrum. The simulation of inverter is carried out with Matlab/Simulink and experimental studies are performed utilizing TMS320F2812 DSP. The proposed SPWM schemes is tested according to various control strategies such as switching frequency (fsw) and modulation index (mi) terms by using a full bridge inverter. The analytical model improved to calculate and generate switching intervals is simultaneously operated in DSP instead of managing a look-up table. The experimental studies of the inverter verify that the developed SPWM modulation scheme mitigates the side band harmonics successfully. The higher order harmonics are eliminated and the THD ratios are decreased owing to proposed SPWM scheme.

© 2012 Elsevier Ltd. All rights reserved.

1. Introduction

The static power converter based inverters are utilized in adjustable speed drives (ASDs), static VAR compensators, active filters, uninterruptible power sources (UPSs), and flexible AC transmission systems (FACTS) which are only a few applications for industrial uses. The AC voltage generated at the output of inverter may be variable or constant depending to the requirements of the applications. The voltage source inverters (VSIs), where the independently controlled AC output is a voltage waveform, behave as voltage sources required by many industrial applications. The current source inverters (CSIs) are still widely used in medium-voltage industrial applications, where high-quality current waveforms are required. The VSI generates an AC output voltage waveform composed of discrete values (high dv/dt); therefore, the load should be inductive at the harmonic frequencies in order to produce a smooth current waveform.

A capacitive load in the VSIs will generate large current spikes, which can be prevented by an inductive filter between the AC side of VSI and the load. An inductive load in CSIs will generate large voltage spikes as on the contrary to VSI. If this is the case, a capacitive filter between the CSI AC side and the load should be used [1–4]. The efficiency parameters of an inverter such as switching losses and harmonic reduction are principally depended on the modulation strategies used to control the inverter [5–7]. As depicted in Fig. 1, inverter control techniques are based on fundamental frequency and high switching frequency.

The regular PWM modulation methods can be classified as an open loop and a closed loop owing to its control strategy. Open loop PWM techniques are the SPMW, the space vector PWM, the Sigma–Delta modulation, while closed loop current control methods are the Hysteresis, the Linear, and the Optimized current control techniques. The modulation methods developed to control the multilevel inverters are based on multi-carrier orders with PWM. Due to pre-defined calculations are required, the Selective Harmonic Elimination SHE–PWM is not an appropriate solution for closed loop implementation and dynamic operation in multilevel inverters. Among various control schemes, the sinusoidal PWM (SPWM) is the most commonly used control scheme for the control of multilevel inverters. In classical SPWM, a sinusoidal reference waveform is compared with a triangular carrier waveform to generate switching sequences for power semiconductor in inverter modules. The fundamental frequency SPWM control method was proposed to minimize the switching losses. The multi-carrier SPWM control methods are also implemented to increase the
performance of multilevel inverters and are classified according to vertical or horizontal arrangements of carrier signal [8–12]. There are several studies performed to evaluate control algorithms with DSPs in recent years owing to its robust processing capabilities of 32-bit, and fixed or floating-point calculations [13–15].

In this paper, classical SPWM control algorithm is developed by considering the side band harmonics and modulation bandwidth in Simulink during simulation. The experimental verification of the modeled system is analyzed by controlling the IGBT modules with a TMS320F2812 DSP. The current and voltage waveforms generated by both simulation and experimental studies are compared under various conditions such as variable \( m_i \) and \( f_{sw} \) values. The THD ratios obtained and power factor of the implemented system are compared according to the similar studies in the literature. The performed studies were focused on DSP implementation instead of comparative analyzing in terms of harmonic contents or other factors in the generated line voltages and currents. The performance of the simulation is checked with DSP implementation. The THD ratios of both voltage and current of the implemented VSI provided better results according to previous studies [15–19].

2. System modeling

Modeling studies are performed by defining the inverter and control algorithm requirements. Full bridge inverter topology is selected due to its widespread application area. The circuit topology, the SPWM control scheme, and implementing the Simulink model of the inverter are analyzed in detail.

2.1. Circuit topology

While the single-phase VSIs cover low-range power applications, three-phase VSIs cover medium to high-power applications. The main purpose of these topologies is to provide a three-phase output voltage, where the amplitude, the phase, and the frequency of voltage should always be controllable. Three-phase bridge inverters are widely used in motor drives and general-purpose AC supplies. A typical three-phase VSI topology is shown in Fig. 2. As in single-phase VSIs, the switches of any leg in the inverter (\( S_1 \) and \( S_4 \), \( S_3 \) and \( S_6 \), or \( S_5 \) and \( S_2 \)) cannot be switched on simultaneously to prevent a short circuit across the DC link voltage supply.

Similarly, in order to avoid undefined switching states and undefined AC output line voltages in the VSI, the switches of any leg in the inverter cannot be switched off simultaneously. The phase outputs are mutually phase shifted by 120° angles as seen in the Fourier expansions in Eqs. (1)–(3) where, \( V_d \) is the DC supply voltage. The line voltages can be defined as expressed for \( V_{ab} \) in Eq. (4).

\[
V_{ab} = \frac{2V_d}{\pi} \left( \cos \omega t - \frac{1}{3} \cos 3\omega t + \frac{1}{5} \cos 5\omega t - \cdots \right)
\]  

\[
V_{bo} = \frac{2V_d}{\pi} \left[ \cos \left( \omega t - \frac{2\pi}{3} \right) - \frac{1}{3} \cos \left( \omega t - \frac{4\pi}{3} \right) \right]
\]  

\[
+ \frac{1}{5} \cos \left( \omega t - \frac{2\pi}{5} \right) - \cdots
\]  

Fig. 1. Classification of multilevel inverter control schemes.
The modulating reference sinusoidal signal is compared with a constant DC voltage level. The SPWM modulation scheme is used to control the switching elements in an inverter to generate a sinusoidal output voltage. The switching states are obtained with interpolation in discrete time domain which is equivalent to filtering process in frequency domain. The harmonic elimination feature of the developed modulation scheme is increased by adding digital filtering operations with interpolation method. The Bessel functions are defined in series expansion form in electromagnetic, telecommunication, and power systems. First order Bessel function is defined by Gradsteyn and Ryzhik as seen in the following equation [25–28]

\[ J_0(x) = \sum_{k=0}^{\infty} (-1)^k \frac{x^{2k}}{2^k k!(k+1)!} \]  

(5)

where \( \Gamma \) is the gamma function and \( x \) is the degree of the Bessel function. The Bessel function is rearranged for \( x = 0 \) and \( x = 1 \) orders as given in the following equations:

\[ J_0(x) = \sum_{k=0}^{\infty} (-1)^k \frac{x^{2k}}{2^k k!(k+1)!} \]  

(6)

\[ J_1(x) = \sum_{k=0}^{\infty} (-1)^k \frac{x^{2k+1}}{2^k (2k+1) k!(k+1)!} \]  

(7)

The equivalent integrative definition of 1st kind and \( x \) ordered Bessel function is obtained as seen in the following equation [28–30]:

\[ J_x(x) = \frac{x}{\sqrt{\pi \Gamma(x+\frac{1}{2})}} \int_{1}^{\infty} (1-\omega^2)^{-\frac{x}{2}} \cos(\omega x) d\omega \]  

(8)

Firstly, Eq. (8) that is obtained using the general form of the Bessel function is added to analytical model of regular SPWM equation in order to eliminate the odd ordered harmonic contents (Eq. (9)).

\[ V_0(t) = \left[ \frac{m_s V_{dc}}{2} \cos(\omega_c t) \right] \]  

\[ + \left[ \frac{2V_{dc}}{\pi} \sum_{k=1}^{\infty} J_0(k \cdot m_s \frac{\pi}{2}) \right] \sin \left( k \cdot \omega_c t + \frac{k \cdot \pi}{2} \right) \]  

(9)

where, \( m_s \) is the amplitude of modulation ratio, \( V_{dc} \) is the DC supply voltage, \( \omega_c \) is the reference frequency, \( \omega_c \) is the carrier frequency and \( J_0 \) is the Bessel function.

First component of Eq. (9) is the fundamental component that is also known as regular SPWM model. The second part of the equation defines amplitude of harmonics located at the carrier frequency and multiples of carriers. The Bessel function arranged in this way eliminates the harmonics caused by the carrier and side bands of carrier in SPWM modulation. According to modulation theory, a square wave in the time domain generates side bands on its own bandwidths in frequency domain that is explained with sinc function. Therefore, side band harmonics of carrier frequency are required to be eliminated in addition to carrier harmonics analyzed in Eq. (9). The enhanced SPWM modulation scheme is obtained as seen in Eq. (10) by considering the additional Bessel function that provide to eliminate side band harmonics of carrier in Eq. (9). The output periodic voltage waveform, \( V_0(t) \), consists of three major terms to eliminate possible harmonic contents in generated AC output. The carrier frequency determines the rate at which the switching elements will change their status, and affects the distribution of the harmonics of the output. The first term of Eq. (10) gives the amplitude of fundamental component, which is directly proportional to \( V_{dc} \) and the amplitude of modulation ratio, \( m_s \), which is defined as in Eq. (11). The second term of Eq. (10) depicts the amplitude of the harmonics at the carrier frequency and the multiples of carrier. The last term indicates the amplitudes of the harmonics in the sidebands around each multiple of the carrier frequency.

\[ V_0(t) = m_s V_{dc} \cos(\omega_c t) + \frac{2V_{dc}}{\pi} \sum_{k=1}^{\infty} J_0(k \cdot m_s \frac{\pi}{2}) \sin \left( k \cdot \frac{\pi}{2} \right) \]  

\[ \times \cos \left( k \cdot \omega_c t \right) \]  

\[ + \frac{2V_{dc}}{\pi} \sum_{k=1}^{\infty} \sum_{l=1}^{\infty} \frac{J_l(k \cdot m_s \frac{\pi}{2})}{k} \]  

\[ \times \sin \left( \left( k \cdot l + \frac{\pi}{2} \right) \cos(k \cdot \omega_c t + l \cdot \omega_c t) \right) \]  

(10)

where, \( m_s \) is the amplitude of modulation ratio, \( V_{dc} \) is the DC supply voltage, \( \omega_c \) is the sinusoidal reference frequency, \( \omega_c \) is the triangular reference frequency and \( J_0 \) and \( J_1 \) are the Bessel function.
where $V_p$ is the peak value of the modulating signal and $V_t$ is the peak value of carrier triangular signal. The line voltage rates of inverter are determined according to modulation indexes ($m_i$) which defines the operating areas as linear modulation ($m_i \leq 1$) or over-modulation ($m_i > 1$) ranges. The line voltages are limited to $(\sqrt{3}V_d/2)$ of DC line in linear modulation range and limited to $(4/\pi\sqrt{3}V_d/2)$ in over modulation range [5,31]. The SPWM modulator acts as an amplifier in the linear modulation range with the gain parameter ($G$) that is seen as in Eq. (12) by combining the Eqs. (10) and (11).

$$G = \frac{0.5m_i V_d}{V_p} = \frac{0.5V_d}{V_t}$$ \hspace{1cm} (12)

The gain yields 78.55% of the peak value of the square voltage while $m_i = 1$. In SPWM control technique, the output voltage is defined as given in Eqs. (13) and (14) in linear modulation range and the over-modulation, respectively.

$$V_{AB} = V_{BC} = V_{CA} = m_i \frac{\sqrt{3}V_d}{2} \hspace{0.5cm} 0 \leq m_i \leq 1$$ \hspace{1cm} (13)

$$\frac{\sqrt{3}V_d}{2} < V_{AB} = V_{BC} = V_{CA} < \frac{4}{\pi} \frac{\sqrt{3}V_d}{2} \hspace{0.5cm} m_i \geq 1$$ \hspace{1cm} (14)

2.3. Implementing the Simulink model of the inverter

The complete design of SPWM controlled inverter is illustrated in Fig. 3. The model contains two main parts which are constituted...
by modulator block and switching devices of inverter. The SPWM modulator generates unipolar switching signals in order to control the three-phase inverter. The output of the inverter is connected to a load over an L-C filter that contains 1 mH inductor and 6 μF capacitor. In the unipolar SPWM modulation, the phase voltage varies between positive peak and zero level in case of carrier signal exceeds the modulating reference signal in the interval of 0 ≤ ωt ≤ π while the voltage varies between negative peak and zero level in the left part of a period. The mentioned states are shown in Fig. 4 as indicating modulator signals, which are compared in the SPWM modulator block of model in the first curve. The S1 switching signal for the upper switch of one of the phase legs is seen in the second curve, while S4 switching signal for the lower switch of a phase leg is depicted in the third curve, and the output phase voltage of inverter in the last curve. The \( m_i \) value of modulator is set to 0.8 adjusting the proportion of modulating sinusoidal signal to triangular carrier at 500 Hz. The output line frequency is adjusted to 50 Hz due to predefined frequency of modulating signal.

**Table 1**

<table>
<thead>
<tr>
<th>State</th>
<th>Switching orders</th>
<th>( V_{oa} )</th>
<th>( V_{ob} )</th>
<th>( V_{oc} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>On On Off Off Off On</td>
<td>( V_d ) 0 (-V_d)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>On On On Off Off Off</td>
<td>0 ( V_d ) (-V_d)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Off On On On Off Off</td>
<td>(-V_d ) ( V_d ) 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Off Off On On Off On</td>
<td>(-V_d ) 0 ( V_d )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Off Off Off On On On</td>
<td>0 (-V_d ) ( V_d )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>On Off Off Off On On</td>
<td>( V_d ) 0 (-V_d)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>On Off On Off On Off</td>
<td>0 0 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Off On Off On Off On</td>
<td>0 0 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Fig. 5.** Inverter output voltage and current waveforms. (a) Three-phase line and rms voltages. (b) Three-phase line currents.
The line voltage measured at the output of inverter is seen in Fig. 4d when the inverter is controlled at 0.8\textasciimac{m}i. The switching signals generated in the modulator block are applied to the full-bridge inverter block, which is constituted in Simulink according to topology given in Fig. 2. The phase outputs of inverter are obtained at +50 V, 0 V, and −50 V levels in Simulink studies when 50 V\textsubscript{dc} supply utilized in analyses. In order to prevent undefined output levels in the VSI, and thus undefined AC output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously.

There are eight predefined switching states provided using modeled SPWM controller as shown in Table 1. Two switching states (7th and 8th) generate the zero level while the other states generating the positive and negative AC voltages of inverter. In this case, the AC line currents freewheel through either the upper or the lower components [1,2,4].

The line voltage measured at the output of inverter is in Fig. 4d when the inverter is controlled at 0.8\textasciimac{m}i. The switching signals generated in the modulator block are applied to the full-bridge inverter block, which is constituted in Simulink according to topology given in Fig. 2. The phase outputs of inverter are obtained at +50 V, 0 V, and −50 V levels in Simulink studies when 50 V\textsubscript{dc} supply utilized in analyses. In order to prevent undefined output levels in the VSI, and thus undefined AC output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously.

There are eight predefined switching states provided using modeled SPWM controller as shown in Table 1. Two switching states (7th and 8th) generate the zero level while the other states generating the positive and negative AC voltages of inverter. In this case, the AC line currents freewheel through either the upper or the lower components [1,2,4].

The Simulink design is analyzed with Y-connected serial R–L loads, which are combined connecting a 30 Ω resistor and 10 mH coil at the outputs of each phase. The output voltages and currents of the three-phase inverter are illustrated in Fig. 5a and b with the 5 kHz switching frequency and 0.8\textasciimac{m}i conditions. The output voltage is measured about 37 V while the rms value is 24.55 V in the experiments. The line currents under the same load configuration is 0.407 A.

3. Experimental study

3.1. Experimental setup

The block diagram of the three-phase inverter is shown in Fig. 6. The experimental setup is built by considering the requirements of Simulink model. The SPWM switching signals that are generated by TMS320F2812 DSP are applied to IGBT gate drive circuit. The full-bridge circuit is built with 2MBI150U2A-060 dual-in-package IGBT modules of Fuji Electric Device Technology [32]. The collector-emitter voltage of IGBT modules is 600 V and collector current...
is 150 A in continuous conducting modes. The gate-emitter voltage is ±20 V, while turn-on and turn-off times are about 0.40 μs [32].

The gate driver circuit is developed using EXB-840 IGBT driving circuit, which is capable of driving IGBTs up to 1200 V with isolated gate supplies [33]. The phase outputs of inverter are filtered with 1 mH–6 μF passive LC filter. The line voltages and line currents are measured using LA-55P current sensors and LV-25 voltage sensors. The developed experimental system is illustrated in Fig. 7.

LA-55 current sensor is capable of measuring the line currents up to 50 A using the magnetic flux carried on the transmission line. LV-25 voltage sensor measures the line or phase voltages converting the line current to voltage over a measurement resistor in the 2500:1000 conversion ratios [34,35].
3.2. Generating the SPWM with DSP

The SPWM modulation scheme is generated using eZdsp F2812 board as depicted in Fig. 7. The PWM generation in a DSP is controlled by General Purpose (GP) timers, which perform the operations under the control of Event Manager-A (EVA) with GP Timer 1/2 and Event Manager-B (EVB) with GP Timer 3/4. All the GP Timers are 16-bit which are called as TxCNT for up-down counter, TxCMPR for timer-compare operation, TxPR for timer-period register, and TxCON register for timer-control register. The other units of Event Managers are full-compare/PWM units, capture units, and quadrature–encoder pulse (QEP) circuits. Each Event Manager of F2812 DSP is capable to generate up to six-channel PWM outputs separately, thus the deadband Generation can be enabled/disabled for each compare unit output individually. The deadband-generator circuit produces two outputs (with or without deadband zone) for each output signal of compare unit [36,37].

The advantage of applying symmetric PWM signal is that two inactive zones of the same duration at the beginning and at the end of each PWM period are equivalent. This symmetry is shown to cause fewer harmonic than asymmetric PWM signal in the phase currents of an AC motor, such as induction and DC brushless motors, when sinusoidal modulation is used. Fig. 8 shows two examples of symmetric PWM waveforms [38]. To create a PWM signal with a specific frequency and duty cycle, the values for the period and the compare registers need to be calculated. In order to calculate the values, the proper SYSCLKOUT frequency should be known which is 150 MHz for TMS320F2812 DSP. The calculation of period value and compare values are given in Eqs. (15) and (16) below:

$$\text{Table 2}$$

<table>
<thead>
<tr>
<th>Harmonic order</th>
<th>$f_{sw} = 5$ kHz</th>
<th>$f_{sw} = 10$ kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$m_i = 0.8$</td>
<td>$m_i = 1$</td>
<td>$m_i = 1.2$</td>
</tr>
<tr>
<td>3rd</td>
<td>0.13%</td>
<td>0.13%</td>
</tr>
<tr>
<td>5th</td>
<td>0.28%</td>
<td>0.28%</td>
</tr>
<tr>
<td>7th</td>
<td>0.29%</td>
<td>0.29%</td>
</tr>
<tr>
<td>11th</td>
<td>0.16%</td>
<td>0.16%</td>
</tr>
<tr>
<td>13th</td>
<td>0.16%</td>
<td>0.16%</td>
</tr>
</tbody>
</table>

Fig. 12. Line currents of inverter, filtered ($I_R$ and $I_S$) and unfiltered outputs ($I_T$).

Fig. 13. Simulation and experimental result of line currents at 5 kHz switching frequency. (a) $m_i = 0.8$ simulation. (b) Experimental study while $m_i = 0.8$. 

$$\text{Table 2}$$

<table>
<thead>
<tr>
<th>Harmonic order</th>
<th>$f_{sw} = 5$ kHz</th>
<th>$f_{sw} = 10$ kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$m_i = 0.8$</td>
<td>$m_i = 1$</td>
<td>$m_i = 1.2$</td>
</tr>
<tr>
<td>3rd</td>
<td>0.13%</td>
<td>0.13%</td>
</tr>
<tr>
<td>5th</td>
<td>0.28%</td>
<td>0.28%</td>
</tr>
<tr>
<td>7th</td>
<td>0.29%</td>
<td>0.29%</td>
</tr>
<tr>
<td>11th</td>
<td>0.16%</td>
<td>0.16%</td>
</tr>
<tr>
<td>13th</td>
<td>0.16%</td>
<td>0.16%</td>
</tr>
</tbody>
</table>
Period Value (P.V.) = \frac{HSPCLK}{2 \pi \times (PWM \text{ Freq.})} \quad (15)

where HSPCLK = SYSCLKOUT/(Input Clock Prescaler). The compare register value is calculated as given in the following equation:

\text{Compare Value} = (P.V.) \times \frac{(\text{Duty Cycle})}{100} \quad (16)

The flowchart of the SPWM generating software compiled using CCS is depicted in Fig. 9. The initial setup and enable procedures are prepared in order to obtain six channels SPWM over EVA module using PWM1–PWM6 outputs.

The generated SPWM switching signals without deadband are shown in Fig. 10a and b for PWM1–2–5–6 outputs, and the 2 μs deadband example is illustrated in Fig. 11. The appropriate deadband between two PWM outputs can be inserted using the DBTCON register. The deadband circuitry of the TMS320F2812 reduces the active portion of the odd PWM channels from the leading transition end. However, the deadband circuitry increases the active portion of the even PWM channels from the lagging transition end. The switching signals generated using eZdsp F2812 development board are applied to gate drive circuit seen in Fig. 7. The simulation studies are verified utilizing implemented application board under same conditions such as similar modulation and load parameters and the performance comparison of both the simulation and experimental studies are analyzed in the next section of this paper.

4. Comparison of the simulation and experimental study

It is a widely studied area to eliminate harmonic contents in an output waveform owing to control algorithm. Although there are numerous studies performed in this subject, some of them are especially compared in this paper since existing the similarity between them [15–19,39–41]. It is intended to decrease the THD ratio by arranging dead-band times in switching orders in [15], as done in [16–19]. Even though these studies propose that the dead-band arrangement decreases the THD, it is seen that side band harmonics in the output FFT spectrums those increase the THD ratio. The most important point of these studies overlooked is harmonic contents generated by carrier frequency and side-bands of carrier frequency. This situation is clearly seen in [39] where the higher ordered harmonic contents in FFT spectrum and their effect in output waveforms are depicted. Although Refs. [40] and [41] are focused on predictive control algorithms to reduce the required calculations, the side-band harmonics are permanently seen as a result of control strategy applied to inverter. In the proposed SPWM control scheme, the side-band harmonics are eliminated in addition to arrange dead-band intervals. The enhancements obtained and experimental results are analyzed with following figures and table.

The system implemented is controlled using various \(m_i\) and \(f_{sw}\) parameters while the inverter loads were only resistive (30 Ω) and resistive–inductive (30 Ω–10 mH). The switching frequency is set to 5 kHz and 10 kHz while the modulation index varies from 0.8 to 1.2. The effect of filtering on the output line currents of inverter is depicted in Fig. 12. The R and S phase switching signals are filtered in order to determine the effect of the filter on the output parameters of inverter, while the T phase output is obtained unfiltered.

The simulation model is verified by experimental studies with several measurements such as line currents as depicted in Fig. 13. The spikes on the line currents will also increase proportionally to...
modulation index. The harmonic analyses performed in the simulation studies showed that the THD ratios are 0.88% while $m_i$ is 0.8, 1.66% while $m_i$ is 1.0 and 3.04% while $m_i$ is 1.2 conditions at 5 kHz switching frequency.

The sideband harmonics such 3rd, 5th, 7th, 11th, and 13th are increased rapidly in the over-modulation operation area. The sideband harmonics measured according to various $m_i$ values at 5 kHz switching frequency are depicted in Table 2. The first column of Table 2 shows that the side band harmonics are being attenuated during the 0.8$m_i$ control situations against the alternative control strategies. The seventh harmonic in the second column increases the THD ratio of line current while the fifth content is distorting the output current in the third column.

The least harmonic containing operation status at 10 kHz switching can be obtained by setting the modulation index to 1.0 as seen in the fifth column of the Table 2. It is possible to see the side band harmonics and their effects on THD ratio in Fig. 14. One of the measured line currents (R-line) are analyzed for THD curves in Fig. 14 during the inverter is loaded with a serial R–L load and controlled at 5 kHz switching frequency. The current measurement are obtained using LA-55 current sensor with 1:10 rms conversion ratio. The fundamental signal in Fig. 14a is measured as $24V_{rms}$ while the converted load current is measured as $24.7V_{rms}$. The highest side band harmonics are detected at 0.01% ratio against 0.7–0.8$V_{rms}$ values. The most effective side band harmonics such as 5th, 7th, 11th, and 13th exhibit an increment while the modulation index is exceeding the linear operation area as seen in Fig. 14a. The measurement in Fig. 14b is performed at 10 kHz switching frequency. The side band harmonics in Fig. 14b are measured around 7% and 8% with $m_i = 0.8$ operating conditions.

5. Conclusions

The proposed SPWM algorithm is developed using eZdsp F2812 evaluation board and applied to a three-phase full bridge inverter. The simulation studies are performed using Matlab/Simulink to prove the accuracy of the improved SPWM modulator. The proposed SPWM scheme applies digital filtering to carrier and reference signals in modulator. The switching states are obtained with interpolation of samples that are used to regenerate the
sampled modulation signals in the developed mathematical model
of the SPWM scheme. An interpolation process in the discrete time
domain is equivalent to filtering process in frequency domain. The
harmonic elimination feature of the developed modulation scheme
is increased by adding digital filtering operations with interpola-
tion method. The calculation method that improves the harmonic
elimination ability of the modulator is easily performed with
DSP. The current and voltage analyses of the inverter are realized
under several operating conditions such as various switching fre-
quency and modulation indexes. It is determined that the side
band harmonics are increased proportional to switching frequency.
The measured THD values verify that the DSP controlled system is
capable to diminish harmonic contents according to previous stud-
ies compared in the introduction and comparison parts of this
paper.

The DSP controlled full-bridge inverter is also operated using
200Vdc supply to generate 380 V three-phase AC line outputs. The
proposed novel SPWM scheme is verified in terms of harmonic
elimination issues at base and side band frequencies. The simulta-
neous calculation of switching angles and intervals is also
proposed instead of look-up table usage in order to improve the re-
sponse of controller. Converting the inverter topology to a multi-
level such as neutral point clamped or cascaded H-bridge will de-
crease the dv/dt ratio and the THD ratios caused by side band
harmonics in high frequency switching conditions as a future
work. In this situation, the H-bridge inverter topology may also
provide higher harmonic rejection or mitigation ability to inverter.

References

[1] Bose BK. Modern power electronics and AC drives. USA: Prentice Hall Inc.;
2002.
2005.
harmonics with symmetrical output current for single-phase ac/ac matrix
[7] Ramasamy M, Thangavel S. Photovoltaic based dynamic voltage restorer with
power saver capability using PI controller. Int J Electri Power Energy Syst
modulation algorithm for high power multilevel inverters. In: Power
2011;29:565–70.
general hybrid topology of multilevel inverter. In: Proceedings of the interna-
tional symposium on power electronics, electrical Drives and motion;
[12] Shireen W, Tao L. A DSP-based active power filters for low voltage distribution
[13] Azl N.A. A DSP-based regular sampled pulse width modulation (PWM)
technique for a multilevel inverter. In: Proceedings of the international
space-vector modulation for two-level inverter. Int J Electri Power Energy Syst
2012;38:9–19.
main aspects in the harmonics generation. In: Proceedings of brazilian power
single-stage maximum power point tracking PV inverter. In: Applied power
electronics conference and exposition (APEC); 2010. p. 948–52.
voltage-source inverters for distributed generation systems. IET Renew Power
[18] Bakar M.S., Azl N.A. Simulation of a regular sampled pulse width modulation
(PWM) technique for a multilevel inverter. In: Power engineering conference
[19] Lin W. A new approach to the harmonic analysis of SPWM waves. In:
Proceedings of the IEEE international conference on mechatronics and
[20] Pan Z., Fang Z. A novel SPWM method with voltage balancing capability for
multilevel rectifier/inverter systems. In: Applied power electronics conference;
[21] Hua C.C., Wu C.W., Chiang C.W. Fully digital control of 27-level cascade
inverter with variable DC voltage sources. In: 2nd IEEE conference on
[22] Benvenuto N, Cherubini G. Algorithms for communications systems and their
1998.
[26] Uluisik C, Sevgi L. A tutorial on Bessel functions and numerical evaluation of
Bessel integrals. IEEE Anten Propagat Mag 2009;51:222–33.
[27] Chengyun Z., Minyi C., Je W. Design and implementation of real time
crossover based on bessel digital filter. In: International conference on
[29] Gross FB. New approximations to Jn and Jn functions. IEEE Trans Anten
[30] Chen B, Hsu YY. An analytical approach to harmonic analysis and controller
[31] Colak L, Kabalcı E, Bayindir R. Sagiroglu S. The design analysis of a 5-level
cascaded voltage source inverter with low THD. In: Proceedings of
international conference on power engineering, energy and electrical
products/lv%2025-1000%20e.pdf>.
c2600.spectrumdigital.com/ezf2812/docs/ezf2812_techref.pdf>.
[37] TMS320F28x Event manager [EV] peripheral reference guide. Texas
Instruments, May 2002.
[38] Figarado S, Bhattacharya T, Mondal G, Gopakumar K. Three-level inverter
scheme with reduced power device count for an induction motor drive with
of multilevel cascaded h-bridge inverters. IEEE Trans Ind Electron
2010;57:2691–9.
[40] Mahrous EA, Rahim NA, Hew WP. Three-phase three-level voltage source
inverter with low switching frequency based on the two-level inverter