Thermo-mechanical design of a generic 0-level MEMS Package using Chip Capping and Through Silicon Via’s

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Abstract
This paper describes the thermo-mechanical design of an advanced zero-level capping technology used for packaging of a MEMS die. The package approach uses Intermetallic Compound (IMC) bonding to seal the MEMS die with a cap, and uses Through Silicon Via’s (TSV) to provide the electrical connections from the MEMS die to the second level substrate (LTCC or PCB). Advanced FEM based thermo-mechanical simulations are performed to estimate the impact of processing and temperature cycling on the mechanical stresses and deformations induced in the structure. Special focus goes to the rigid CuSn IMC bond, the copper TSV using a polymer dielectric and the cap deflection under a pressure of 1 bar (vacuum inside) and 90 bar (simulating overmoulding). Finally, the impact of assembling the MEMS package on an LTCC substrate and an FR4 printed circuit board with CuSn, respectively solder connections is investigated with respect to the package reliability, the cap deflection and the strain and anchor rotation at location of the MEMS.

1. Introduction to 0-level MEMS packaging
Today, the commercialization of (RF-)MEMS, is greatly hampered by two critical success factors, namely, the development of an appropriate packaging technology and solving the reliability issues providing MEMS components working for a long time. RF-MEMS switches for instance, contain movable fragile parts that must be packaged in a clean and stable environment. The same applies to RF-MEMS varactors and variometers. RF-MEMS resonators require high levels of vacuum, in order to have sufficiently low damping at resonance. A specific low-cost packaging approach is required offering protection during fabrication as well as during operation. Although encapsulation of the MEMS device is possible using proven hermetic 1-level ceramic or metal can packages [1-3], the cost can be high and poses technological complications. For instance, standard wafer sawing cannot be used as it will destroy the MEMS device. This makes that packaging is preferably carried out on the wafer during wafer processing, prior to die singulation. This packaging step is referred to as wafer-level or 0-level packaging.

There is clearly a trend towards 0-level packaging for MEMS [4]. The 0-level package defines the first protective interface for the MEMS device, achieved through on-wafer encapsulation of the movable parts in a sealed cavity. In addition to a low-cost fabrication process and physical protection, the 0-level package must be strong, equipped with electrical signal feed-throughs and be (near-) hermetic, preventing any particles and moisture from migrating into the region of the MEMS and the region underneath the released MEMS structure. On the other hand, 0-level packaging should not increase the die form factor too much, both for cost reasons and for implementation reasons. Some applications such as cell phones also put a constraint on the total height of the die. Once 0-level packaged, the wafer can be diced without any danger of demolishing the MEMS device. The individual chip assemblies can next be mounted via wire-bond or solder bumps in a low-cost plastic molded package, e.g., SOIC-8 or BGA package. Alternatively, the assembly can be handled as a chip scale package (CSP) to be directly joined to a printed circuit board.

Figure 1: Illustration of the 0-level packaging of a MEMS device based on “chip-capping” encapsulation

In case of 0-level chip capping, it is common practice to bond a recessed capping chip or die onto the MEMS device wafer, as illustrated in Figure 1. Capping is done either as a chip-to-wafer (C2W), also called die-to-wafer (D2W), or as wafer-to-wafer (W2W). The end result in essence is the same. The bonding & sealing ring is typically 50 to 300 µm in width, whereas the cap has a die thickness that is typically in the range of 100 to 500 µm.
This paper focuses on thermal-mechanical aspects of the MEMS-package design. Temperature variations occur during processing (e.g. bonding at elevated temperatures) and in operation (ambient temperature fluctuations) and cause mechanical stresses in a structure consisting of different materials (different coefficient of thermal expansion). One requirement is that the package should not have critical fractures as it has to provide a protective environment during the whole life time of the MEMS. Also the interconnections from the MEMS to the outer of the package must not fail in order provide signal transfer. Furthermore, the package structure should not cause mechanical stress on the MEMS itself as their electro-mechanical performance is sensitive to mechanical stress (e.g. mechanical resonance frequency of the MEMS may be stress dependent).

2. Description of the 0-level MEMS Package

Figure 2 shows imec’s chip capping concept for packaging (RF-) MEMS dies. The MEMS, e.g. an RF switch or a resonator, is realised on top of a high resistive silicon die, so-called MEMS-die. A cap made of the same high resistive silicon material, is assembled to the MEMS die in order to protect the MEMS structure. Unique for this concept is that the MEMS die is flipped down onto the cap and the through silicon via’s (TSVs) to make connections to the outer world, are made in the cap instead of the MEMS die. On the bottom side of the cap, bonding pads are foreseen which can be used to make first level interconnections to an intermediate substrate (e.g. LTCC) or even second level interconnections by soldering the MEMS package directly onto the printed circuit board. Figure 3 shows an assembly for which multiple caps with different sizes are bonded onto a MEMS wafer in one flip chip operation.

The IMC bonding provides the hermetic sealing of the cap to the MEMS die connection but also provides the electrical connection from the MEMS die to the cap (Figure 4). The IMC bonding results from a sandwich of Cu-Sn-Cu [5]. At both dies, a 5 µm thick copper ring is applied. At one of the two dies, typically the cap, also a 5 µm thick Sn layer is electroplated. The connection between the two dies is made by increasing the temperature just above the melting temperature of Sn. At the same time, a pressure is applied. Thanks to the combination of melting and pressure, the joint is formed. During this process the “soft” Sn is transformed into the stiff and brittle CuSn intermetallic compound by interdiffusion.

The Cu TSVs provide the interconnection from the top to the bottom of the CAP (Figure 5). First, via’s of about 70 µm diameter are etched in the 100 µm thick silicon die using DRIE. A uniform polymer layer is applied to function as a dielectric. Finally, copper is electroplated in the via [6].
3. Description of Finite Element Model

A complex 3D finite element model (FEM) is constructed for the MEMS package using the software code Msc.Marc\textsuperscript{TM}. Figure 6 shows the model for a 2 by 2 mm\textsuperscript{2} MEMS package, assembled on an LTCC substrate. Thanks to the square symmetry, only one–quarter of the structure needed to be modelled. The symmetry is achieved by assuming no displacement perpendicular to the plane. A different axi-symmetric model is created to investigate the copper TSV in more detail.

Following advanced FEM features are used to build this model:

- Contact bodies for attaching different meshes with non-coinciding nodes
- Non-linear material properties, such as ideal plasticity for Al and Cu, hypo-elastic properties for polymer.
- Element de-activation: elements of a specific material are only activated at the moment they are applied in the processing cycle.
- Delamination feature for bodies in glue contact for simulating potential adhesion failures.

The material properties used in this model are summarised in Table 1.

4. Results – part 1: stress in CuSn IMC after cap-to-MEMS die bonding

Once the top wafer with MEMS structures and the bottom cap wafer with TSV’s are processed, the two wafers are bonded to each other by melting the tiny Sn layer together with an external pressure. As this process occurs at 250°C, a residual stress in the relative brittle IMC layer is expected after cool down to 20°C due to thermal CTE mismatch between the copper and the silicon. Figure 8 shows the maximum principal stress at 20°C after bonding. A quite uniform tensile principal stress over the whole sealing IMC is found with a magnitude of about +450 MPa. As the IMC is not allowed to shrink by the stiff silicon, a large tensile stress is generated. Plastic deformation of the copper could compensate the mismatch between the IMC and the Si. However, the stress in the copper at 250°C is compressive (-200 MPa), and becomes tensile (+200 MPa) at room temperature which is an elastic stress overlap of 400 MPa (Figure 9).
This high tensile stress for the brittle CuSn bond could become a risk factor for this MEMS packaging concept. However, first bonding experiments resulted in a nice bond (see also Figure 4) which stayed intact after processing. First shear tests revealed that the IMC bonding was not the critical location of failure. Further experiments are planned to measure the ultimate stress of these CuSn bonds.

5. Results – part 2: stress in copper TSV

The structure of the TSV is shown in Figure 7. A polymer is located in between the silicon and the copper via. This polymer has hypo-elastic properties, allowing large deformations without large stress build-up. Thanks to this property, the polymer can compensate the large thermal CTE mismatch between the copper TSV and the silicon. As a consequence, the copper via is almost not stressed under temperature cycling loading.

There could be an issue with the adhesion of the polymer to the copper and the silicon. The nominal thickness of this polymer layer is about 5 µm. But due to processing reasons, the thickness of the polymer layer near the top area is only 0.7 µm, while the copper layer is very thick at this location. The FEM simulation reveals that there is a stress concentration in the polymer at that point.

In order to investigate the adhesion strength, the advanced “delamination” feature in the software code has been used. This feature allows having separation of the mesh between two materials if the following requirement over the interface is fulfilled.

\[
\left( \frac{\sigma_{\text{shear}}}{\text{ultimate } \sigma_{\text{shear}}} \right)^n + \left( \frac{\sigma_{\text{normal}}}{\text{ultimate } \sigma_{\text{normal}}} \right)^n \geq 1
\]

The exponent \( n \) is chosen to be 2. In order to find the weak place where interface failures could start first, a low ultimate interface strength of 25 MPa is chosen for this study. Figure 11 shows that, indeed, the location where the polymer thickness is lowest, the first interface delamination starts. A parameter study shows that the interface strength should be at least 75 MPa to avoid interface failures.

6. Results – part 3: deflection of the MEMS cap

The distance between the cap and the MEMS die is only about 15 µm. In this small gap, also the MEMS has to function, so the deflection, defined as the relative movement of the cap towards the MEMS die, is limited to only a few µm.

The deflection can be caused by deformation induced by thermal expansion mismatches, but also by the external pressure acting on the cap-to-MEMS die assembly, e.g. 1 bar (= 0.1 MPa) outside pressure when the inner area is vacuum, or temporary even 90 bar can be applied during an overmoulding process. Figure 12 shows the deformed package due to a 1 bar outside pressure (this represents vacuum inside). Figure 13 shows the deflection values for a 2 by 2 mm\(^2\) MEMS package. At room temperature, the deflection is 0.28 µm. Due to CTE mismatches, the deflection is slightly higher at -40°C, and slightly lower at 125°C. However, temperature has clearly a secondary effect on the deflection.
Although the proposed technology does not need to be moulded in order to protect the MEMS, the overmoulding can become interesting in some cases to also protect the package itself. It can then also be used for standard pick and placement assembly. In such moulding process, the pressure can go up to 90 bar. Simulating the deflection as function of the outside pressure reveals that the cap already touches the MEMS die at around 30 bar (Figure 14). So, the current build-up for the 2 by 2 mm\(^2\) package does not allow to be moulded.

A solution is proposed in Figure 15. About 350 additional (Cu-CuSn-Cu) studs are foreseen to connect the coplanar lines at both dies (in the original design, only 6 studs were designed). These 350 studs provide both electrical and mechanical connections. This new design can support the 90 bar pressure. Figure 16 shows that the cap deflection is only about 1.5 µm at 90 bar outside pressure.

7. Results – part 4: impact of assembly on LTCC carrier and PCB

Looking purely to the MEMS package concept, the “silicon on silicon” assembly will not cause thermomechanical stresses due to global CTE mismatch. However, the package still has to be mounted on a substrate which probably has a different CTE. Figure 17 shows two possible assemblies. For the assembly on the rigid LTCC carrier, a rigid CuSn IMC bonding is used. The right assembly is on a standard FR4 board using lead-free solder balls. Following aspects will be compared: maximum stresses in critical IMC sealing bond, the in-plane deformation in the MEMS area and the cap deflection. As reference, these results will be compared with the package before it is assembled on a substrate.
Figure 18 shows the maximum principal stress in the IMC sealing bond (see also Figure 8 for the stress distribution). The assembly to a substrate with different CTE almost does not affect this stress. The main reason is that the IMC is located at the neutral fibre of the MEMS package (both MEMS die and cap are 100µm thick). The existing stress is induced by local CTE mismatches between the silicon and the IMC. As a consequence, the highest stress is found at lowest temperature due to the largest difference with the stress free temperature (= soldering temperature).

A different conclusion can be made with the mechanical impact on the MEMS. Both in-plane deformations over the MEMS length as well as rotations of the MEMS anchor points on the die can affect the performance of the MEMS by changing the mechanical stress in the MEMS (Figure 19). And when this stress become too high, also failures after processing or fatigue failures during operation can happen.

Figure 20 shows the in-plane deformation of the MEMS die as function of the temperature. This deformation is calculated from anchor point to anchor point (for this 2 by 2 mm² package, the chosen distance is 1.1 mm long). The strain values are compared to the free thermal expansion of silicon. Both the package and the package on PCB well follow the free expansion of silicon. However, there is an obviously different behaviour when the MEMS package is assembled on the LTCC carrier. The main reason is the second level interconnection. For the LTCC, a stiff CuSn connection is chosen and this causes a bending of the package, as shown in Figure 20. For the assembly on PCB, a soft solder joint is used and this compensates the CTE mismatch between the package and the PCB.

Figure 18: Maximum principal stress in IMC sealing bond at different temperature and with different assemblies.

Figure 19: Description of the in-plane deformation of the MEMS die (left) and the rotation at the anchor point of a MEMS (right).

Figure 20: In-plane strain in the MEMS substrate (average strain from anchor point to anchor point)

Figure 21: Deformed MEMS package on substrate assembly at -40°C (deformations multiplied by factor 20).

A similar conclusion can be made for the anchor rotation (Figure 22). Figure 21 already showed a reasonable bowing of the MEMS package when it is assembled on LTCC with the rigid CuSn bond. In particular at lowest temperature, the anchor rotation becomes almost 0.001 rad.

Whether the in-plane deformation and MEMS anchor rotation are potential problems of the functionality of the MEMS, depends on the sensitivity of the MEMS to these deformations.
8. Conclusions
An in-depth thermo-mechanical study has been applied to an innovate 0-level MEMS capping technology. For this study, advanced FEM feature are used such as contact, element de-activation, delamination at interfaces and non-linear material behaviour. The mechanical reliability of the structure is simulated after processing and under thermal cycling conditions. It is found that some parts of the build-up are vulnerable to potential reliability problems. In particular the IMC bonding, which is a brittle CuSn interconnection, has already a high stress after processing. Also the copper TSV’s are potential locations for fatigue failure when they are subjected to thermal cycling conditions. The impact of an outside hydrostatic pressure of 90 bar was investigated. The high pressure results in a deflection of the cap touching the MEMS die, which is not desired. A solution that is viable thermo-mechanically is to use dummy mechanical connections over the whole dummy area between the two dies functioning as supporting pillars. Finally, it was found that second level assembly has an impact on the stresses and strains in the MEMS package. The different CTE of the substrate causes stresses and deformations, in particular when a rigid second level interconnect is used. Therefore, the second level may not be neglected for any thermo-mechanical optimisation of a MEMS package.

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